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RF205x Family Application Note Reducing Synthesizer Lock Time

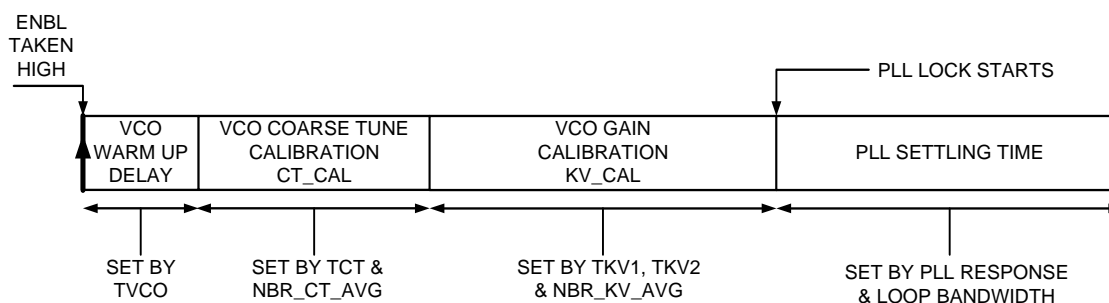RFMD Multi-Market Products Group

Introduction

This document aims to give all of the information required to reduce the lock time of the fractional-N synthesizer used in all of the RF205x family of integrated, configurable components.

In normal operation the synthesizer lock time is increased by the internal VCO calibration mechanisms. These calibrations can be disabled and the calibration timers minimized, in order to reduce the lock time significantly. The fractional-N synthesizer gives the flexibility to be able to increase the loop bandwidth and speed up the lock time further, without compromising suppression of reference spurs. There is though a trade-off between synthesizer phase noise and lock time. Plots are shown to demonstrate the impact of reducing lock time on phase noise.

The lock time or settling time is also highly dependent on the application's specification. For example it could be the time taken to settle within ±25KHz of the final frequency, or ±5KHz of the final frequency. The lock time for the RF205x devices is defined as the time between taking the ENBL line high and for the LO frequency to settle to within a specified offset from the final frequency.

Synthesizer Start-Up And Calibration Times

After activating the synthesizer by taking the ENBL line high there are several steps that the state machine goes through before the PLL acquisition is commenced. This is illustrated below. The crystal oscillator will be activated before enabling the device by setting REFSTBY = 1 in register CFG3 at least 500usecs before taking ENBL pin high, in order to allow the frequency to settle.

Figure 1. Start-Up and Calibration Times

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VCO WARM UP

The first time period allows the VCO to warm up as it comes out of standby, and it's length is set by a timer TVCO in register CFG1. This setting is important, since if set too short the VCO calibration (or PLL acquisition if calibration disabled) will commence whilst the VCO is still drifting after start up, and this will actually lengthen the lock time. If TVCO is set too high there will obviously be a longer delay before the other mechanisms start. The VCO warm up delay is defined by the following equation:

VCO Warm Up Delay = TVCO * 32 / F_{PFD}

Where F_{PFD} is the phase detector frequency.

For the standard 26 MHz crystal and phase detector frequency used with the RF205x devices the optimal TVCO setting is 8 (01000) giving about 9.85 usecs VCO warm up time. The optimal TVCO setting will change if a different phase detector frequency is used.

VCO COARSE TUNE CALIBRATION

The VCO frequency range is set by a bank of seven switched capacitors in parallel with the varactor. The switched capacitors give 128 possible coarse tuning steps. The VCO coarse tune calibration, or CT_CAL, uses a frequency locked loop to centre the VCO by varying the switched capacitors to give the optimal tuning voltage at the programmed VCO frequency. The tuning voltage used is typically about +1.2V, in the centre of the tuning voltage range available from the loop filter op-amp. The target tuning voltage can be changed by varying the coarse tuning voltage setting, P1_CT_V/P2_CT_V. After coarse tuning has completed, the VCO will be on the correct frequency band and the phase locked loop acquisition can begin. For more information please refer to the RF205x Calibration User Guide.
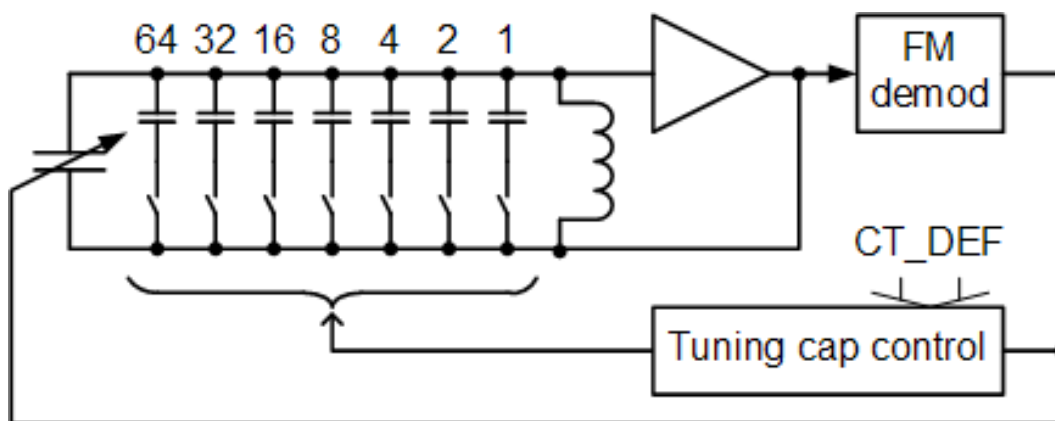

Figure 2. VCO Coarse Tuning

The time spent in the CT_CAL state is given by the sum of the CT_CAL Delay and the CT_Averaging Delay:

CT_CAL Delay = TCT * 32 / F_{PFD}

CT_Averaging Delay = 16 * (2^N1) / F_{PFD}

Where TCT is the coarse tuning timer setting in register CFG4, and N1 is the number of averages set by NBR_CT_AVG in CFG2.

Note that the time set by TCT and NBR_CT_AVG still applies even if the CT_CAL mechanism is disabled. To speed up synthesizer locking then CT_CAL can be disabled and TCT and NBR_CT_AVG set to zero.

With CT_CAL disabled the VCO frequency band still needs to be set. This can be done by programming the correct value for the required VCO frequency into P1_CT_DEF/P2_CT_DEF. This value can be obtained by programming the required frequency with CT_CAL enabled and the default TCT and NBR_CT_AVG settings. After raising ENBL and locking the synthesizer the CT_CAL

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value can be read back from register RB1. This could be done for example when the device is initialized and a look up table of VCO frequency versus CT_CAL constructed. The CT_CAL value will vary between devices due to process and assembly variations, so each RF205x device will need a unique set of CT_CAL data. Temperature variations also need to be considered, the normal recommendation is to recalibrate for every 30°C change.

Note that for the RF2053 with external VCO then CT_CAL is not used and can be disabled.

VCO GAIN CALIBRATION

The VCO gain calibration, or KV_CAL, can be used to tightly control loop response over a range of LO frequencies. This is done by varying the charge pump current to compensate for changes in VCO gain, K_{VCO} in MHz/V, and divide ratio, N. This calibration is disabled by default and not used in the majority of RF205x applications. For more information refer to the RF205x Calibration User Guide.

The time spent in the KV_CAL state is the sum of the two KV_CAL Delays and the KV_Averaging Delay:

KV_CAL Delay 1 = TKV1 * 256 / F_{PFD}

KV_CAL Delay 2 = TKV2 * 256 / F_{PFD}

KV_Averaging Delay = 16 * (2^N2) / F_{PFD}

Where TKV1 and TKV2 are the KV_CAL timer settings in register CFG3, and N2 is the number of averages set by NBR_KV_AVG in CFG2.

Note that the time set by TKV1, TKV2 and NBR_KV_AVG still applies even if the KV_CAL mechanism is disabled. (This is the case when the default register settings are used.) To speed up synthesizer locking then KV_CAL can be disabled and TKV1, TKV2 and NBR_KV_AVG all set to zero.

PLL SETTLING TIME

The PLL settling time is dependent on the loop filter response. This is set by the loop filter component values, the N divider value, the charge pump current setting, and the VCO gain. In general the settling time is directly related to the loop bandwidth, but it's not quite so simple and the loop response should be properly simulated. The phase margin and damping ratio have an effect.

The application's specification time is also important, normally the time for the VCO to settle close to the final frequency. So the smaller the frequency window specified, the longer the settle time.

A rough estimate is given by the following equation:

PLL Settling Time = 2.5 / Loop Bandwidth

So for a typical RF205x synthesizer loop bandwidth of 60kHz then the PLL settling time would be expected to be somewhere in the region of 42 usecs.

The loop filter can be widened to speed up settling, but this will have an effect on synthesizer phase noise. It will also affect the levels of spurious, but with a fractional-N synthesizer the reference spurs are generally well outside the loop bandwidth, typically at 26MHz offset.
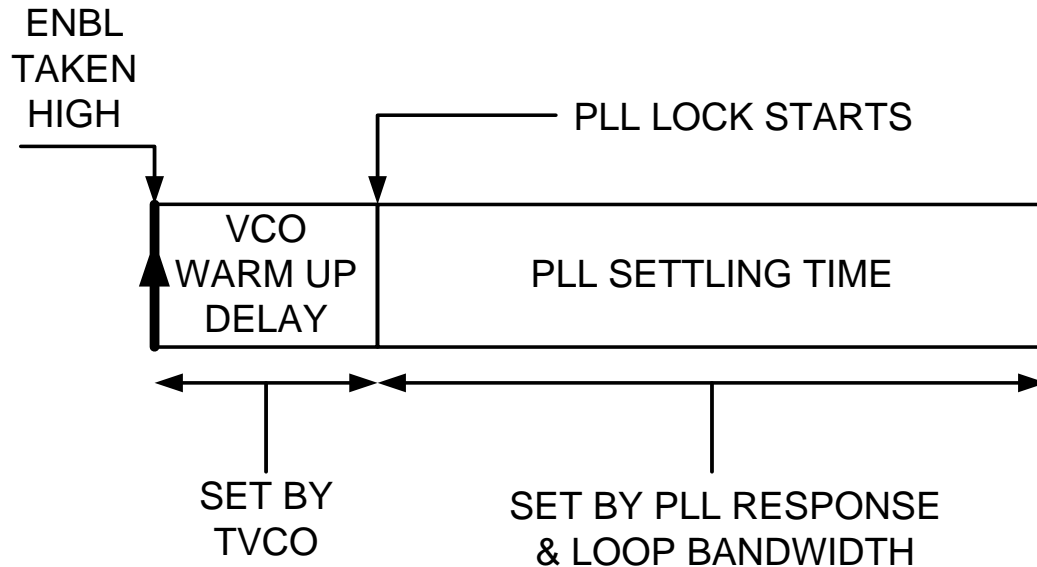
To speed up PLL settling it is best to set the highest charge pump current, set by P1_CP_DEF/P2_CP_DEF = 111111. This gives about 240uA charge pump current, double the default setting of 011111. Increasing charge pump current widens the loop bandwidth.

The loop bandwidth can also be increased by operating with a slightly lower tuning voltage, between +0.7V and +1.0V. This can achieved by performing CT_CAL with P1_CT_V/P2_CT_V set at 8 (01000), lower than the default value of 16 (10000). This

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has the effect of setting the CT_CAL value 1 or 2 bits higher, and the VCO runs at a point with lower K_{VCO}, pushing out the loop bandwidth. The temperature range and VCO drift need to be considered when running with lower tuning voltage.

FAST LOCK SETTINGS

With the CT_CAL and KV_CAL calibrations disabled, and importantly the timers and averaging all zeroed, the start-up simplifies to just the VCO warm-up time and PLL settling time as shown:

Figure 3. Start Up Times for Fast Locking

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Register Settings For Fast Lock

The following table shows the various register settings used for the start up and calibration timings. The default values (chip hardware defaults) are shown along with the values required for fast lock operation, ie the calibrations disabled and all timers minimized.

Bit Name	Register Name	Register Values (HEX)		Note
		Default	Fast Lock	
XO Warm-Up				
REFSTBY	CFG3 [0]	0	1	Always set to 1
SU_WAIT	CFG6 [15:6]	4	0	Set to zero
VCO Warm-Up				
TVCO	CFG1 [13:9]	8	8	Modify as required for VCO startup
CT_CAL				
Px_CT_EN	PLLx0 [13:12]	3	0	Disable CT calibration
TCT	CFG4 [4:0]	F	0	Set CT acquisition time to zero
NBR_CT_AVG	CFG2 [2:3]	2	0	Set CT averaging time to minimum
KV_CAL				
Px_KV_EN	PLLx0 [11:10]	0	0	Disable KV calibration
TKV1	CFG3 [15:12]	0	0	Set KV settle time 1 to zero
TKV2	CFG3 [11:8]	4	0	Set KV settle time 2 to zero
NBR_KV_AVG	CFG2 [1:0]	0	0	Set KV averaging time to minimum

With the default settings CT_CAL is enabled, and KV_CAL disabled. The KV_CAL timers are not zeroed, so there will still be a delay between the end of CT_CAL and the start of PLL acquisition as the state machine runs these timers. The default setting for REFSTBY is 0, so this should always be programmed to 1 at least 500 usecs before enabling the device to allow the crystal oscillator to warm up and settle.

Using the default settings, with the exception of REFSTBY = 1, the equations in the "Synthesizer Start-Up and Calibration TImes" above give the time between taking ENBL high and the start of PLL acquisition as about 70 usecs. This is with a 26 MHz phase detector frequency. This breaks down to 10 usecs for VCO warm up, 20 usecs for the CT_CAL, and 40 usecs for the KV_CAL timers to run.

So just be reducing the KV_CAL timers the lock time will reduce by about 40 usecs. By disabling CT_CAL and minimizing all the timers, the fast lock settings in the table, then the lock time should be reduced by a further 20 usecs. These improvements are not seen exactly in practice, as you are starting the PLL acquisition earlier. The PLL acquisition and settling itself may take slightly longer the earlier it is started since the VCO may still be warming up and drifting.

With CT_CAL and KV_CAL disabled and all timers reduced the time between raising ENBL and the start of the PLL acquisition will be about 11 usecs, dominated by the VCO warm up time.

These times are all for a phase detector frequency of 26 MHz. They can be easily scaled for other phase detector frequencies; although the optimal VCO warm up time itself will be the same and the TVCO setting will need to be adjusted.

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Programming Device Registers for Fast Lock

For a small step in LO frequency just the fractional divider value may need to change, so one or two registers will need to be programmed dependant on whether the MSB and LSB both change. For larger steps the integer divider and VCO coarse tune setting may also change, so three registers will need to be programmed. In some cases the VCO number and LO divider may also change. A register write will take 1.3 usecs at the maximum serial clock rate of 19.2 MHz. The new register value will be clocked into the synthesizer when ENX is taken high at the end of each write operation.

For the RF205x devices it is recommended that ENBL is taken high to ensure reliable synthesizer lock, for any change of LO frequency.

There are several methods of programming the RF205x for fast lock, dependant on the application.

PROGRAMMING WHILST IN STANDBY

The simplest method would be to lower the ENBL line, program the registers for the new LO frequency, then raise the ENBL line to lock the synthesizer at the new frequency. The disadvantage is the time spent in standby whilst the registers are programmed, something of the order of 2 usecs to 5 usecs even with the fastest serial clock rate.
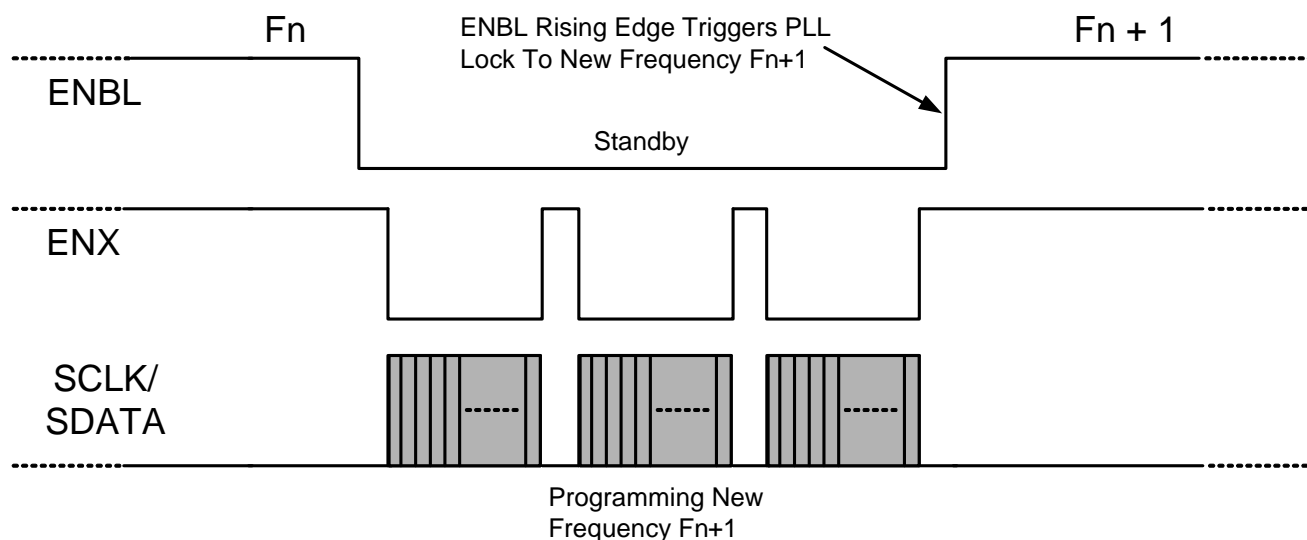
Fn

ENBL Rising Edge Triggers PLL
Lock To New Frequency Fn+1

Fn + 1

ENBL

Standby

ENX

SCLK/
SDATA

Programming New
Frequency Fn+1

Figure 4. **Programming a New LO Frequency Whilst in Standby Mode**

SWITCHING BETWEEN MIXERS

The two register banks give some flexibility. For the RF2051 and devices with two mixers then the typical application will switch between the mixers and two different LO frequencies, say for TX/RX switching. So the register bank for PLL2 can be written when path 1 is active, and PLL1 register bank written when path 2 is active. The MODE pin is used to switch between the mixer paths and the PLL register banks after ENBL is lowered. Then ENBL is raised to activate the new path and lock the synthesizer. In this case the programming time is not so critical.
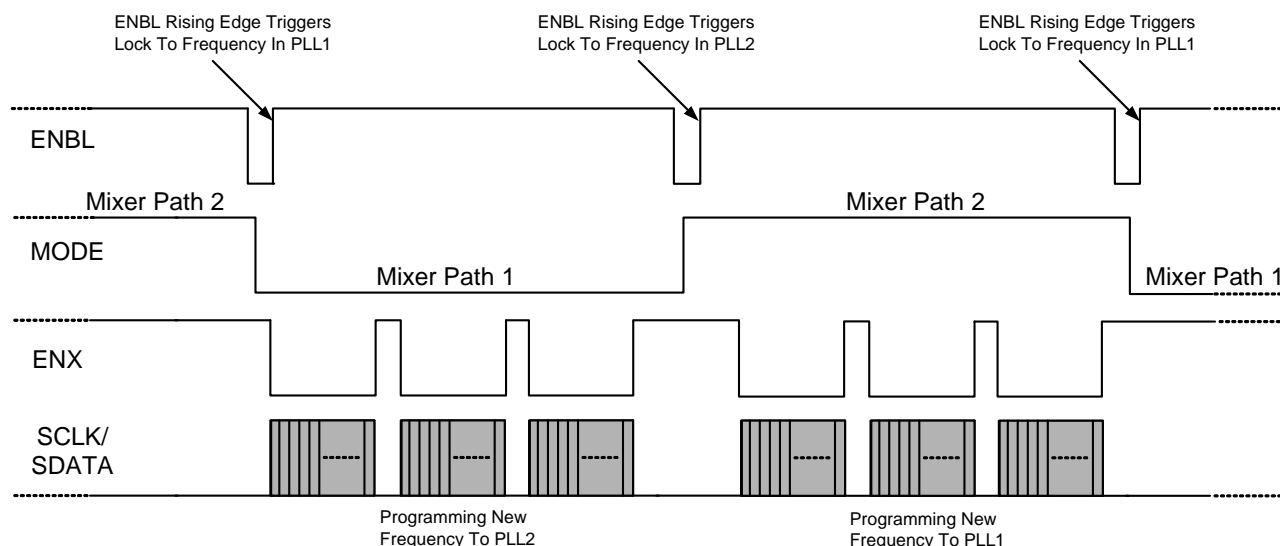
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ENBL Rising Edge Triggers
Lock To Frequency In PLL1

ENBL Rising Edge Triggers
Lock To Frequency In PLL2

ENBL Rising Edge Triggers
Lock To Frequency In PLL1

ENBL

Mixer Path 2

MODE

Mixer Path 1

Mixer Path 2

Mixer Path 1

ENX

SCLK/
SDATA

Programming New
Frequency To PLL2

Programming New
Frequency To PLL1

Figure 5. Programming a New LO Frequency Whilst Switching Between Mixers

FULL DUPLEX MODE

Full Duplex operation is useful as it enables both mixers at once with the same LO frequency routed to both. This enables fast switching between mixers; for example the mixers could be switched on and off as required by switching the mixer supply via the output pins, typically via the balun center tap. To enable Full Duplex mode set FULLD = 1 in CFG1.

In Full Duplex operation the MODE pin now just selects the PLL register bank that is active. This can be useful since when PLL1 is active, with MODE pin low, PLL2 can be programmed. Similarly if PLL2 is active, with MODE pin high, PLL1 can be programmed. To change frequency then ENBL is lowered, then MODE pin changed to set the PLL register bank and LO frequency, then ENBL is raised to lock the synthesizer at the new frequency.

This is ideal for applications where the LO frequency is continually being changed or "hopped." There is no delay between hops whilst registers are programmed.
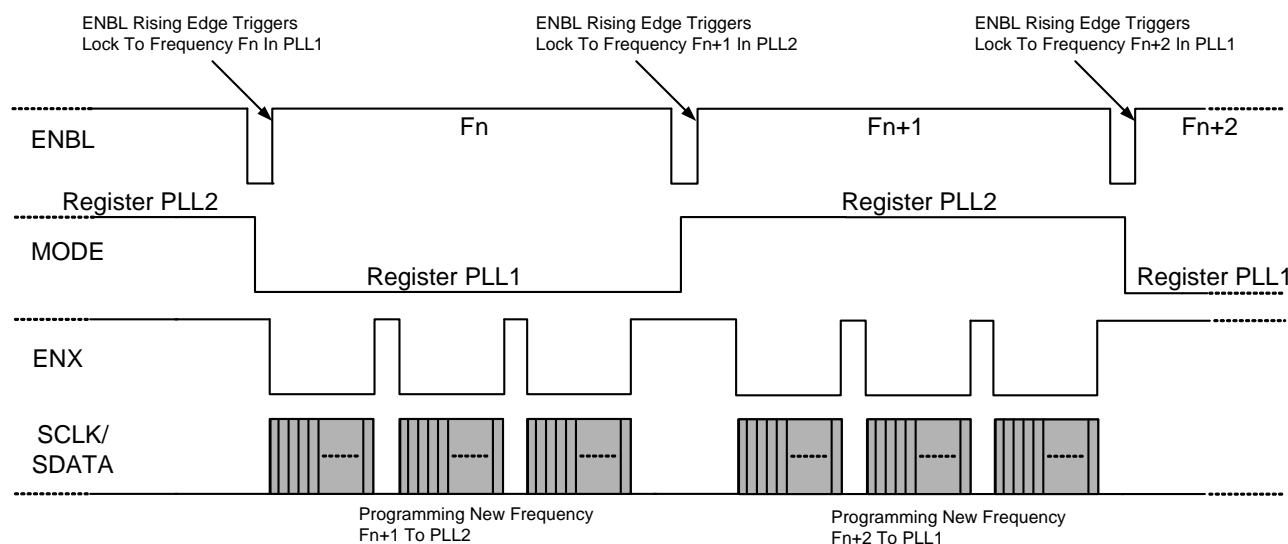
ENBL Rising Edge Triggers
Lock To Frequency Fn In PLL1

ENBL Rising Edge Triggers
Lock To Frequency Fn+1 In PLL2

ENBL Rising Edge Triggers
Lock To Frequency Fn+2 In PLL1

ENBL

Fn

Fn+1

Fn+2

Register PLL2

MODE

Register PLL1

Register PLL2

Register PLL1

ENX

SCLK/
SDATA

Programming New Frequency
Fn+1 To PLL2

Programming New Frequency
Fn+2 To PLL1

Figure 6. Programming a New LO Frequency in Full Duplex Mode

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FULL DUPLEX MODE AND SINGLE MIXER

The RF2052 and RF2053 have only one mixer, but Full Duplex operation can still be used by setting FULLD=1 in CFG1. The MODE pin just changes the active PLL register bank when in Full Duplex mode, and programming is as described above.

COARSE TUNE CALIBRATION

To achieve the fastest lock times with the RF205x devices it is necessary to disable the VCO coarse tune calibration process. With CT_CAL disabled the correct CT_CAL value must be programmed to P1_CT_DEF / P2_CT_DEF in order to centre the VCO on the correct frequency band.

The flow chart below gives a typical process for obtaining the VCO frequency versus CT_CAL values. This could be done at system initialization as shown. It may also be advisable to recalibrate at other times, for example if there has been over 30°C temperature change. The CT_CAL values could be stored in a look up table, and it should be possible to interpolate the CT_CAL curve from measurements taken at a few spot frequencies across the range. Note that each RF205x will need to be calibrated as there will be process and assembly variations that affect the VCO frequency range.
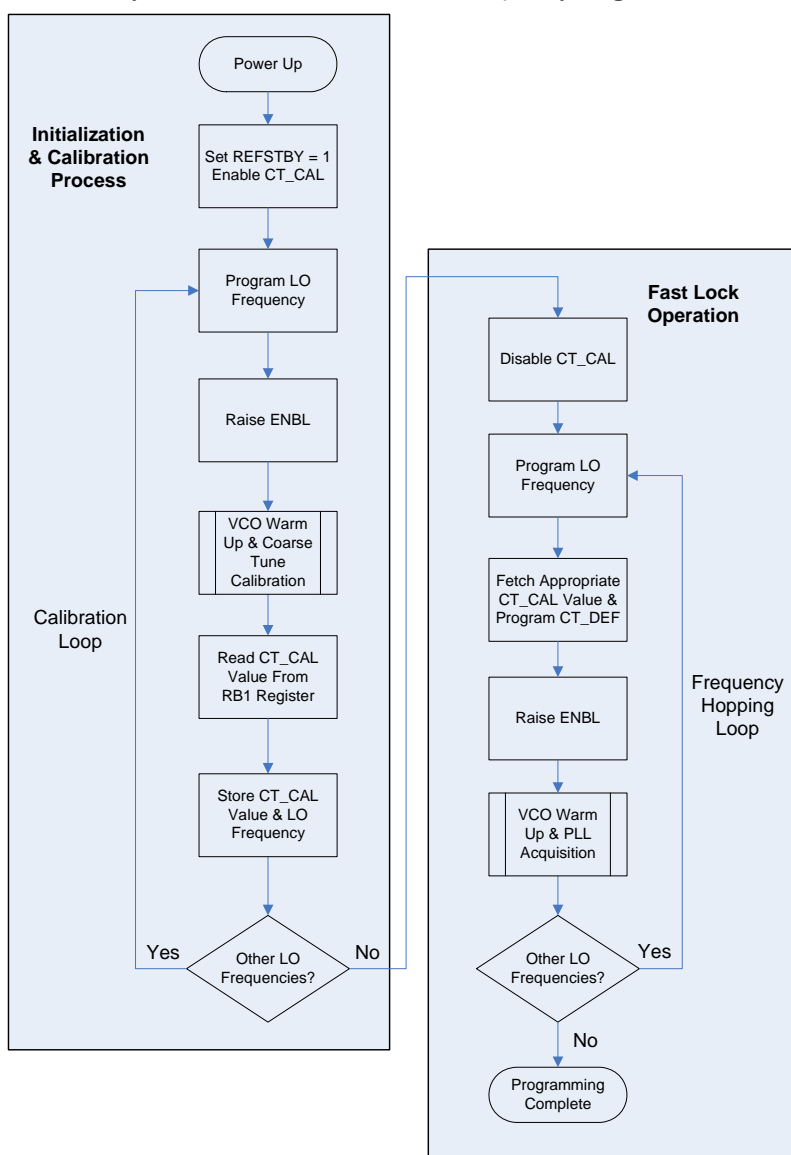

Figure 7. Flow Diagram of Calibration Process and Fast Lock Operation

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RF205X Synthesizer Lock Time Tests

Measurements were performed on an RF2052 evaluation board, using the standard loop filter configuration and 26 MHz crystal and phase detector frequency. An LO frequency of 915 MHz was chosen, 1830 MHz on VCO2 with an LO divide by two. An Agilent E5052B Signal Source Analyzer was used in Transient Analysis mode. The trigger was taken from the RF2052 ENBL line, via an oscilloscope to buffer the trigger signal into the analyzer. Note that there is a 100 KΩ series resistor on the ENBL line and a 33 pF capacitor, so the scope was probe was placed on the device side of the resistor to avoid inaccuracy due to the RC delay of several usecs.

The concern with this method is the delay time of the trigger through the oscilloscope and analyzer. This seems to be negligible as the analyzer results show the VCO power coming up in the expected time.
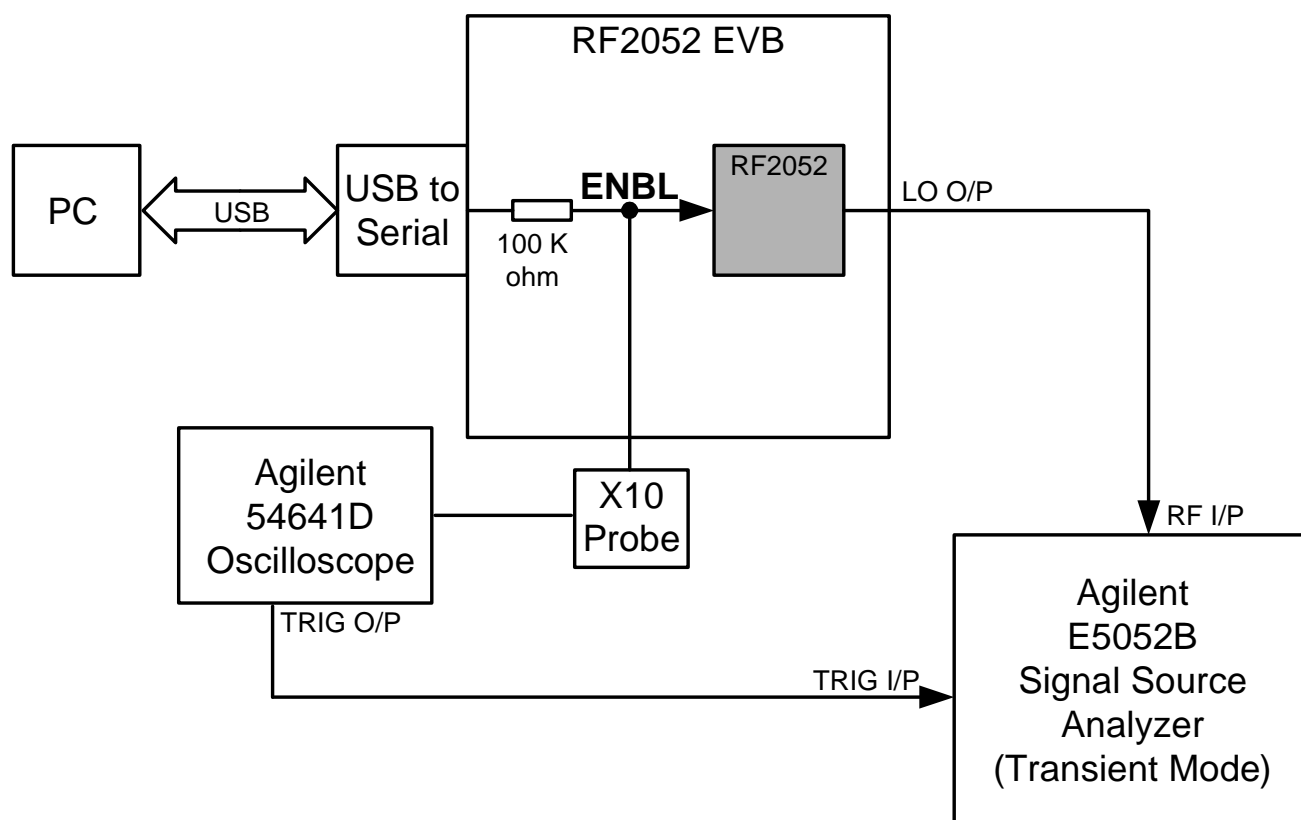

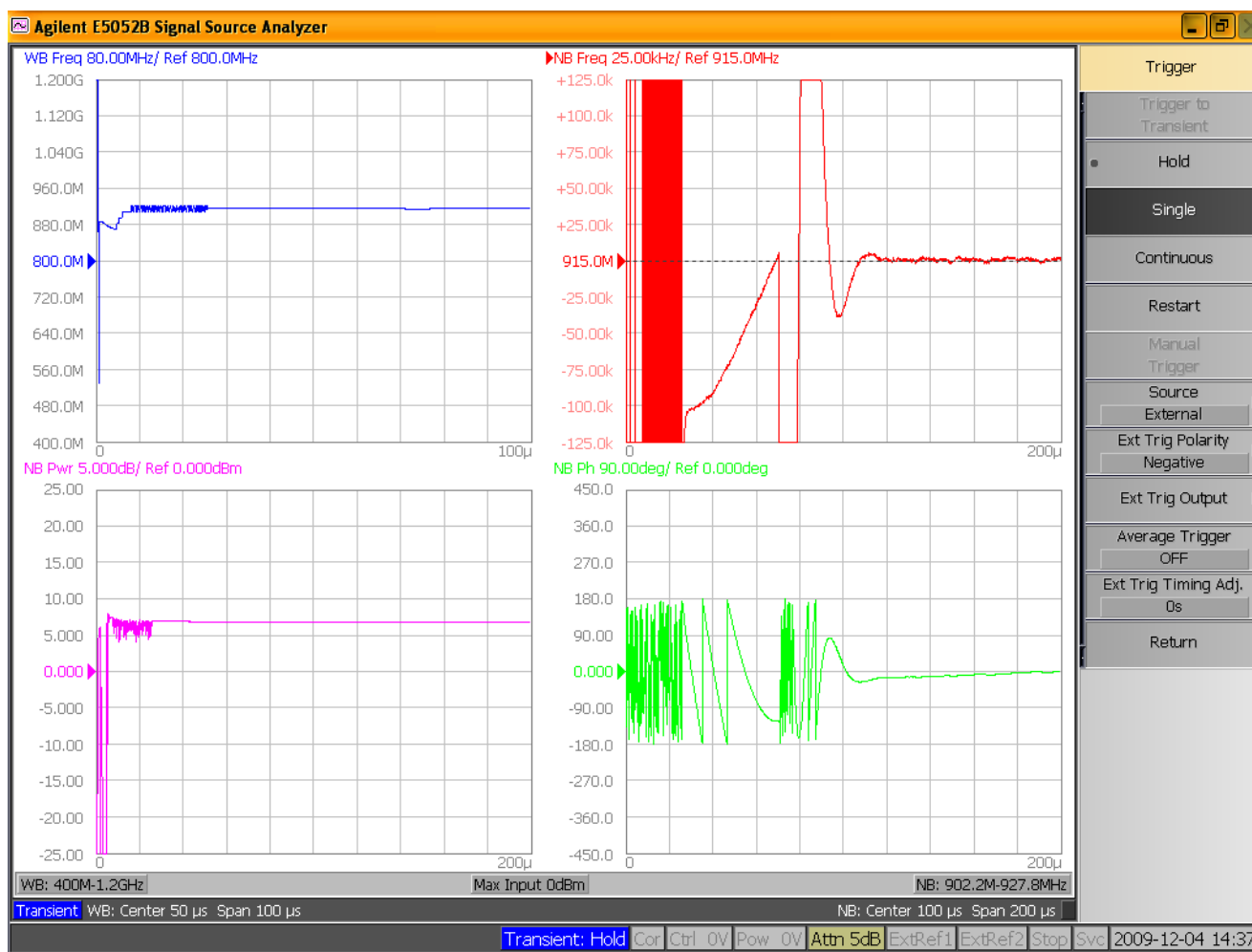Figure 8. Lock Time Test Set Up

RESULTS FOR DEFAULT SETTINGS

Default settings, with CT_CAL enabled and charge pump current P2_CP_DEF=011111.

On the plot below you can make out the VCO warm up and CT_CAL in the first 30usecs, then 40usecs for the KV_CAL timers to run, then finally about 50usecs as the PLL acquires lock and settles to the final frequency. The loop bandwidth is about 60KHz.

The total lock time is <120usecs for the PLL to settle within ±5KHz. See red trace.

Note the x-axis changes from 200usecs to 100usecs for the top left plot.

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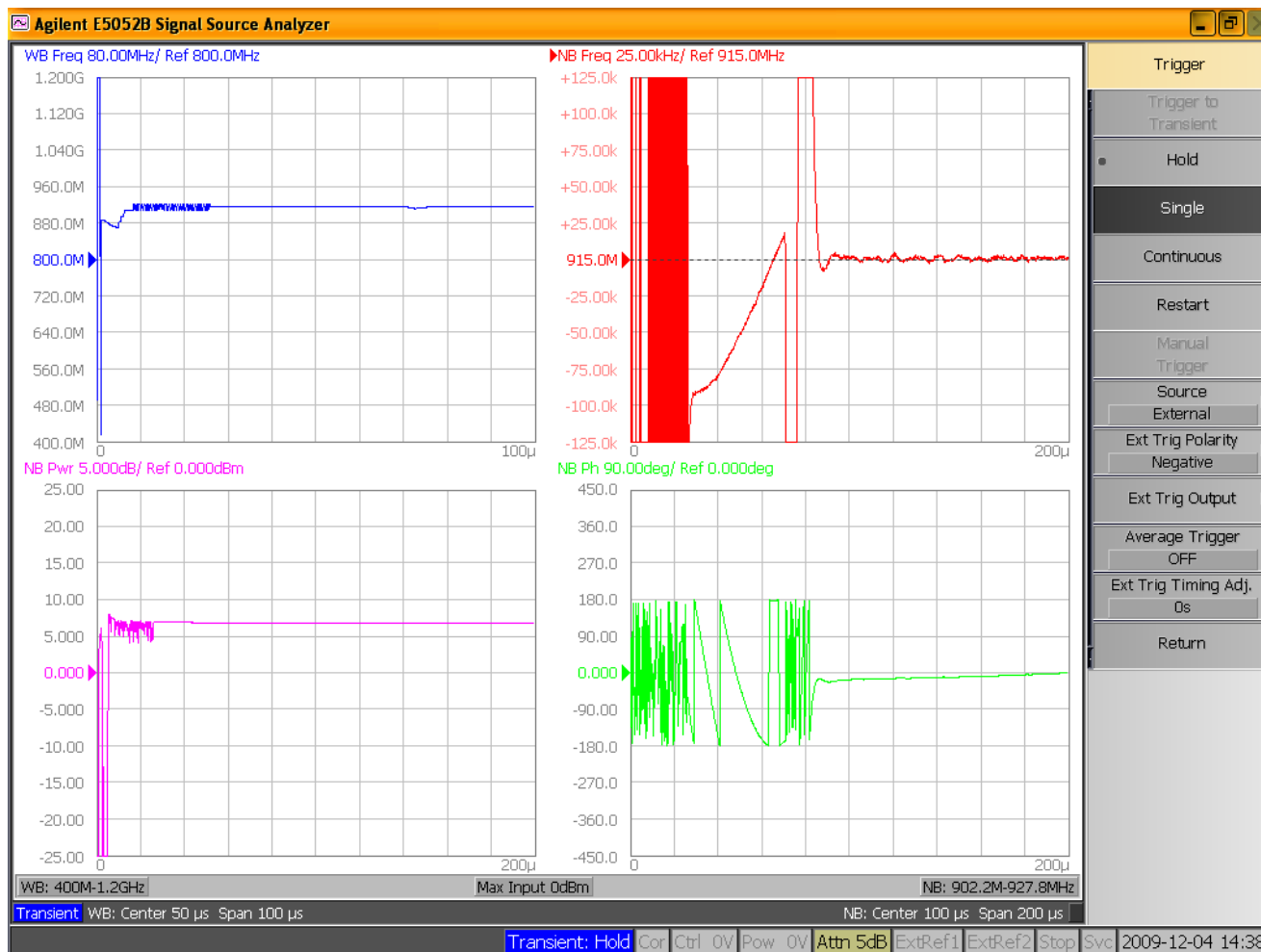
RESULTS FOR DEFAULT SETTINGS AND MAX CHARGE PUMP CURRENT
Default settings, with CT_CAL enabled and charge pump current increased to P2_CP_DEF=111111.

The charge pump current, and increase in bandwidth to about 110 KHz, speeds up the PLL settling time. The time until the start of PLL acquisition is unchanged, but the PLL settle time itself has been halved.

The total lock time is <95 usecs for the PLL to settle within ±5 KHz. See red trace.
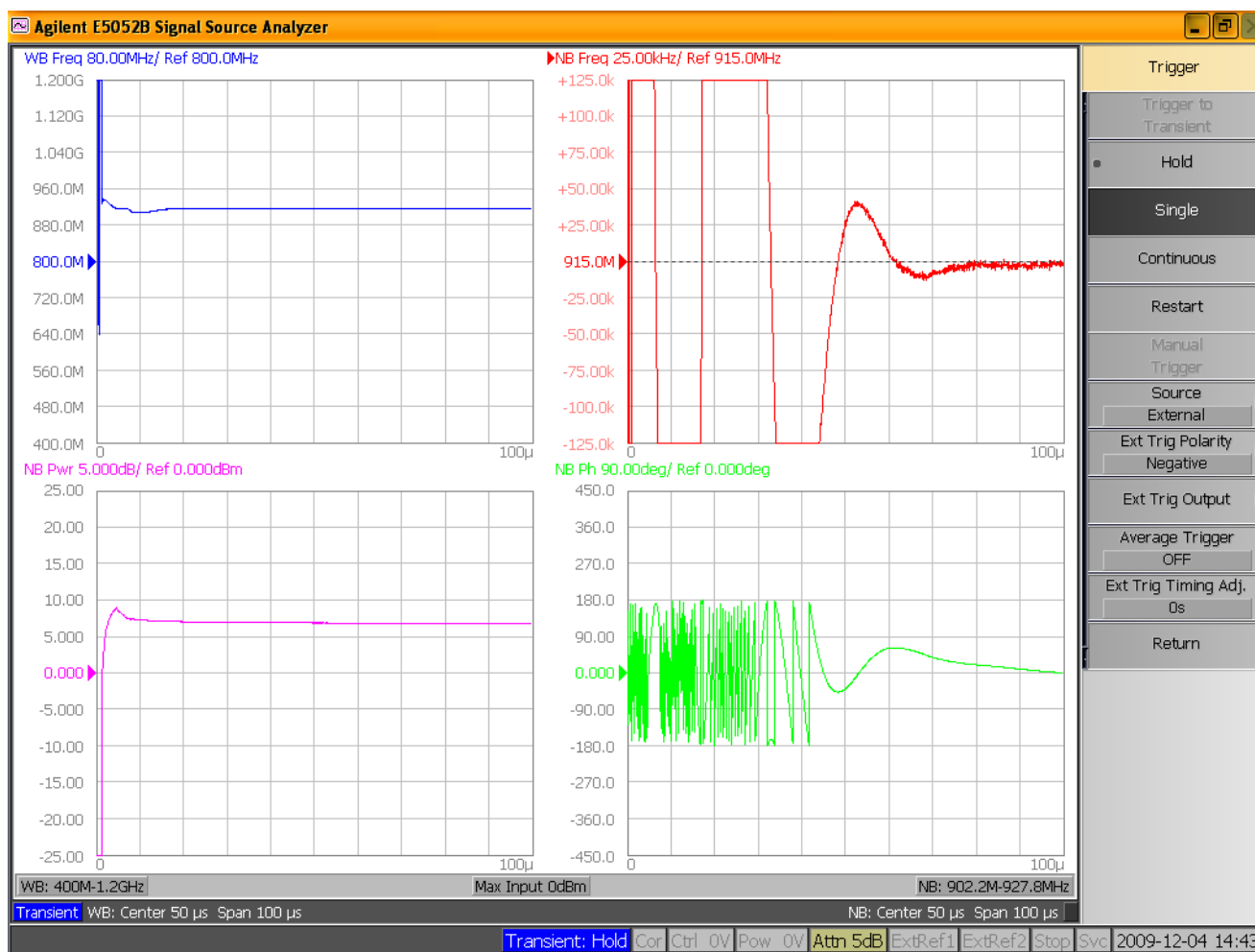
Note the x-axis changes from 200 usecs to 100 usecs for the top left plot.

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FAST LOCK SETTINGS

This plot is for the calibrations disabled and timers minimized. Default charge pump current is used, P2_CP_DEF = 011111, CT_CAL = 1001101, and V_{TUNE} = 1.11V.
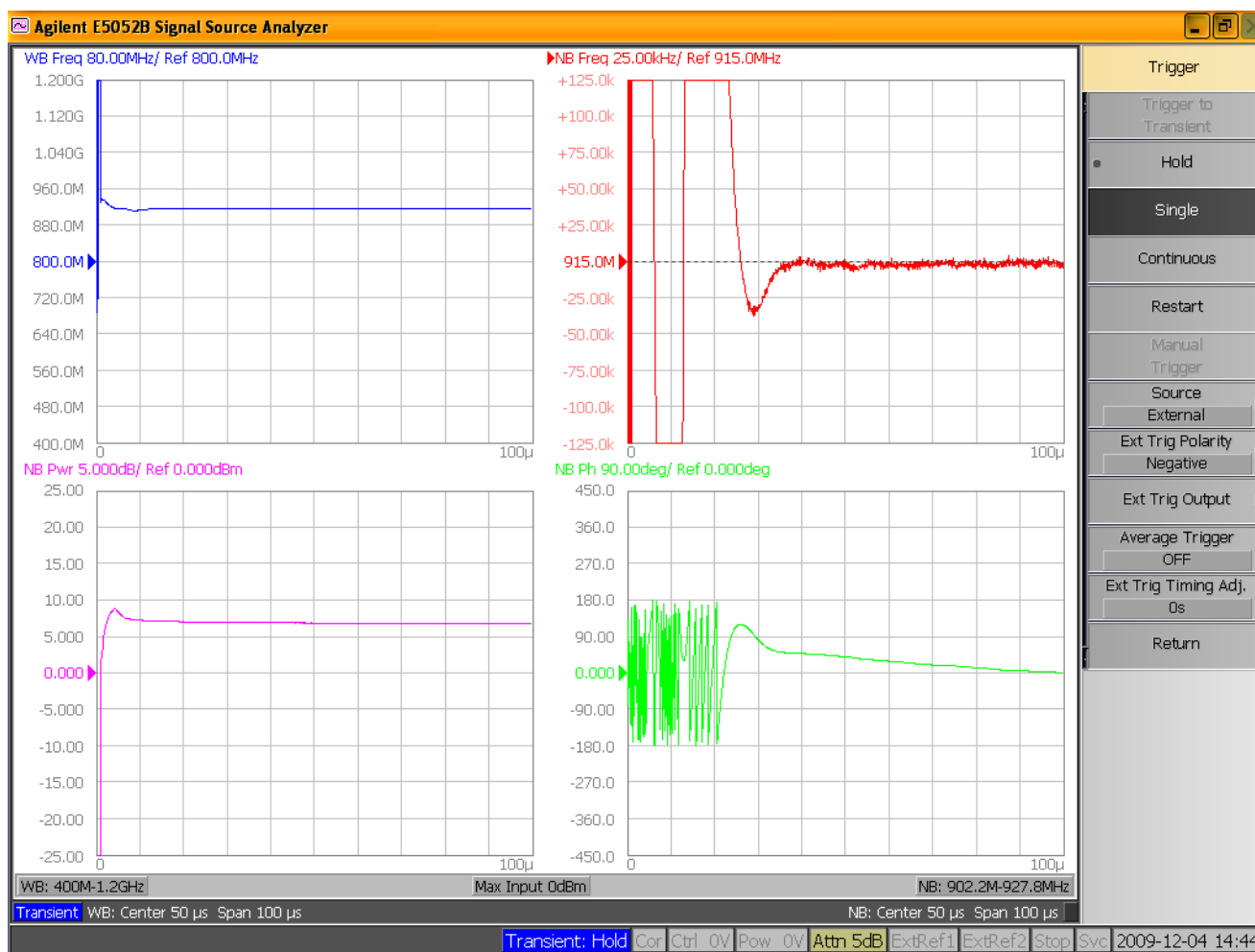
The total lock time is about 75usecs for the PLL to settle within ±5KHz. The majority of this is the PLL settling time, which starts after VCO warm up time of about 10usecs.

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FAST LOCK SETTINGS AND MAX CHARGE PUMP CURRENT

This plot is for the calibrations disabled and all timers minimized. Maximum charge pump current is used, P2_CP_DEF=111111, CT_CAL=1001101, and V_{TUNE}=1.11V.

The total lock time is 35usecs to 40usecs for the PLL to settle within ±5KHz. The increase in charge pump current and loop bandwidth has halved the PLL settling time.

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FAST LOCK SETTINGS AND LOWER TUNING VOLTAGE

This plot is for the calibrations disabled and timers minimized. Default charge pump current is used, P2_CP_DEF=011111, CT_CAL=1001110, and V_{TUNE}=0.82V. This lowers K_{VCO}.
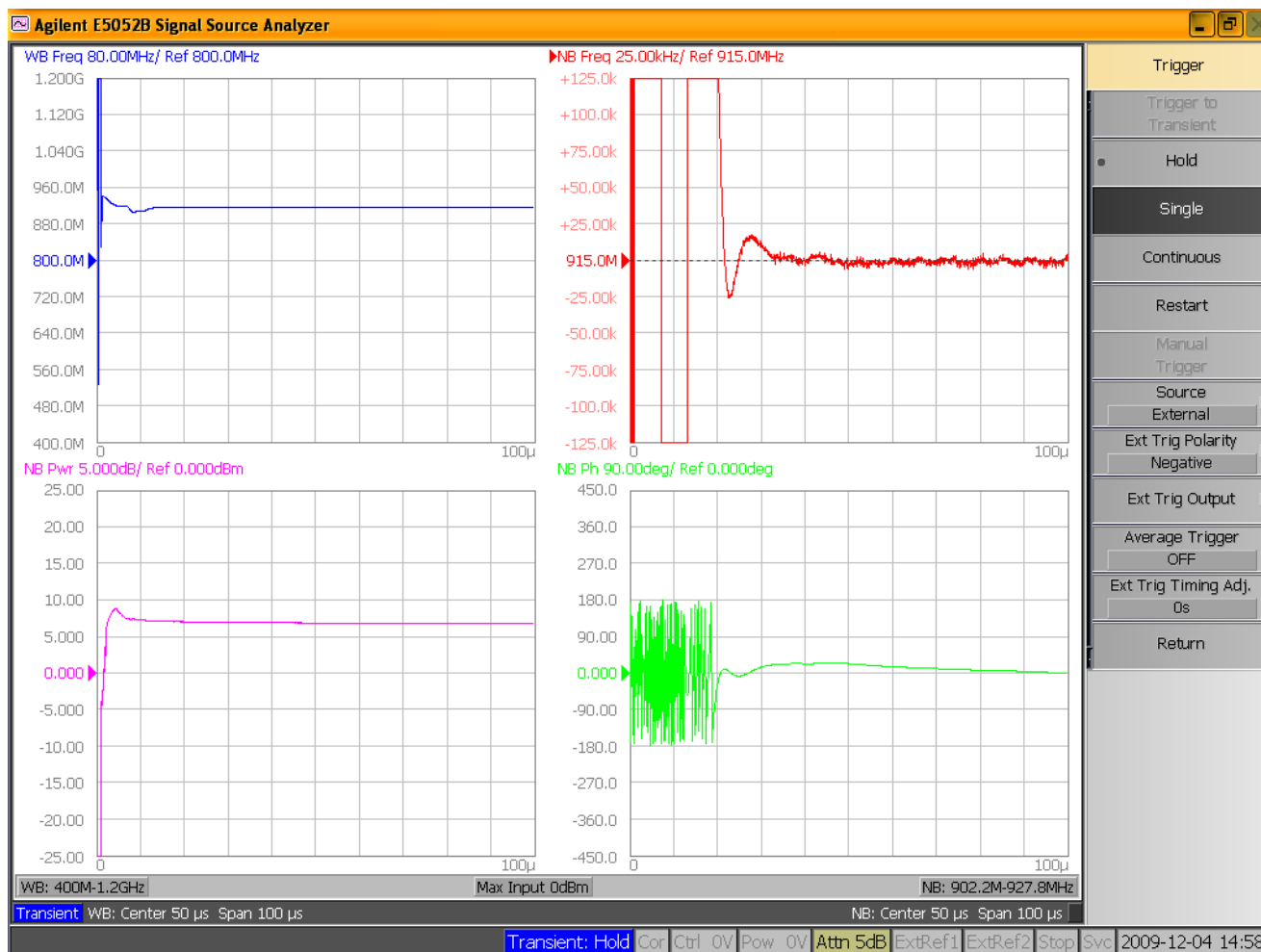
The total lock time is about 45usecs for the PLL to settle within ±5KHz.
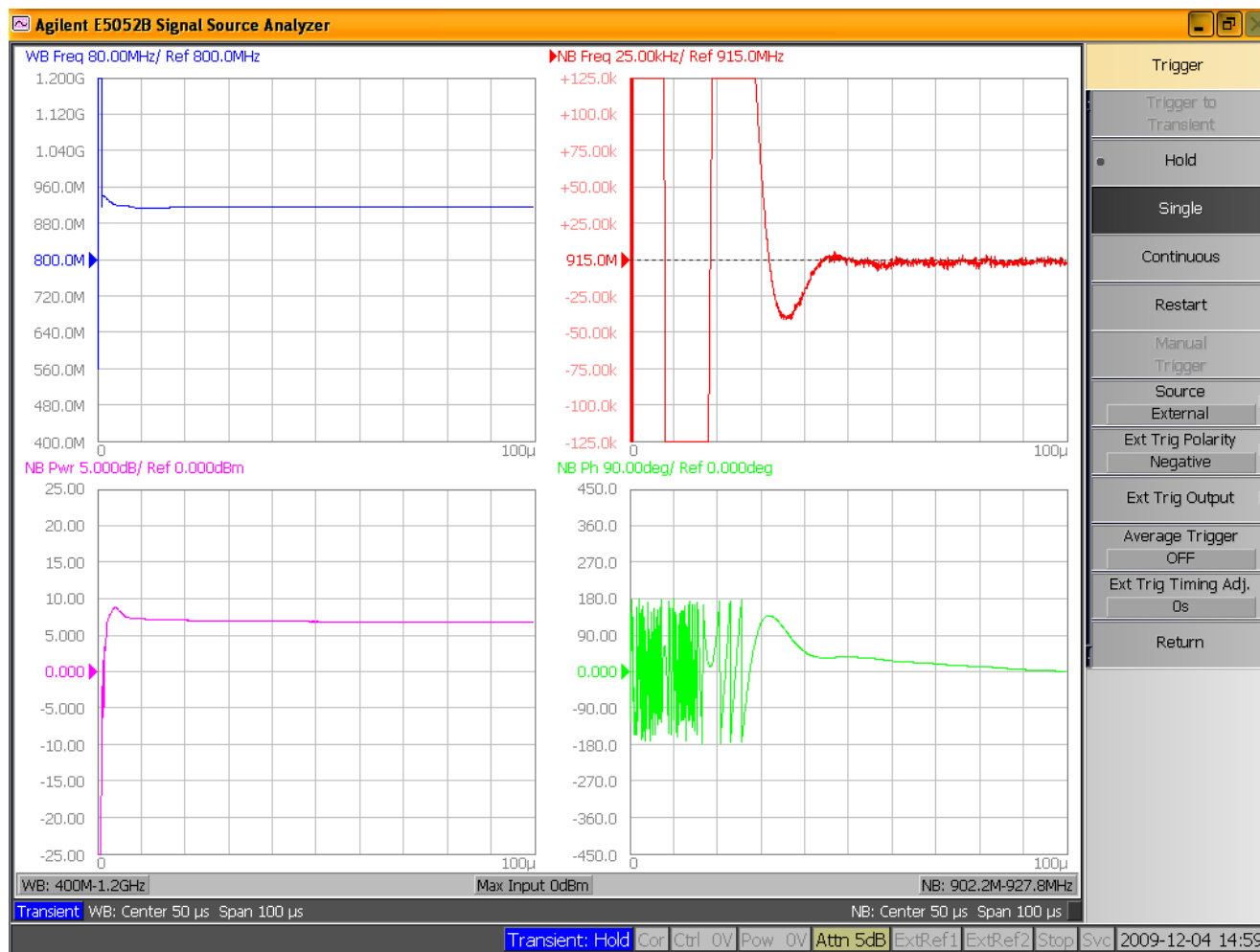
FAST LOCK SETTINGS, LOWER TUNING VOLTAGE, AND MAX CHARGE PUMP CURRENT

This plot is for the calibrations disabled and timers minimized. Maximum charge pump current is used, P2_CP_DEF = 111111, CT_CAL = 1001110, and V_{TUNE} = 0.82 V. This lowers K_{VCO}.

The total lock time is about 35 usecs for the PLL to settle within ±5 KHz.

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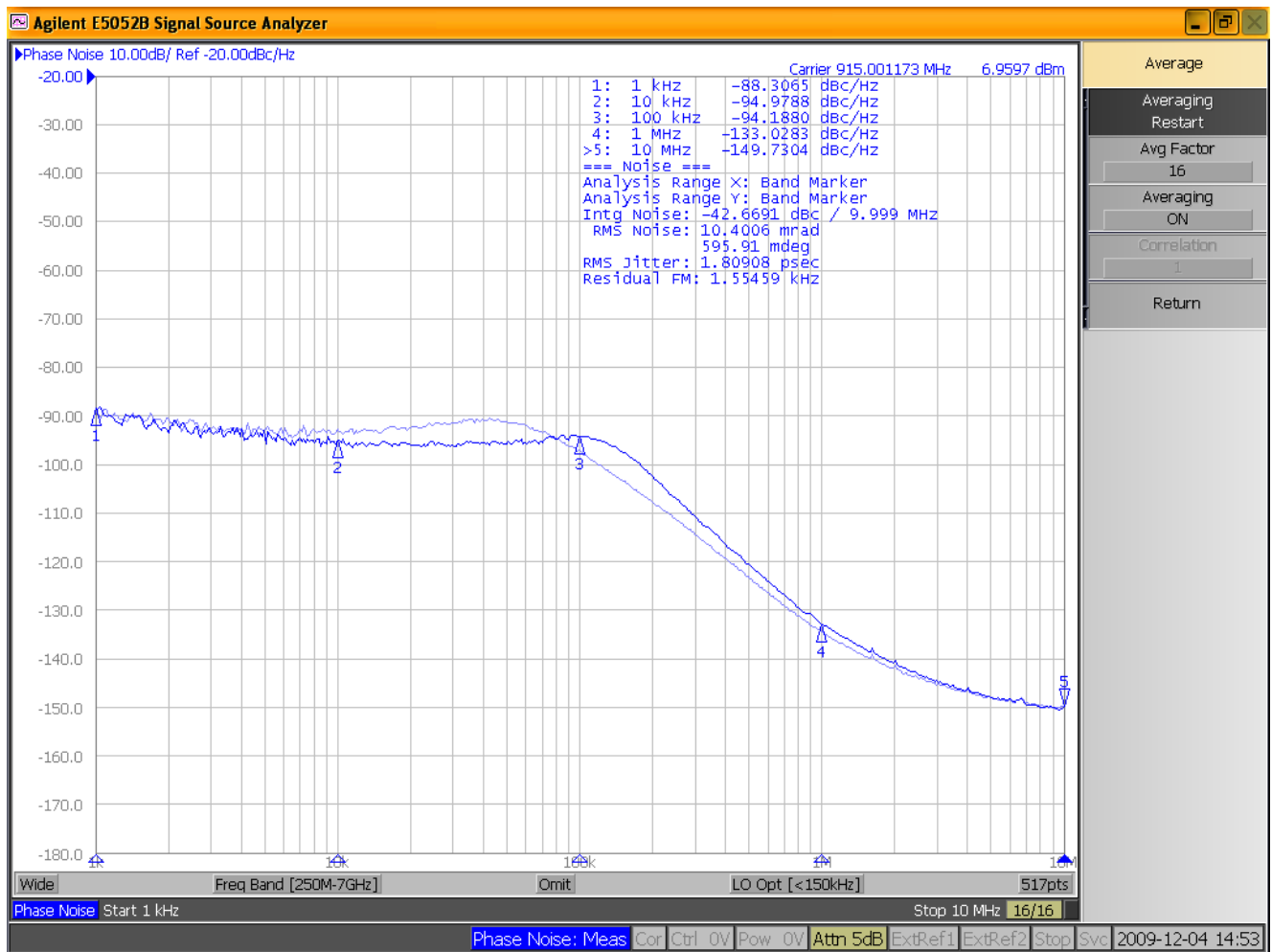
Effects On Synthesizer Phase Noise

The following plots show the effect of reducing lock time on loop bandwidth and phase noise. The plots correspond to the settings used in Synthesizer Lock Time Tests.

PHASE NOISE AT 915 MHz WITH V_{TUNE} = 1.11V

CT_CAL = 1001101 to give V_{TUNE} = 1.11V.

Icp = 011111 (saved trace) loop bandwidth about 70KHz.

Icp = 111111 (active trace) loop bandwidth about 140KHz.

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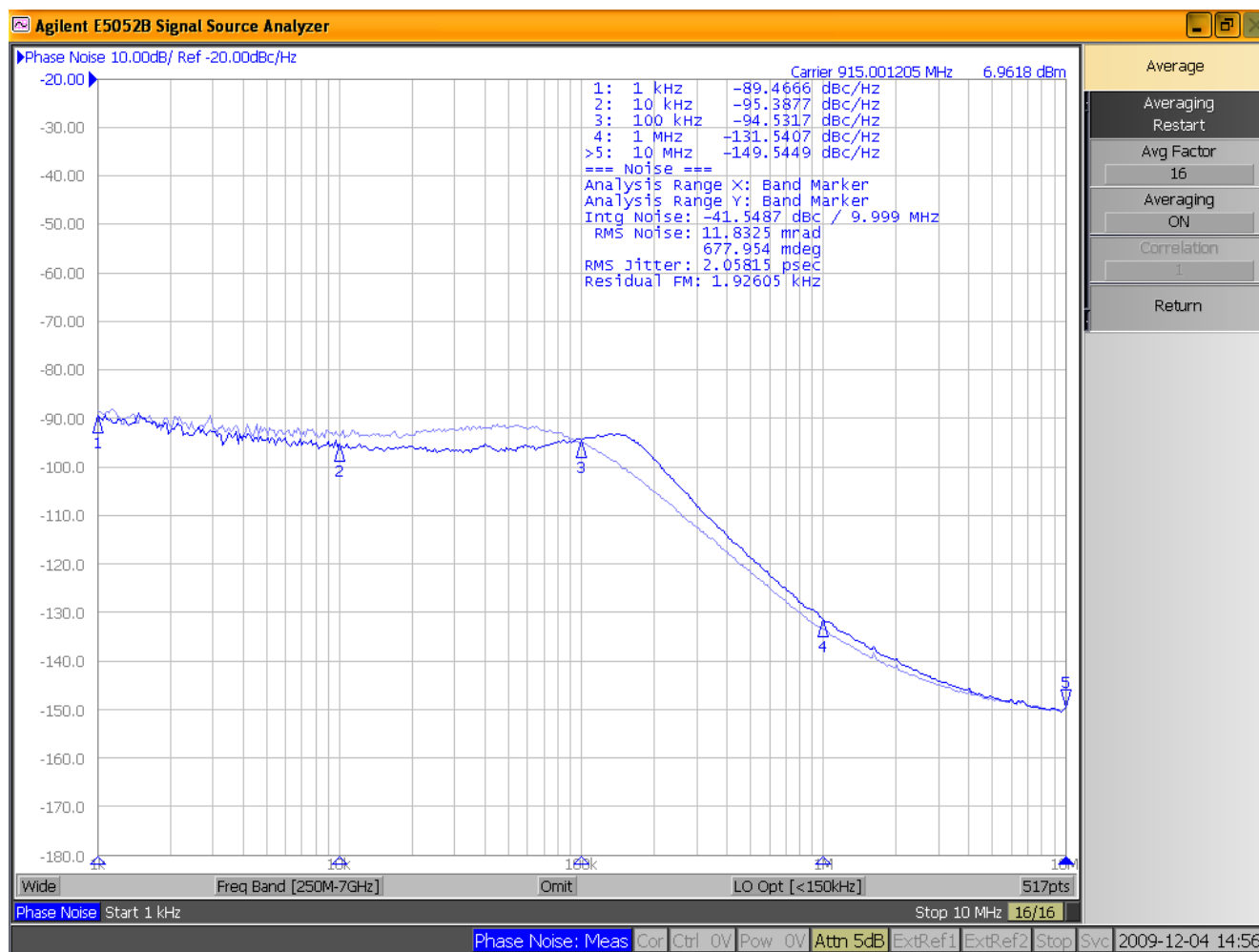
PHASE NOISE AT 915MHz WITH V_{TUNE}=0.82V

CT_CAL=1001110 to give V_{TUNE}=0.82V.

Icp=011111 (saved trace) loop bandwidth about 100KHz.

Icp=111111 (active trace) loop bandwidth about 200KHz.

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Conclusions

With the default register settings the typical time for the RF205x synthesizer to lock is of the order of 120 usecs. This assumes a 26 MHz phase detector frequency and 60 KHz loop bandwidth.

It has been shown that just by disabling the VCO coarse tune calibration, CT_CAL, and minimizing all of the calibration timers that this lock time can be reduced significantly, by about 45 usecs. This has no impact on loop bandwidth or phase noise. However the CT_CAL values for each device do need to be determined and programmed into the device for each LO frequency.

Pushing out the loop bandwidth by increasing charge pump current to maximum gives further reduction of the PLL settling time. This actually improves the rms integrated phase noise, although the phase noise at 100 KHz offset is slightly higher. This gives lock time of 40 usecs, from ENBL going high to the VCO frequency settling to within ±5 kHz of the final value. Another 5 usecs to 10 usecs reduction was obtained by adjusting the CT_CAL value, and hence the tuning voltage and K_{VCO}. This gave loop bandwidth of about 200 KHz with the same loop filter components.

So without significant impact on phase noise the lock time can be reduced from around 120 usecs to 35 usecs. If the loop bandwidth is widened the lock time can be reduced further, to around 20 usecs, but with the cost of increased degradation of phase noise.

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