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RF205x Family Frequently Asked Questions

RFMD Multi-Market Products Group

Overview

The RF205x family is a series of components integrating several RF functions; a single or dual wideband mixer, and local oscillator generation. The devices are wideband and flexible, making them suitable for use in a wide range of RF applications. The device settings and configuration can be changed to enhance performance for a particular application.

This document lists some frequently asked questions, providing answers that will hopefully enable new users to evaluate and design quickly and efficiently with the RF205x devices.

Frequently Asked Questions

Synthesizer

References: RF205x Frequency Synthesizer User Guide & RF205x Calibration User Guide

- How do I optimize the phase noise performance?

  Set charge pump leakage setting CPL=01. This lowers close in phase noise by about 2dB.

  Increase charge pump current. This also lowers close in phase noise, and widens the loop bandwidth.

  Use a higher phase detector frequency to minimize N and noise multiplication in the PLL, 20log10N.

  Select the VCO that's at the low end of the tuning range, where possible. For example at 2GHz you could use VCO1 or VCO2, but VCO1 has lower phase noise at this frequency.

  Set LDO_BYP=1. This will improve the VCO phase noise, as long as the power supply is from a low noise source.

  A passive loop filter gives slightly lower phase noise at around 100kHz offset, since there is no noise contribution from the op-amp used in the active loop filter. Plots in the data sheet demonstrate this. You do need to be more careful about VCO coarse tune calibration though, see questions below on CT_CAL for further details.

- How do I access the LO signal?

  If one of the mixer input pins is connected to DC ground then the mixer becomes unbalanced and the LO signal is routed to the mixer output. The level will be around +3dBm ±3dB.

- What level will the fractional N spurs be?

  The fractional N divider is controlled by a sequence generator, a form of sigma delta modulator known as a MASH. This effectively takes the spurs seen on a traditional fractional N synthesizer caused by the N/N+1 switching and pushes them outside the loop bandwidth as random noise. So the fractional divider does not put spurs on the LO as such, but a small noise contribution at 100kHz to 1MHz offset which is attenuated by the loop filter, typically 60kHz loop bandwidth.

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- What does the CT_CAL do?

  The VCO coarse tuning or VCO band selection basically switches capacitors into the VCO resonator until it is centered at the required frequency. This calibration is enabled by default, and is performed after the ENBL pin is taken high. After the calibration the PLL locking begins. The coarse tuning calibration can be disabled, for example to speed up lock time, but the value of CT_CAL word for the required VCO frequency needs to be written to the device.

- What does the Kv cal do?

  The loop filter or Kv calibration is disabled by default, and is not required in the majority of applications. This calibration varies the charge pump current to compensate for changes in KVCO (MHz/V) and N with different LO frequencies. It is only necessary in applications where the VCO is tuned over a wide frequency range and the loop response needs to be tightly controlled.

- What is the PLL locking time?

  This depends on what calibrations are enabled, the clock (phase detector) frequency, and the loop bandwidth. Different applications will also have different definitions of the locking time. Typically with a 26MHz clock, 60kHz loop bandwidth, and CT_CAL enabled the lock time will be approximately 120usecs after ENBL is taken high. If CT_CAL is disabled, then the typical lock time will be reduced to approximately 70usecs. The lock time can be reduced further by widening the loop bandwidth, but this will have an effect on phase noise.

- What if I change to a different reference frequency?

  The reference frequency, or more precisely the phase detector frequency after the reference divider, will affect the phase noise within the loop bandwidth. It sets the divider value N and the amount of noise multiplication in the loop. So with a lower phase detector frequency the phase noise will be higher. This follows 20log10N, except for higher frequencies above 40MHz where the synthesizer noise floor increases. For example increasing from 26MHz to 52MHz will decrease the phase noise at 10kHz offset by only about 2dB, not 6dB. The phase detector frequency is also used as the clock for the synthesizer calibrations, so will also affect lock time. A lower clock frequency will increase the lock time.

- Can I run the VCO's higher or lower than the data sheet suggests?

  The VCO frequency ranges specified in the data sheet are conservative to allow margin for process, assembly and temperature variations. They are the guaranteed frequency ranges. The VCO's may operate outside of these ranges, for example it may be possible to lock VCO1 at 2600MHz. The specified frequency ranges given are also for optimum phase noise and tuning gain, Kvco.

  It is possible to tune VCO3 outside of the normal guaranteed frequency range of 1200MHz to 1600MHz, by changing the external inductors. The maximum possible frequency will be when the pins are directly shorted to ground, so the resonator inductance is about 0.5nH on each pin from the inductance of the device bond wires. For lower VCO frequencies lumped high Q inductors could be used. Again the performance of VCO3 is not guaranteed outside of the specified frequency range. For applications requiring LO frequencies below 300MHz we recommend using the RF2056. The RF2056 uses external inductors on the VCO resonator, and is specified to operate from 50MHz to 500MHz LO. This is dependent on the value of external inductors used on the VCO, and the LO divider setting.

- Can I use the RF2053 with the on-chip loop filter op-amp?

  The integrated op-amp on the RF2053 can be used, but it is not recommended for two reasons. Firstly the op-amp output voltage range is only about +0.2V to +2.4V, which is not sufficient for the tuning range of most external VCO's. The other issue is that the noise performance of the op-amp is not low enough to give the full benefit of the low phase noise performance offered by an external VCO.

- Can I use the RF2051 with an external VCO?

  The RF2051 can be used with an external VCO, of frequency range 300MHz to 2400MHz, if the phase noise of the integrated VCO is not adequate for the application. An external low noise op-amp will also be required. The external VCO output needs to be fed into pins 2 and 3 of the RF2051, via a balun, normally the VCO3 external inductor pins. Then the register settings P1/P2_VCOSEL need to be set for VCO3, and the EXT_VCO bit set high in register CFG1. This is the same as for the operation of the RF2053.

- How does the lock detect circuitry work?

  When the ENBL pin is taken high, the VCO coarse tuning calibration (CT_CAL) adjusts the VCO switched capacitance until the VCO is centered on frequency and the VCO tuning voltage is around +1.1V. This is in the middle of the op-amp output voltage range of approximately +0.2V to +2.4V.

  The lock detect function is a window detector, indicating an out of lock condition when the VCO tuning voltage is outside of a certain voltage range. When out of lock then the LOCK bit will be high, bit 1 in the read back register RB1. It is possible that when an out of lock is indicated the PLL is still locked but the tuning voltage outside of the window.

  There are two windows for the lock detector:

  - LD_LEV = 0: 0.55V to 1.60V (narrow window)
  - LD_LEV = 1: 0.33V to 1.81V (wide window)

  The two lock detector windows can be useful to indicate how much the VCO is drifting, and when it will be necessary to perform another CT_CAL. If with LD_LEV=0 you get an out of lock state appear, this would probably indicate that the PLL is still locked, but the VCO and tuning voltage has drifted somewhat with temperature variation. If you get a lock indicated still with LD_LEV=1 then this would confirm this. At this point it would be advisable to perform a CT_CAL to re centre the VCO.

  If you get an out of lock indicated with both LD_LEV=0 and 1 then this would indicate that either there is no PLL lock, or you are dangerously close to the tuning range limits. So it would be necessary to perform a CT_CAL, by re-enabling the device.

  Note that the LOCK detect function will not work with the RF2053 and external VCO's. However a similar window detector could be used on the external VCO tuning line for example by using comparators.

- How do I tell that the CT_CAL has been successful?

  As well as the fact that the PLL has locked, the CT_CAL result is available in the read back register RB1. This can be useful for diagnostics since the expected CT_CAL word (0 to 127) for the programmed VCO frequency can be compared to the read back result. There is a plot of typical CT_CAL results versus VCO frequency in the RF205x Calibration User Guide.

- How often does CT_CAL need to be performed?

  In time switched applications this is not an issue as the VCO coarse tuning is performed every time one of the mixers is enabled. For applications where the device is always on, the question is raised of how often to perform the coarse tune calibration. Testing the RF205x devices over temperature has shown that the synthesizer will maintain lock over the full temperature range, with the same CT_CAL setting. This includes the worst case of performing the CT_CAL at one temperature extreme, then taking the device to the other extreme. It is recommended to perform the CT_CAL for every 30°C temperature change in order to maintain the loop response and maximize performance. This assumes the standard configuration with the active loop filter.

  For the case of using a passive loop filter then it is recommended to perform the CT_CAL for every 10°C temperature change. This is because the charge pump output voltage range is significantly less than that of the op-amp, so any change in tuning voltage due to VCO frequency drift needs to be minimized.

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- Which XTAL pin do I use for an external reference?

  The XTAL pins 10 and 11 are differential, so an external reference can be fed into either pin, ac coupled. The other pin just needs to be ac coupled to ground.

- What can I do if the LO signal is locked but slightly off frequency?

  It should be possible to minimize the LO frequency error by using the crystal tuning register settings. The crystal oscillator contains fixed and variable loading capacitors that can be used to tune the crystal. The amount of tuning possible will depend on the crystal specification.

Mixers

References: RF205x Baluns and Matching Application Note

- Why is the conversion gain I measure on the evaluation board at my application frequency less than what the data sheet suggests?

  The evaluation board has wideband transformers and has been designed to enable evaluation of the RF205x device across the full mixer bandwidth of 30MHz to 2500MHz. It has not been optimized for any specific frequency. The conversion gain will be lower at higher frequencies, especially for higher output frequencies where the mixer output capacitance rolls off the gain. The output balun used also has 3dB point at 1900MHz. The gain can easily be improved by using a shunt inductor to resonate with the output capacitance at the application frequency, and by switching to a higher frequency balun.

- What is Full Duplex mode?

  In Full Duplex mode both of the mixers are enabled at once, with the same LO frequency. The LO frequency will be set by the contents of register bank PLL1 if MODE pin is low, or PLL2 if MODE is high. The isolation between the mixers is better than 60dB.

- And what about normal/Half Duplex/Simplex mode?

  In this case only one mixer operates when the device is enabled; Mixer 1 when MODE pin is low and Mixer 2 when MODE pin is high. The LO frequencies for each mixer can be the same or different; set by PLL1 register bank for Mixer 1 and PLL2 register bank for Mixer 2. Now this is suitable for time switched applications, but it must be realized that when the MODE pin is switched the ENBL pin must be cycled to calibrate and lock the synthesizer. So the switching time between mixers will be set by the PLL locking time discussed above.

- How can I minimize the time taken to switch between mixers?

  For applications requiring fast switching between mixers and the same LO frequency, then Full Duplex mode can be used. The device is enabled in Full Duplex mode, and the mixers are switched by switching on and off the mixer DC supply via the output pins, typically sourced through the output balun.

- Can I use the mixers at higher or lower frequencies?

  The mixers will operate outside of the 30MHz to 2500MHz specified frequency range, they are basically very wideband devices, but the performance is not guaranteed.

- What baluns can I use with the RF205x mixers?

  The following are wideband transformer baluns recommended for use with the RF205x family mixers. The Mini-Circuits and RFMD parts are all pin compatible.

	Frequency Range	Ω Ratio	Mini-Circuits Part Number	RFMD Part Number
Mixer Input	5MHz to 3000MHz	1:1	TC1-1-13M[1]	RFXF9503
Mixer Output	10MHz to 1900MHz	4:1	TC4-19+ [1]	RFXF6553
	500MHz to 2500MHz	4:1	TC4-25+	RFXF8553
	2MHz to 500MHz	8:1	TC8-1+/TC8-1G2+	-

[1] These are the baluns fitted on the standard RF205x evaluation boards.

  As an alternative ceramic hybrid baluns can be used. These are mainly available in commercial frequency ranges such as cellular, WLAN, and Bluetooth.

- Can I use lumped element baluns on the mixer ports?

  Lumped element baluns can be used, but they may not give the best mixer performance. Typical lead/lag lumped baluns only give good amplitude balance at the center frequency over a narrow bandwidth. So outside of this range, common mode suppression will not be good. This could lead to high noise figure and larger levels of spurs such as LO leakage. This is particularly an issue on the mixer output.

- Can I run the mixer ports single ended?

  This is possible, but will decrease conversion gain. The mixers are double balanced, so require baluns on all ports in order to operate correctly. So running single-ended causes larger levels of spurs such as LO leakage at the mixer output, and degradation of noise figure and linearity.

- What is the effect of changing the mixer current setting?

  The mixer current setting (MIX1_IDD and MIX2_IDD) is important in that it sets the performance of the mixer. It allows the user to trade off linearity against noise figure and current consumption. Each setting steps the mixer current about 5mA. The following table summarizes some typical mixer performance parameters for the five possible current settings. Note that the highest two settings are not recommended as they increase current without improving performance.

Mixer Current Setting MIX_IDD	Mixer Bias Current (GUI Dashboard Tab)	Comments	Total Supply Current (Typ)	Noise Figure dB (Typ)	Input IP3 dBm (Typ)	Pin 1dB dBm (Typ)
000	10mA	Mixer Off	50mA	-	-	-
001	15mA	"Low Noise" Mode	55mA	9.5	+10.0	+2.0
010	20mA		60mA	10.0	+16.0	+7.0
011	25mA		65mA	10.5	+20.0	+9.5
100	30mA	Default Setting	70mA	11.0	+22.0	+11.0
101	35mA	Max Linearity Setting	75mA	11.5	+24.0	+12.0
110	40mA	Not Recommended	80mA	>12dB	-	-
111	45mA	Not Recommended	85mA	>12dB	-	-

  The mixer current setting will also affect the mixer input impedance, mainly the resistive part. The highest mixer current setting of 101 gives a typical resistance of 75Ω, dropping to about 130Ω with the lowest setting of 001.

Programming and Miscellaneous

- I programmed a new frequency and the PLL did not lock?

  Whenever a new LO frequency is programmed, or the MODE pin changed, then the ENBL pin must be cycled. When ENBL is taken high it activates the analog circuits, activates the synthesizer calibrations, and then initiates the PLL locking.

- Do I need 51kΩ on the Rext pin?

  This is the optimal value of resistor. It sets the bandgap reference voltage which biases most circuit blocks on the device. Changing the resistor value will affect the performance of the device.

- Do I need to connect ANA_DEC to ANA_VDD?

  It is recommended to connect ANA_DEC, pin 5, to the main analog supply. This pin was originally designed to be a decoupling point only, not requiring a supply, and the device will operate in this way. Pin 5 is directly connected to ANA_VDD on pin 22 via the supply tracks on chip, which can be relatively high in resistance. It is recommended to connect ANA_DEC to the analog supply, as on the evaluation board, to reduce the risk of any voltage drops on the supply tracks degrading performance.

- Where can I get the latest version of the RF205x Programming Tool

  Below is a link to the RF205x software download site. The FTDI USB drivers are also available here for downloading.

  https://stargate.rfmd.com/sites/RFSliceShare

  The log-in details for the site are as follows:

  - Username: RFSliceShare
  - Password: sL1cesHare!
  - Note: Case sensitive.

  Click on the folder "Software Downloads." This folder contains another folder "GUI Tool" where the RF205x programming tool downloads are stored. The files are compressed into zip files, which are again password protected.

  To unzip the software download file you will be asked for a password which is:

  - Password: RFSlice
  - Note:Case sensitive.

  Before installing a new version of the RF205x programming tool, remove older versions via the Control Panel / Add or Remove Programs facility.

  Run the setup.exe file which creates all the necessary folders and installs the software.

- Where do I find out more information on the USB to serial adaptor on the evaluation boards?

  The USB to serial adaptor on the RF205x evaluation boards is the UM232R sourced from FTDI. It is programmed with a configuration file at RFMD. The USB drivers from FTDI need to be installed prior to using the evaluation boards and programming tool.

  http://www.ftdichip.com/Products/EvaluationKits/UM232R.htm

- What is the difference between the LED indicators on the RF205x Programming Tool?

  The indicator on the top left of the GUI window beneath the RFMD logo checks the status of the USB to serial adaptor. When the adaptor is present the LED indicator is green and reads "BitBanger OK."

  The indicators at the bottom of the window are the PLL Lock Detect, LED green indicating lock, and the Data Interface Status. If the Data Interface Status LED is green it means that the RF205x device registers can be successfully written to and read from. If red it indicates a problem with the serial interface or the device.

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