APPLICATION NOTE

885128

2.4 GHz WLAN/BT LTE Co-Existence BAW Filter

High-performance, high power Bulk Acoustic Wave (BAW) band-pass filter, high rejection in the band-edge and adjacent LTE/TD-LTE bands.

Introduction

This application note purpose to help customers translate the layout and design guidelines for the 885128 Bulk Acoustic Wave (BAW) band-pass filter. The 885128 is a high-performance, high power BAW band-pass filter with extremely steep skirts, simultaneously exhibiting low loss in the WiFi band and high rejection in the band-edge and adjacent LTE /TD-LTE bands. The 885128 enables coexistence of WiFi and LTE signals within the same device or in close proximity to one another. Its unique power handling capability allows for implementation into high performance high power access points and small cell base stations. The 885128 uses common discrete filter packaging techniques to achieve the industry standard 1.1 x 0.9 x 0.50 mm footprint. For more detailed information, please refer to the 885128 datasheet.

Product Details

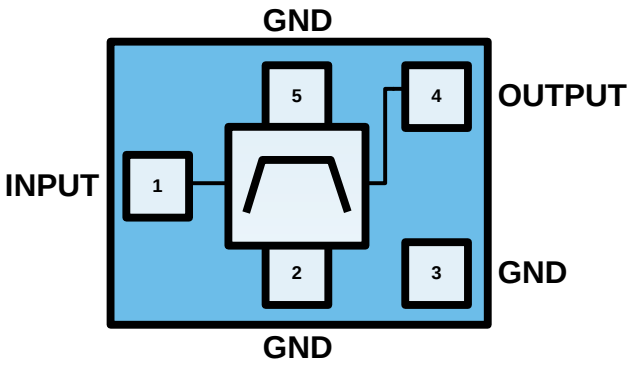


Figure 1. Functional Block Diagram & Pin-out Detail

Table 1. 885128 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1	INPUT	Transmit Port
4	OUTPUT	Antenna Port
2, 3, 5	GND	Ground

Evaluation Board Information

The Qorvo 885128 EVB is designed to provide performance representative of that obtainable in an actual application. The EVB is designed to operate with 50 Ω load impedances at all RF ports, which are provided with SMA connector interfaces. In order to minimize inductive coupling, the PCB was designed so that the matching inductors are mounted at 90 degrees to one another. Only a single shunt inductor is applied as a tuning component between the BAW filter's RF input and RF output pins and the EVB SMA connectors.

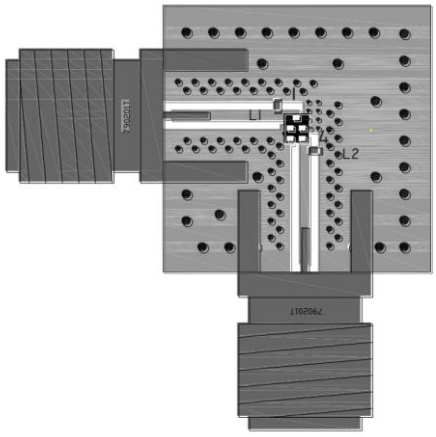


Figure 2a. 885128 Evaluation Board Image

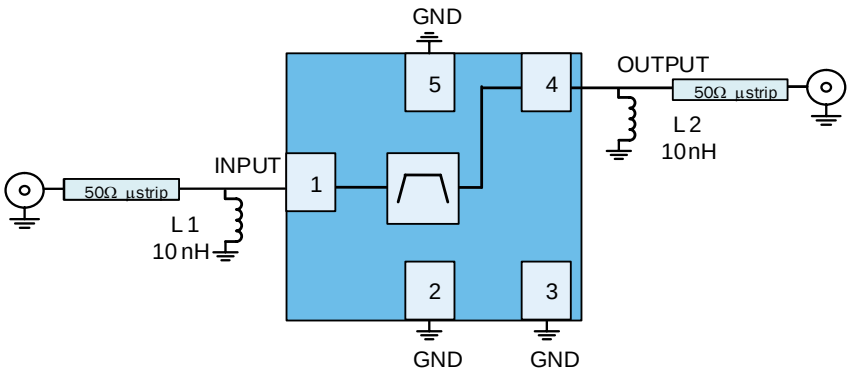


Figure 2b. 885128 Evaluation Board Schematic

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Layer	Copper	0.70mil		
3	Dielectric1	Taconic TLY-5A	7.50mil	2.17	
4	Layer 2	Copper	0.70mil		
5	Dielectric 3	FR4	53.00mil	4.2	
6	Bottom Layer	Copper	0.70mil		

Total Thickness: 62mils +/- 4mils

Figure 2c. 885128-PCB Stack-up

REFERENCE DESIGNATOR	VALUE	DESCRIPTION	MANUFACTURE	PART NUMBER
U1	-	885128 BAW Filter	Qorvo	885128
L1, L2	10 nH	0201, Chip Inductor, ± 3%	Murata	LQP03TN10NH02D

Table 2. 885128 Evaluation Board Bill of Materials

System Architecture Application Circuit Recommendations

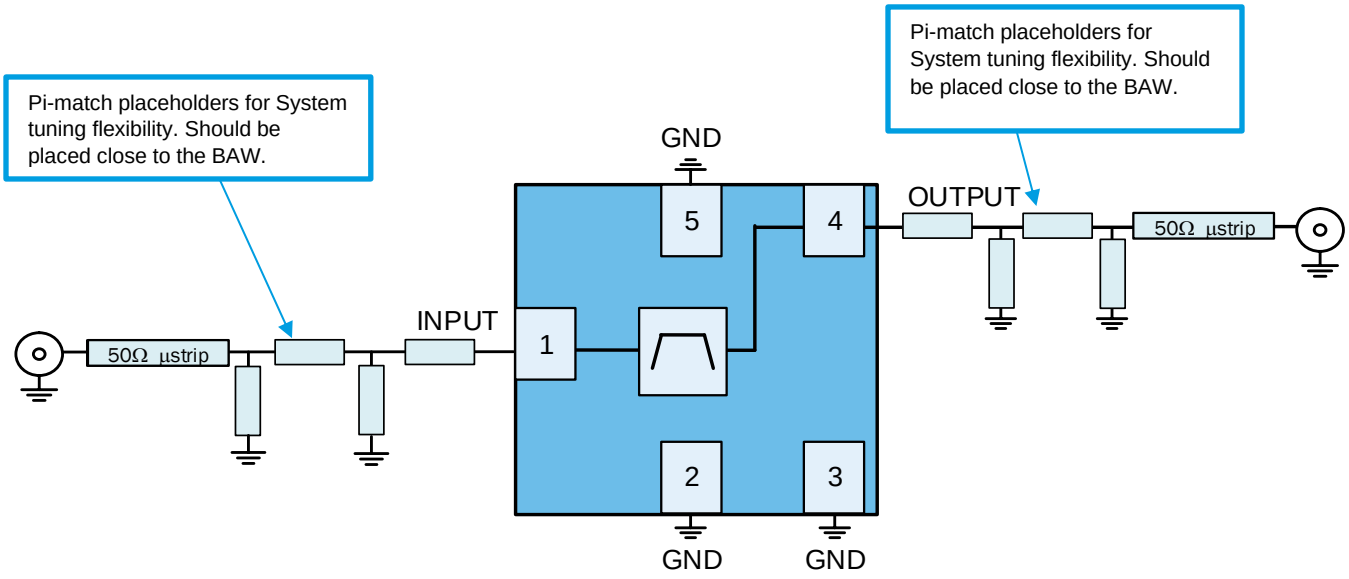


Figure 3. Recommended Application Circuit in a System.

1. The above schematic shows recommended Pi-network match placeholders for System tuning flexibility based on the 885128 EVB. The customer should ensure that sufficient Pi-matching is provided based on their PCB layout.

2. It is recommended to place a ground via next to each GND pin of the BAW and to add ground vias around RF traces. I.e, each ground pin should have their own ground via.

3. We recommend following Qorvo evaluation board layout guidelines as close as possible. The 885128 evaluation board uses 8 mil GND vias with 18 mil pads under the BAW. Gerber files are available upon request.

4. It is recommended to not have a connecting ground trace between ground pins 2 and 5 as illustrated in **Figure 4b** because of most manufacturing restrictions.

PCB Layout Considerations

Board layout must be carefully considered to achieve optimal performance from any BAW filter, including the 885128. In addition to providing connectivity between the BAW and external components, the PCB layout is a part of the overall circuit. The RF and DC parasitic of the traces, along with coupling between traces, must be evaluated. The 885128 Evaluation Board PCB layout guidelines provide a good starting point for designing the layout in the actual application.

RF Traces

All PCB traces between the RF pins and matching networks (where applicable) should be 50 Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. The RF traces should be routed on the top layer to minimize coupling with other RF, control input, and DC traces present on the PCB. If it is not possible for some reason to route RF traces on the top layer, we suggest that you make sure there is proper isolation between traces on the layout to avoid any coupling issues. RF lines should be isolated from other RF and DC signals by adding solid ground planes (with vias) between them to minimize coupling and cross-talking. In addition, we also recommend reducing RF trace lengths, wherever possible.

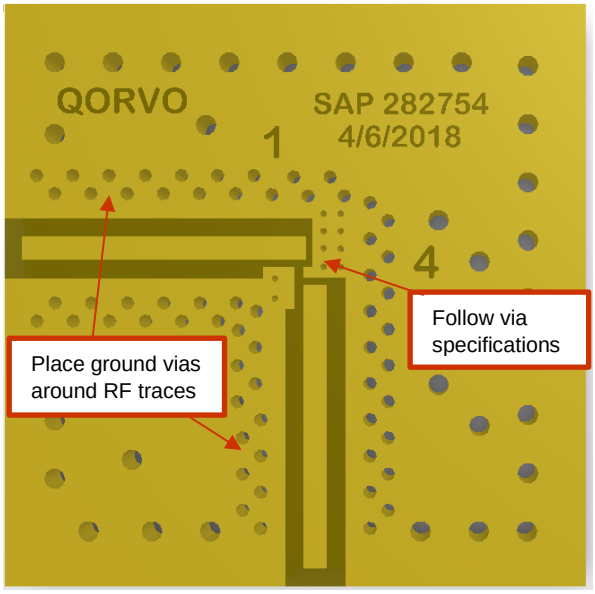


Figure 4a. Recommended PCB layout Considerations.

Grounding Considerations

Grounding of BAW GND pins - The ground pins serve as the primary RF ground reference for the entire BAW. Connect the BAW filter ground pins directly to the main ground plane layer of the PCB. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible. This ground layer also provides the reference layer for microstrip lines.

Reference Plane - A larger number of via holes should be distributed over the entire area below/around the BAW to provide good RF ground reference ground plane, as shown in Figure 4b below. Alternately, it is recommended to place a ground via close and next to each GND pin of the BAW to avoid a ground loop. Each ground pin should have their own ground via The 885128 EVB uses GND vias with an 18mil diameter and 8mil hole size under the BAW.

GND Vias for Thermal Considerations – The BAW GND pins serve as the primary path for heat removal, additionally, the PCB ground vias will serve as a low resistance thermal path between the BAW and the PCB. Vias passing through multiple copper layers provide the best overall RF and thermal performance. The 885128 ground pins have special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduct path for heat dissipation. The GND pad and vias pattern and size used on the Qorvo evaluation board should be replicated. The Qorvo layout files in Gerber format can be provided upon request.

DC Layout Considerations

All DC traces routed near the BAW must be isolated with a GND inbetween the BAW and the DC trace. The GND should have vias on them which route from the top layer through to the bottom GND layer. Where possible, power planes should be used to route DC traces which support high current supplies. It is recommended to avoid routing traces underneath the BAW.

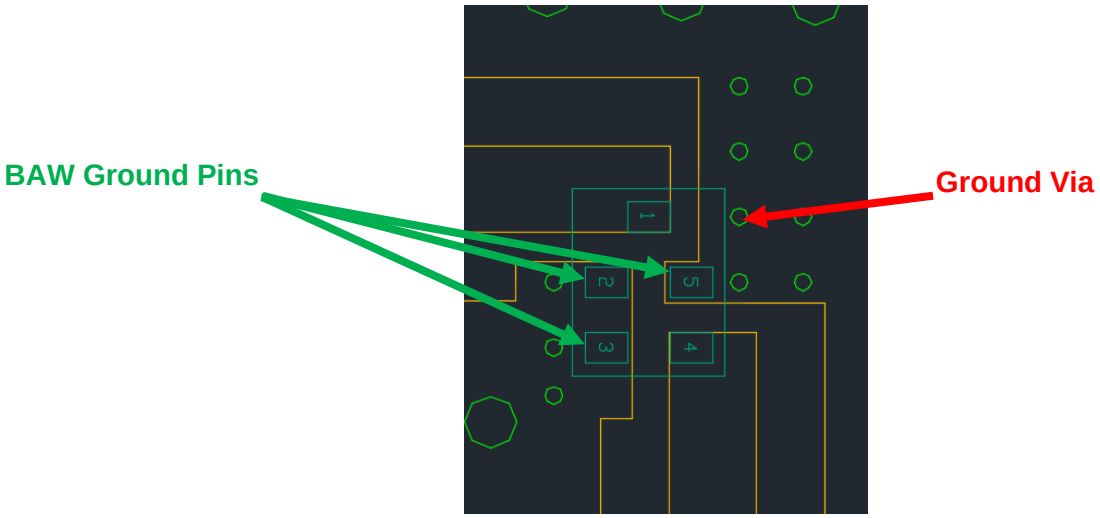
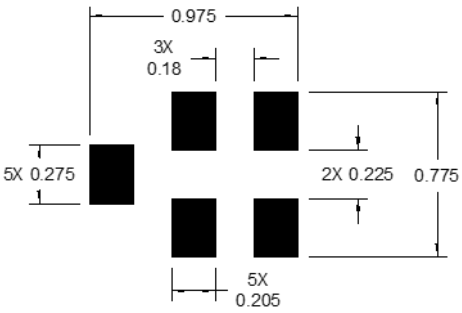


Figure 4b. Recommended Ground Via Placement.

PCB Footprint Recommendations

See **Figures 5a and 5b** below for the recommended package outline drawing and solder mask patterns.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo evaluation board for this product. Some modification may be necessary to suit end user assembly materials and processes.

Figure 5a. PCB Footprint Recommended Solder Mask Pattern.

Package Information

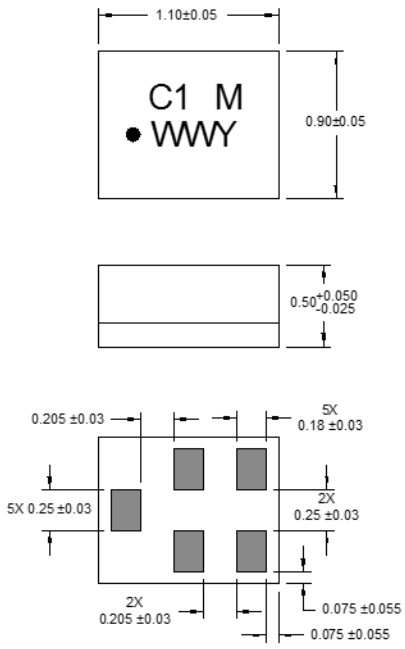


Figure 5b. 885128 Package Outline Drawing.

Package Style: ULC1109A

Dimensions: 1.1 x 0.9 x 0.50 mm

Package for Surface Mount Technology

Terminations: Au plating 0.5 - 1.0 µm, over a 2-6 µm Ni

Plating

Approximate weight 3.96 mg

All dimensions shown are nominal in millimeters.

Unless otherwise specified all tolerances are ±0.05mm except length and width that are specified as ± 0.1mm

The Marking Code is correlated with the Part Number

M=Manufacturing Site Code (Blank for Apopka, C for Costa Rica)

The Date Code consists of:

WW = 2 digit week

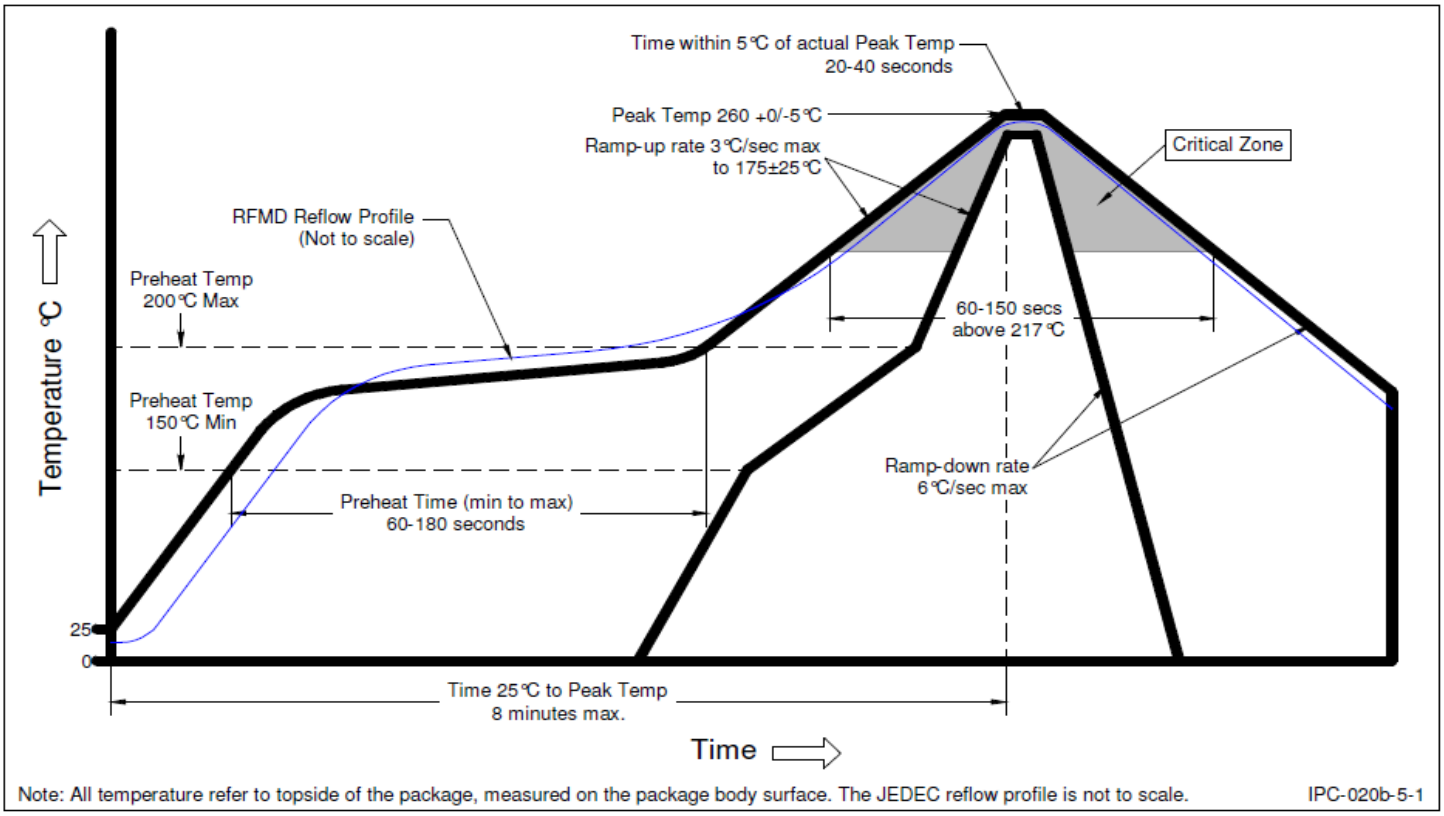
Y=The last digit of the year

Notes:

1. All dimensions shown are typical in millimeters.
2. An asterisk (*) in front of the marking code indicates prototype.

Reflow Profile & Solder Paste

Figure 6a illustrates the recommended reflow profile for the 885128.



CONDITIONS	
Ramp-up rate	3 ºC/second max.
Preheat temperature 175 (±25) ºC	180 seconds max.
Temperature maintained above 217 ºC	60 seconds to 150 seconds
Time within 5 ºC of actual peak temperature	20 seconds to 40 seconds
Peak temperature range	260+0/-5 ºC
Ramp-down rate	6 ºC/second max.
Time 25 ºC to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤ 3
Pre-baking requirements	Refer to JEDEC J-STD-033 if original device package is unsealed
Maximum reflow temperature	260 ºC

Figure 6a. Recommended Reflow Profile & Conditions

Maximum reflow temperature is 260°C. The temperature used to classify the MSL level appears on the MSL label on each shipping bag. Qorvo uses reflow profiles in accordance with IPC/JEDEC J-STD-020 for qualification except for the maximum reflow temperature of 260 °C.

Solder paste used for the Qorvo high temperature reflow qualification.

SPECIFICATIONS	
Solder paste	Multicore 96SCAGS89 (CR39)
Alloy type	Sn95.5/Ag3.8/Cu0.7
Metal content	88.5%
Solder particle size	45 µm to 20 µm

Figure 6b. Solder Paste Specifications.

Support Data

For any further data on the 885128, please request Qorvo point of contact such as marketing, sales or a representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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