APPLICATION NOTE

QPF4519 FRONT-END MODULE

5 GHz WLAN FEM (11a/n/ac)

Multiple functions in a single package — reducing design complexity, shrinking PCB footprints, maximizing performance

Introduction

This application note explains the powering sequence for the QPF4519 evaluation board and recommended system application circuit. The QPF4519 is an integrated front-end module (FEM) designed for Wi-Fi 802.11a/n/ac systems. It provides <1.8% dynamic EVM at +23 dBm output power using MCS9VHT80 (11ac) waveform while drawing 280 mA current at +5.0 V_{CC}. This FEM is a 50-ohm part and is housed in a 5.0 mm x 3.0 mm laminate package and has integrated die-level filtering for 2nd and 3rd harmonics as well 2.4 GHz rejection for DBDC operation.

For more detailed information, please refer to the QPF4519 datasheet.

Product Details

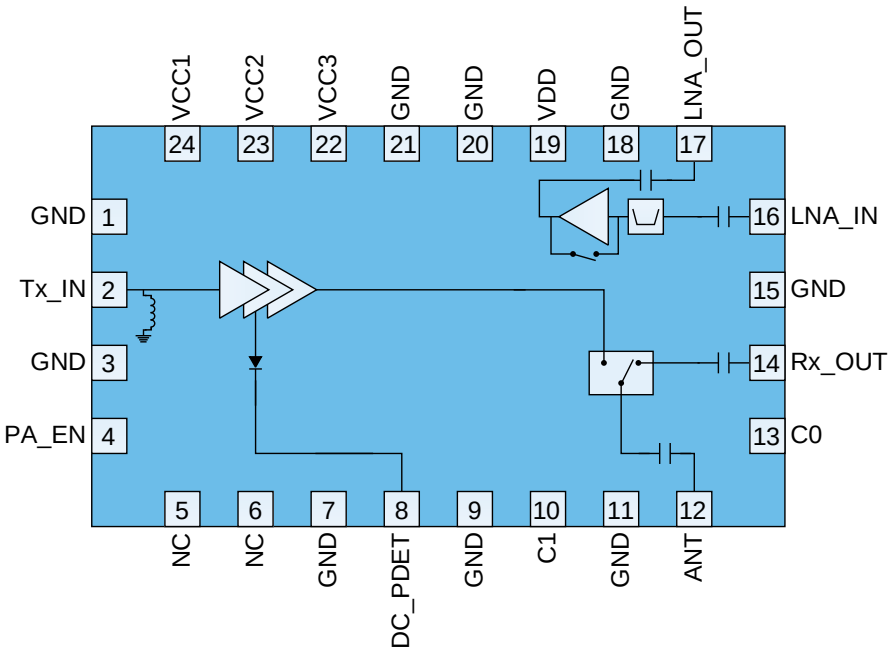


Figure 1. Functional Block Diagram & Pin-out Detail

Table 1. QPF4519 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1, 3, 7, 9, 11, 15, 18, 20, 21	GND	Ground connection
2	TX_IN	RF Input — internally matched to 50 Ω and DC shorted
4	PA_EN	Input enable bias voltage — regulated internally
5, 6	NC	No electrical connection — may be left floating or grounded
8	DC_PDET	DC power detector — provides an output voltage proportional to the RF output power level
10	C1	Switch control pin 1
12	ANT	RF bi-directional antenna port — internally matched to 50 Ω and DC blocked
13	C0	Switch control pin 0
14	RX_OUT	RF output from RX branch of the T/R switch — internally matched to 50 Ω and DC blocked
16	LNA_IN	RF input to the LNA — internally matched to 50 Ω and DC blocked
17	LNA_OUT	RF output from LNA — internally matched to 50 Ω and DC blocked
19	VDD	LNA supply voltage
22	VCC3	Third stage supply voltage
23	VCC2	Second stage supply voltage
24	VCC1	First stage supply voltage
GND Paddle		RF/DC Ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB mounting pattern for suggested footprint

Evaluation Board Information

The Qorvo QPF4519 Evaluation Board (EVB) is designed to provide performance comparable to that found in an actual application. Designed to operate with 50 Ω load impedances at all RF ports, the EVB has SMA connector interfaces. No tuning is applied between the module RF pins and the EVB SMA connectors. Evaluation Board Layout and Schematic.

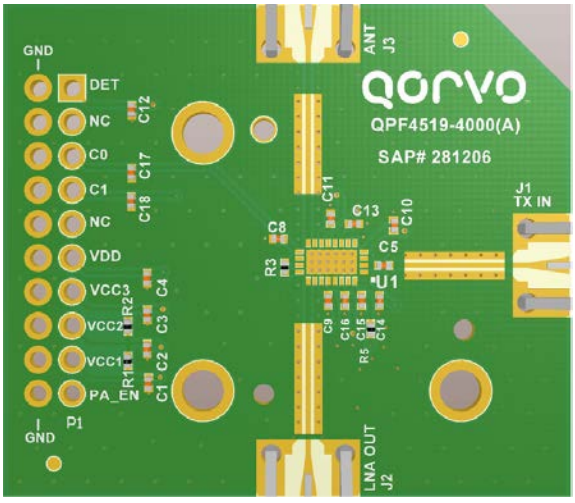


Figure 2a. QPF4519 Evaluation Board Photo

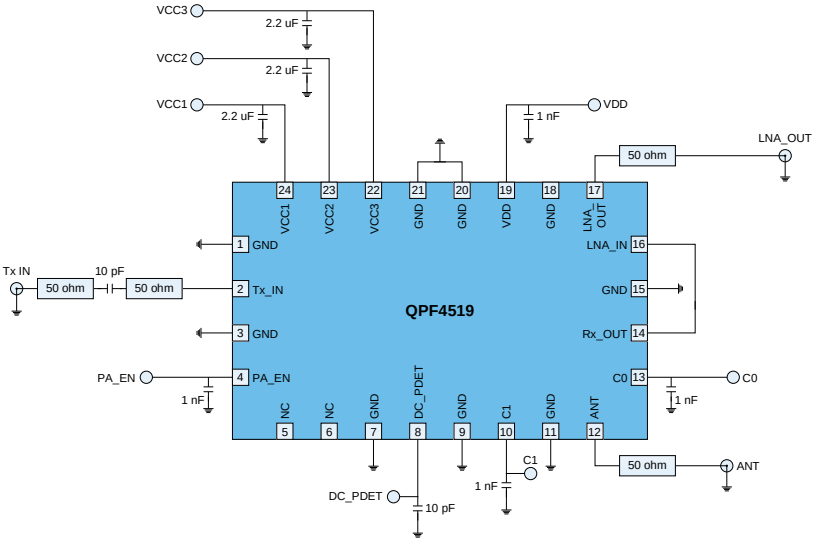


Figure 2b. QPF4519-EVB Schematic

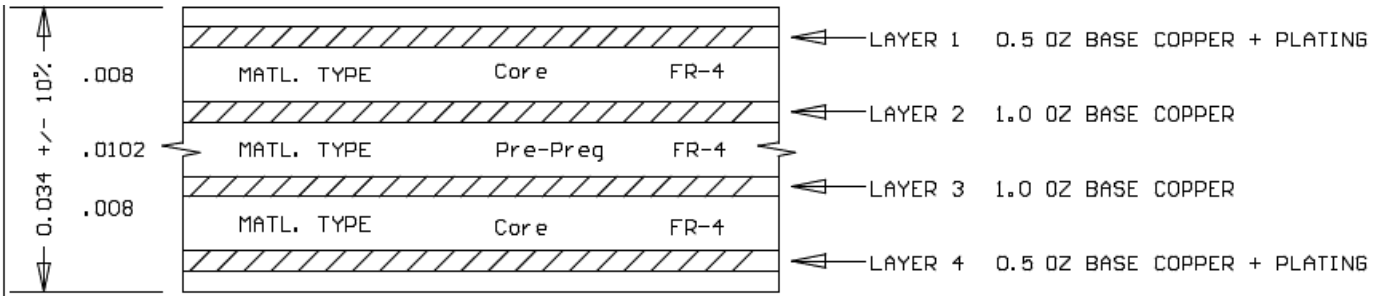


Figure 2c. QPF4519-PCB Stack-up Layers Diagram

Recommended Biasing Sequence

Table 2 below provides the logic truth table for the QPF4519.

MODE	STATE	PA_EN	C0	C1
All Off	1	Low	Low	Low
Transmit	2	High	Low	High
LNA On	3	Low	High	Low
Bypass LNA	4	Low	High	High

Table 2. Logic Table

The QPF4519 logic control and RF input require correct timing to ensure optimal performance and reliable operation. See turn on/off procedure below.

Transmit Power-On Procedure:

1. Connect Power Supplies in OFF mode (0 V) to V_{CC}, V_{DD}, and PA_EN pins.
2. Apply +5.0 V to V_{CC}, V_{DD} pins.
3. Apply control voltages (0 V to C0 and from +3.0 V to V_{CC} to C1 pin.)
4. Apply RF input signal to J1 (Tx pin 2), transmit RF; measure RF output on J3 (ANT pin 12).
5. Power detector output can be monitored on PDET, pin 8.

Transmit Power-Off Procedure:

1. Remove RF input signal.
2. Set all control signals (PA_EN, C0, and C1) to 0 V.
3. Set the Power Supply Voltages on V_{CC}, V_{DD} to 0 V.

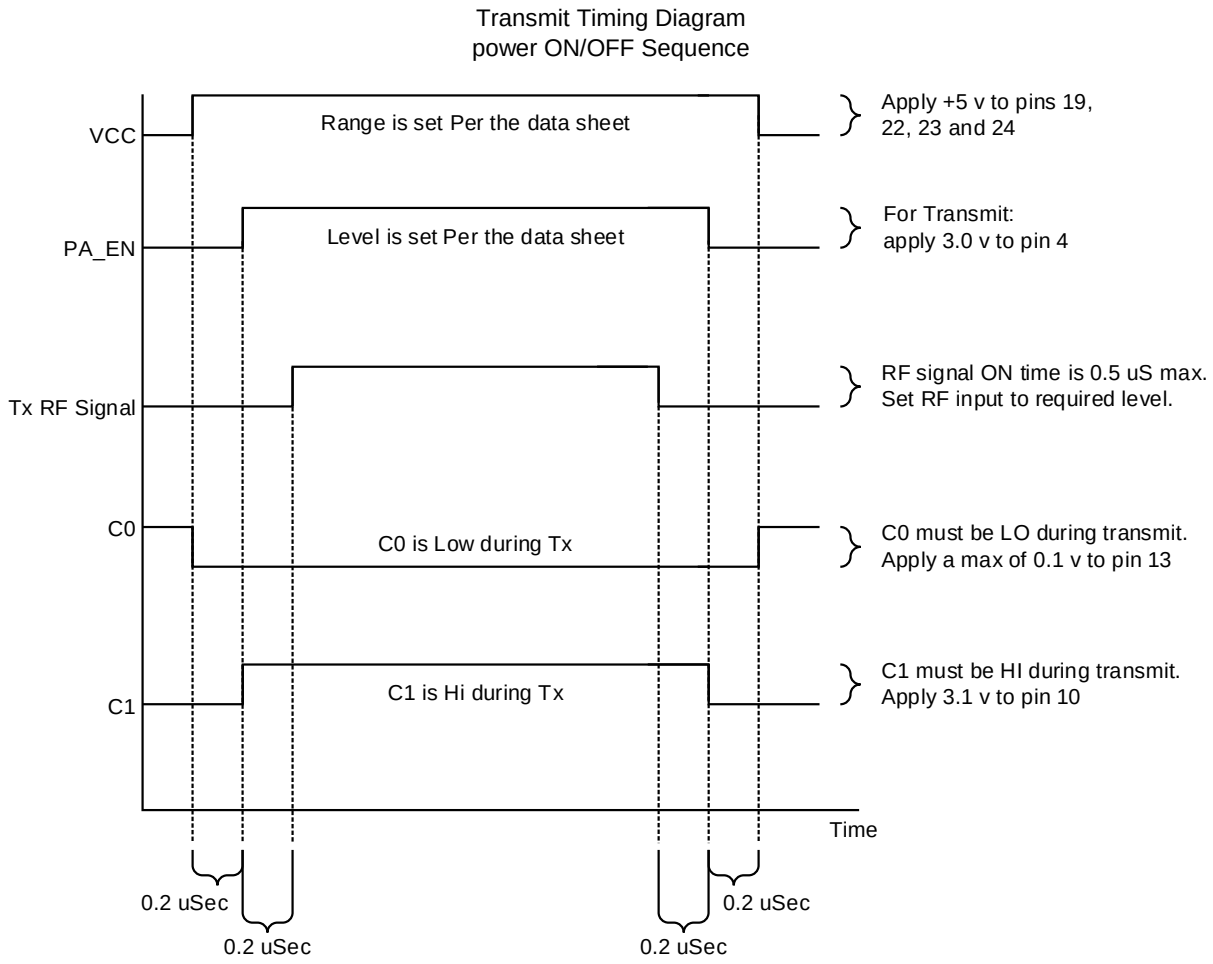


Figure 3. QPF4519 Recommended Control Timing.

Notes:

1. RF Signal for each specific mode is applied after the DC bias is applied.
2. Total ON/OFF time includes from 10% of control switching to 90% of RF power.
3. Listed values on diagram are typical. The maximum is 0.5 uSec for each mode.

System Architecture Application Circuit Recommendations

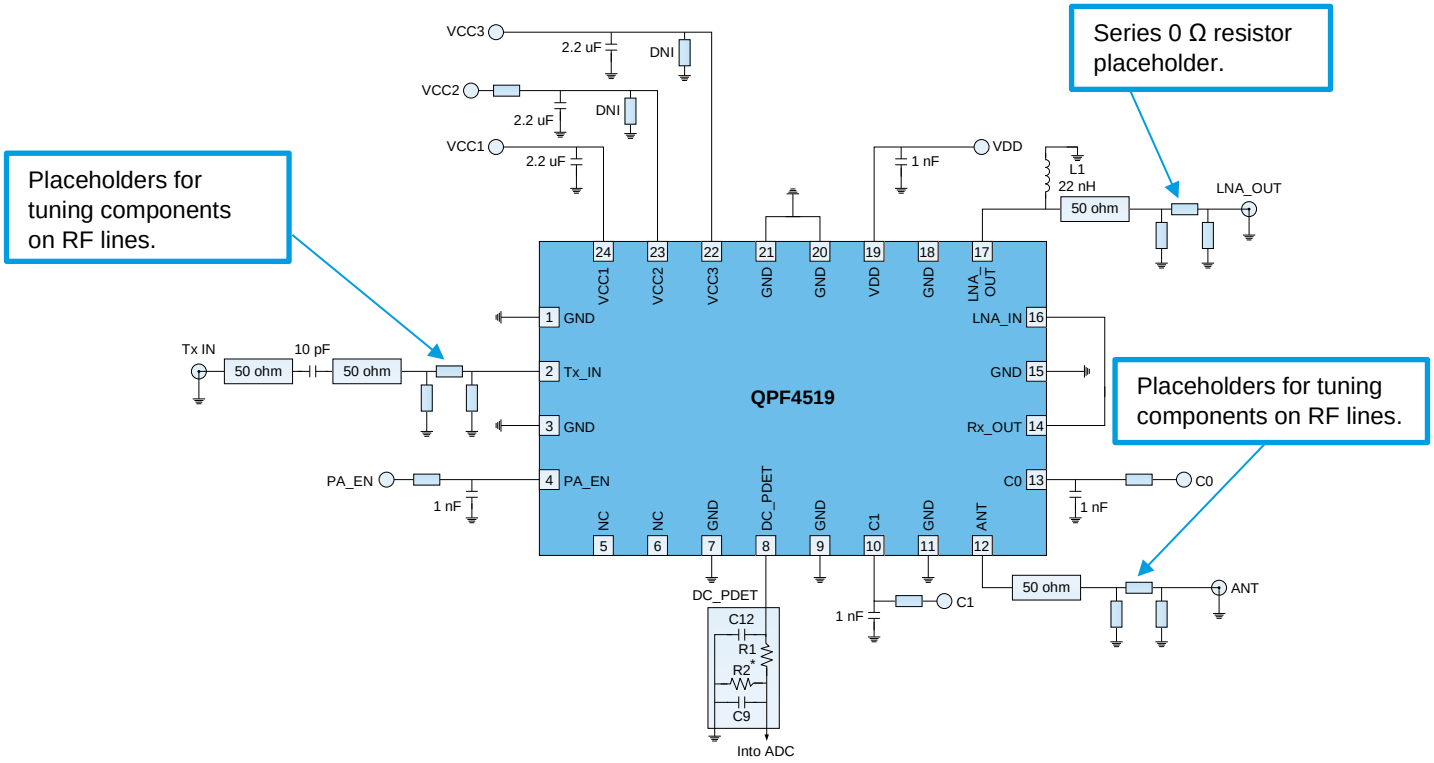


Figure 4. Recommended Application Circuit in a System.

1. The above schematic shows recommended bypassing values based on QPF4519-EVB. The customer should ensure that sufficient bypassing is provided based on their PCB layout. In addition, one should ensure all bypass capacitors are placed as close as possible to respective FEM pins, with the lowest values placed closest to the part pin. It is also recommended that at least one ground via be placed right next to each bypass capacitor ground pad to minimize ground return inductance between the capacitor and the FEM ground.

2. Recommend placing a shunt inductor (L1) of 22 nH value close to the output of LNA_Out pin (pin 17). It provides additional immunity to ESD protection to the part and does not degrade any RF performance.

3. In case there is DC present on the lines connecting RF paths on the board, we recommend using DC block per the recommended values in the schematic. There is no DC present on RF ports of FEM internally. Low value external DC blocking capacitors, however, can be beneficial for improving ESD immunity and overall ruggedness in the presence of transients. The capacitor values should be chosen to be series resonant at approximately mid band. 10 pF is a good choice, assuming the use of standard 0402 or 0201 SMD capacitors.

4. PDET (pin 8) should not be left floating and should be terminated with 100 pF capacitors if this pin is not being used.

5. Suggest having a series element to customer layout at the output of PDET (pin 8) to have flexibility for low-pass filter, if required. R1 can be replaced as 0 Ohm. Since output of detector goes into ADC that acts as high impedance, therefore, external shunt R2 may not be needed for pin 8.

6. Recommend using a “pi” placeholder for tuning flexibility at FEM TX and RX RF ports. In addition, try to place tuning placeholder close to FEM. Transceiver matching components should be placed closer to transceiver with 50-ohm trace connecting to “pi” placeholder near to FEM Input.

7. NC is no connect and can be left floating or grounded on the board. Grounding this pin can add better mounting integrity. If grounding, we suggest to ground it close to FEM pin.

8. It is recommended to fully populate the ground slug with as many thermal vias as possible and to add ground vias around RF traces.

9. Route control lines on separate layer, other than the signal layer, whenever possible and isolate control line traces from RF and V_{CC} traces. Keep a minimum distance of 150 µm between Tx and Rx control lines to minimize coupling.

10. We recommend following Qorvo evaluation board layout guidelines as close as possible. QPF4519 evaluation board uses 12 mil vias and 22 mil pads. Gerber files are available upon request.

PCB Layout Considerations

Board layout must be carefully considered to achieve optimal performance from any FEM, including the QPF4519. In addition to providing connectivity between the FEM and external components, the PCB layout is a part of the overall circuit. The RF and DC parasitic of the traces, along with coupling between traces, must be evaluated. The QPF4519 Evaluation Board PCB layout guidelines provide a good starting point for designing the layout in the actual application.

RF Traces

All of the PCB traces between the RF pins and matching networks (where applicable) should be 50 Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. The RF traces should be routed on the top layer to minimize coupling with other RF, control input, and DC traces. If it is not possible for some reason to route RF traces on the top layer, we suggest that you make sure there is proper isolation between traces on the layout to avoid any coupling issues. RF lines should be isolated from other RF and DC signals by adding solid ground planes (with vias) between them to minimize coupling and cross-talking. In addition, we also recommend reducing RF trace lengths, wherever possible.

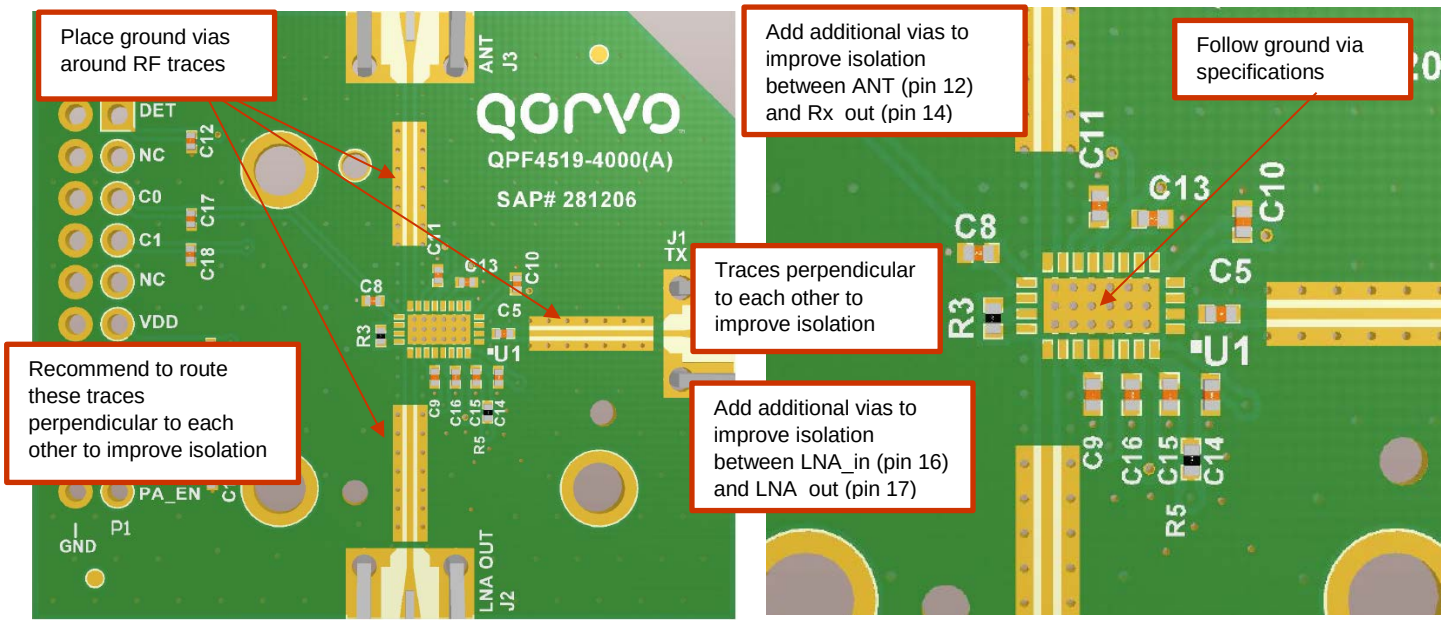


Figure 5a. Example Recommended PCB layout Considerations.

Grounding Considerations

Connect the module center ground pad directly to the main ground plane layer using as many vias as possible. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible. This ground layer also provides the reference layer for microstrip lines.

Close attention should be paid to the grounding of the PA ground slug, the solid metalized area on the bottom side of the package. This serves as the primary RF and DC ground return for the entire PA, as well as the primary path for heat removal. A larger number of via holes should be distributed over the entire ground area below the PA to provide good RF and DC ground returns, as shown in **Figure 5b** below.

Additionally, the vias will serve as a low resistance thermal path between the PA and the PCB. Vias passing through multiple copper layers provide the best overall RF, DC, and thermal performance. It is important to ensure proper vias on ground slug / paddle for better thermal consideration. The QPF4519 ground slug / paddle has special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduct path for heat dissipation. The GND pad and vias pattern and size used on the Qorvo evaluation board should be replicated. The Qorvo layout files in Gerber format can be provided upon request.

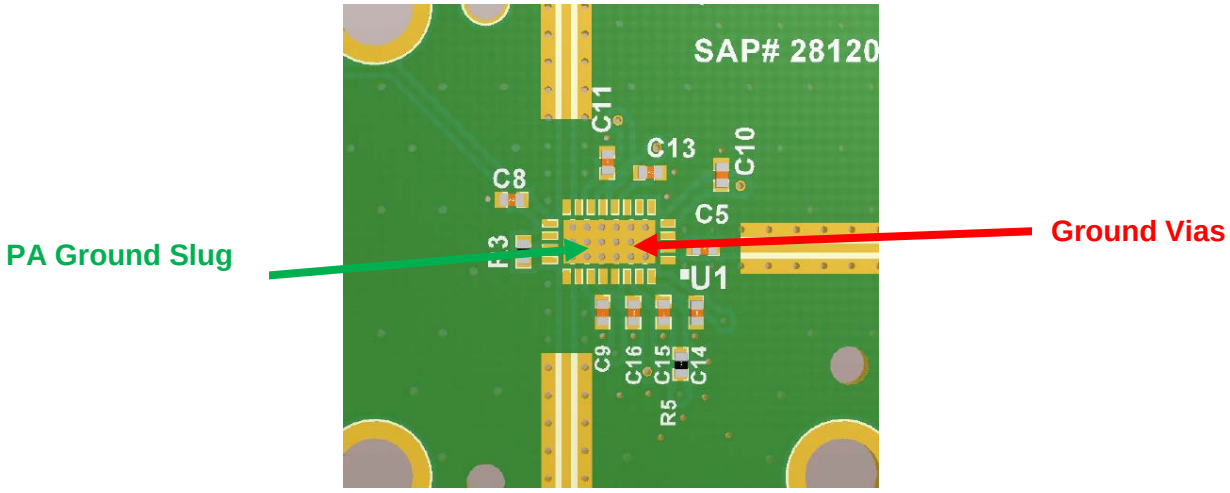


Figure 5b. Example Recommended Ground Via Placement on Module Ground Slug.

DC Layout Considerations

The V_{CC} DC traces must provide low impedances back to their main supply rail. This is the most important layout consideration for the DC layout. Where possible, power planes should be used to route these traces. Where this is not possible due to space constraints, the traces should be made as wide as possible, using multiple copper layers if necessary to achieve an equivalent width of 2 mm or more.

There should be at least one ground layer between these traces and any RF traces even though both are running diagonal to each other on different layers to minimize coupling.

When connecting all V_{CC} pins on the board together, we recommend connecting V_{CC} pins (pin 19, 22, 23, 24) before bypass capacitors as shown in figure 5c. In addition, we suggest running a longer trace for better isolation.

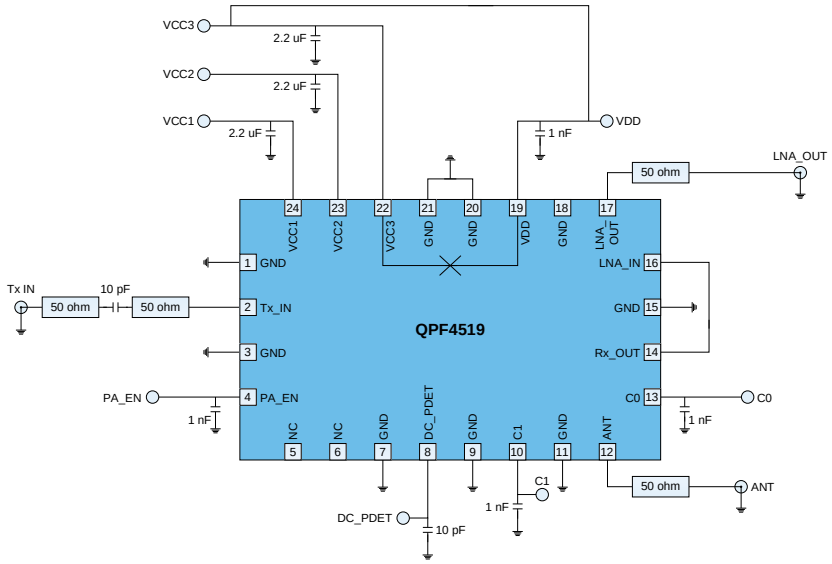


Figure 5c. Recommended Configuration while connecting Vcc pins (19, 22, 23, 24) on the PCB board.

PCB Footprint Recommendations

See **Figures 6a and 6b** below for the recommended package outline drawing and solder mask patterns.

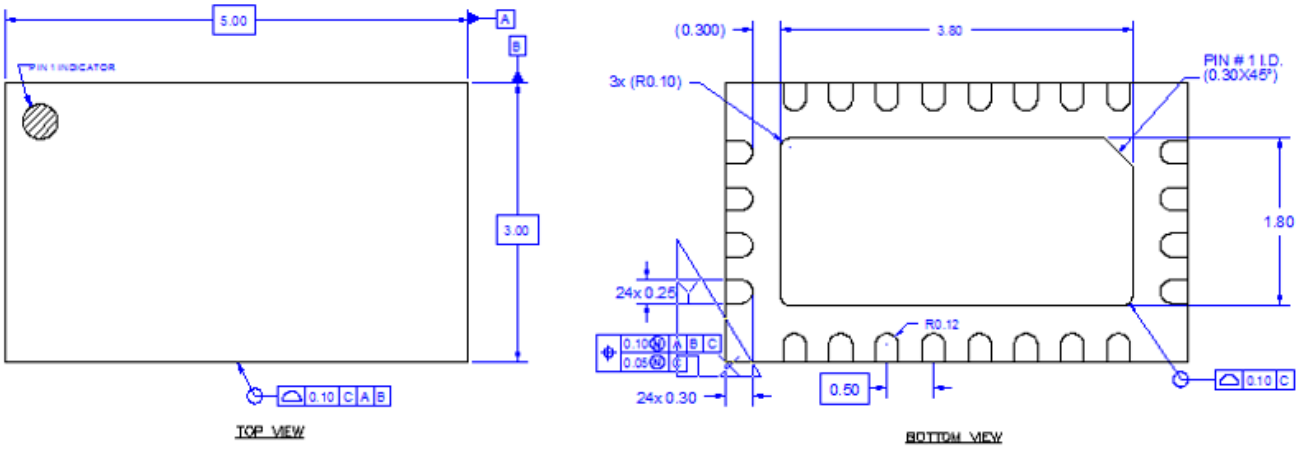


Figure 6a. QPF4519 Package Outline Drawing.

PCB Footprint Recommendations (Cont.)

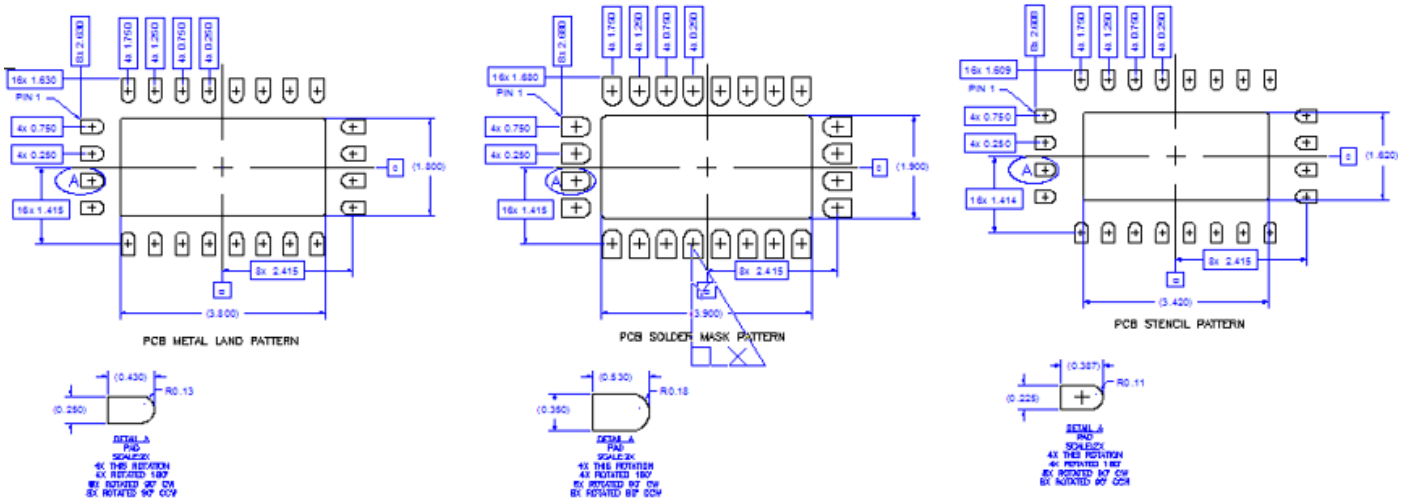
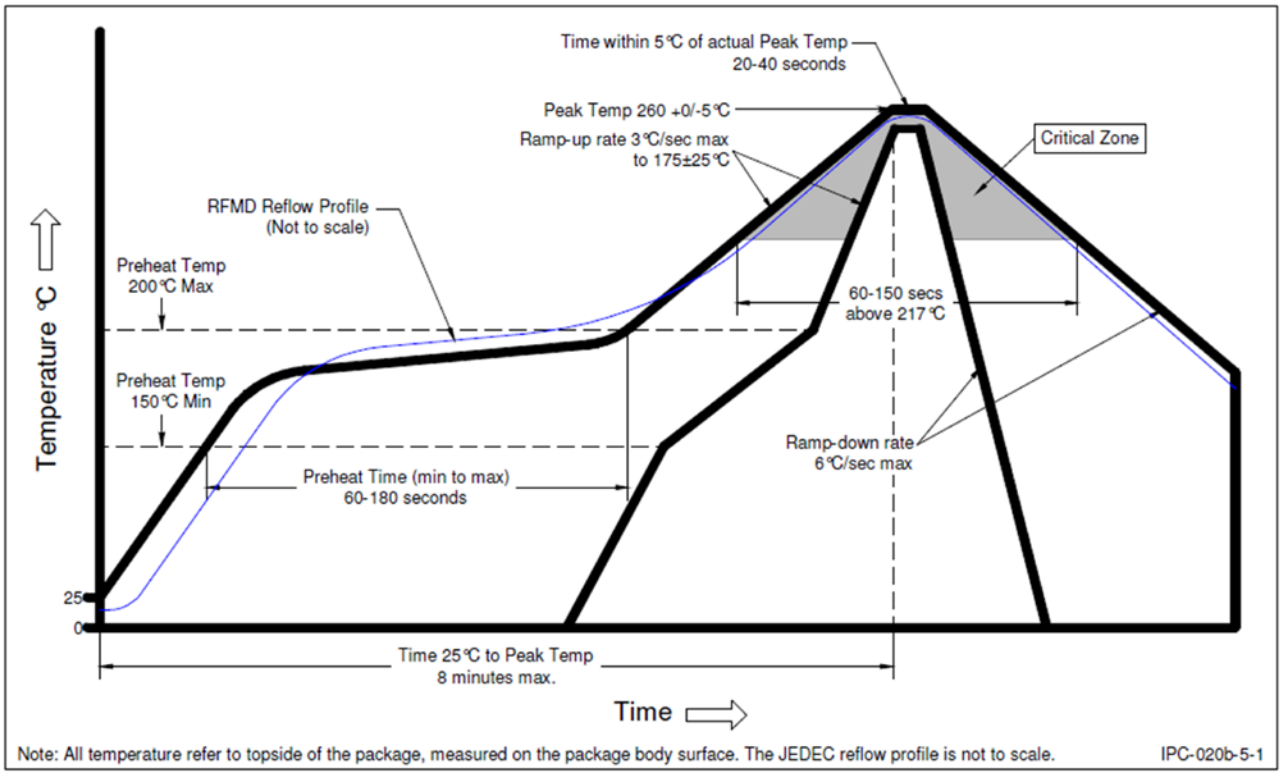


Figure 6b. PCB Footprint Recommended Solder Mask Pattern.

Reflow Profile & Solder Paste

Figure 6c illustrates the reflow profile recommended for the QPF4519.



CONDITIONS	
Ramp-up rate	3 ºC/second max.
Preheat temperature 175 (±25) ºC	180 seconds max.
Temperature maintained above 217 ºC	60 seconds to 150 seconds
Time within 5 ºC of actual peak temperature	20 seconds to 40 seconds
Peak temperature range	260+0/-5 ºC
Ramp-down rate	6 ºC/second max.
Time 25 ºC to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤ 3
Pre-baking requirements	Refer to JEDEC J-STD-033 if original device package is unsealed
Maximum reflow temperature	260 ºC

Figure 6c. Recommended Reflow Profile & Conditions

Maximum reflow temperature is 260 ºC. The temperature used to classify the MSL level appears on the MSL label on each shipping bag. Qorvo uses reflow profiles in accordance with IPC/JEDEC J-STD-020 for qualification with the exception of the maximum reflow temperature of 260 ºC.

Solder paste used for the Qorvo high temperature reflow qualification.

SPECIFICATIONS	
Solder paste	Multicore 96SCAGS89 (CR39)
Alloy type	Sn95.5/Ag3.8/Cu0.7
Metal content	88.5%
Solder particle size	45 µm to 20 µm

Figure 6d. Solder Paste Specifications.

Support Data

For any further data on the QPF4519, please request Qorvo point of contact such as marketing, sales or a representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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