QPM1017

5.7 – 7 GHz 100 W GaN Power Amplifier Module

Product Overview

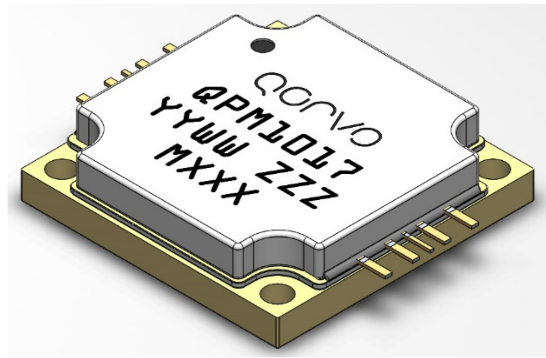
Qorvo's QPM1017 is a packaged, high-power C-band amplifier module, fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). Covering 5.7 – 7 GHz, the QPM1017 provides 100 W of saturated output power with 18 dB of large signal gain while achieving > 35% power-added efficiency. For satellite communications applications, QPM1017 provides 40 W linear power with 25 dBc third order intermodulation distortion products.

The QPM1017 is packaged in a 10-lead 19.05 x 19.05 mm bolt-down package with a Cu base for superior thermal management. It can support a variety of operating conditions to best support system requirements.

To simplify system integration, QPM1017 is fully matched to 50 ohms. Input port is DC grounded for improved ESD performance, output port is AC coupled with integrated DC blocking capacitor.

The QPM1017 is ideal for supporting communications and radar applications in both commercial and military markets

RoHS compliant

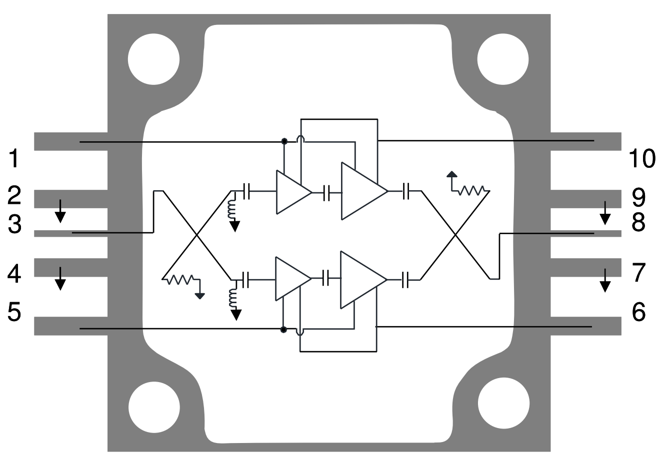


Key Features

- Frequency Range: 5.7 – 7 GHz
- P_{SAT} (P_{IN} = 32 dBm): 50 dBm
- PAE (P_{IN} = 32 dBm): > 35 %
- Power Gain (P_{IN} = 32 dBm): 18 dB
- IM3 (P_{OUT}/Tone = 43 dBm): -25 dBc
- Small Signal Gain: > 24 dB
- Bias: V_D = +24 V, I_{DQ} = 3.4 A, V_G = -2.5 V typ.
- Dimensions: 19.05 x 19.05 x 4.5 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- C-Band Radar
- Satellite Communications

Ordering Information

Part No.	Description
QPM1017	5.7 – 7 GHz 100 W GaN Power Amplifier Module (10 pcs. pack)
QPM1017S2	Samples (2 pcs. pack)
QPM1017EVB	Evaluation Board for QPM1017

Absolute Maximum Ratings

Parameter	Value / Range
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-6 V to 0 V
Drain Current (I_D)	20 A
Gate Current (I_G)	See plot page 18
Power Dissipation (P_{DISS}), 85 °C	Pulsed, 360 W CW, 200 W
Input Power (P_{IN}), Pulsed, 50 Ω, V_D = 24 V, I_{DQ} = 3.4 A, T_{BASE} = 85 °C,	36 dBm
Input Power (P_{IN}), Pulsed, 3:1 VSWR, V_D = 24 V, I_{DQ} = 3.4 A , T_{BASE} = 85 °C	36 dBm
Mounting Temperature	Refer to Assembly Notes, page 22
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)		+24	+24	V
Drain Current, Quiescent (I_{DQ})		3.4		A
Drain Current, RF (I_{D_Drive})	See chart page 4, 7			A
Gate Voltage Typ. Range (V_G)		−2 to -2.9		V
Gate Current, RF (I_{G_Drive})	See chart page 4, 7			mA
Operating Temp. Range (T_{BASE})	−40		+85	ºC

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

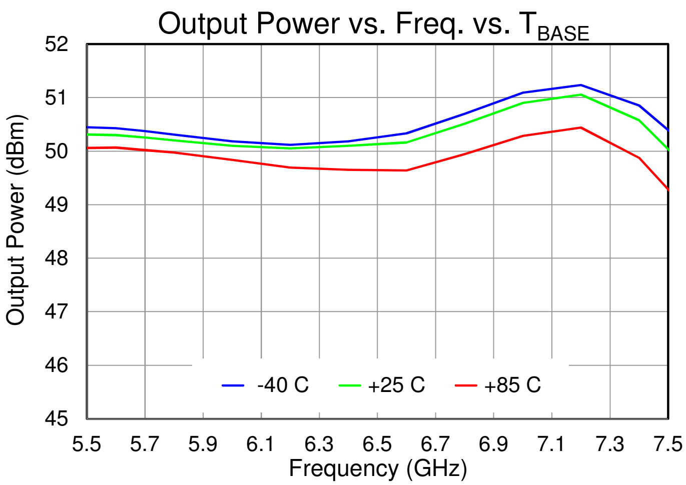
Parameter	Conditions [1] [2]	Min	Typ.	Max	Units
Operational Frequency Range		5.7		7	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = +32 dBm, Pulsed		50		dBm
Power Added Efficiency, PAE	P_{IN} = +32 dBm, Pulsed		35		%
Large Signal Gain	P_{IN} = +32 dBm, Pulsed		18		dB
Small Signal Gain, S21	CW		24		dB
Input Return Loss, IRL	CW		18		dB
Output Return Loss, ORL	CW		20		dB
3RD Intermodulation Products, IM3	P_{OUT}/Tone = 43 dBm; Freq. = 5.7, 6.4, 7 GHz; Δf = 5 MHz, CW		-25		dBc
5TH Intermodulation Products, IM5	P_{OUT}/Tone = 43 dBm; Freq. = 35 GHz; Δf = 5 MHz, CW		-35		dBc
P_{SAT} Temperature Coefficient	T_{DIFF} = −40 ºC to +85 ºC; P_{IN} = +26 dBm, Pulsed		-0.007		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = −40 ºC to +85 ºC, CW		-0.065		dB/ºC
Gate Leakage, I_G	V_D = +10 V, V_G = -4V, no RF	-70.4		0.01	mA

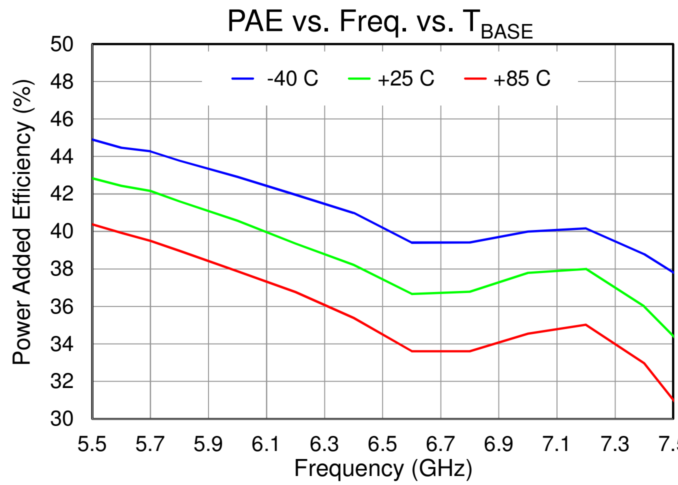
Notes:

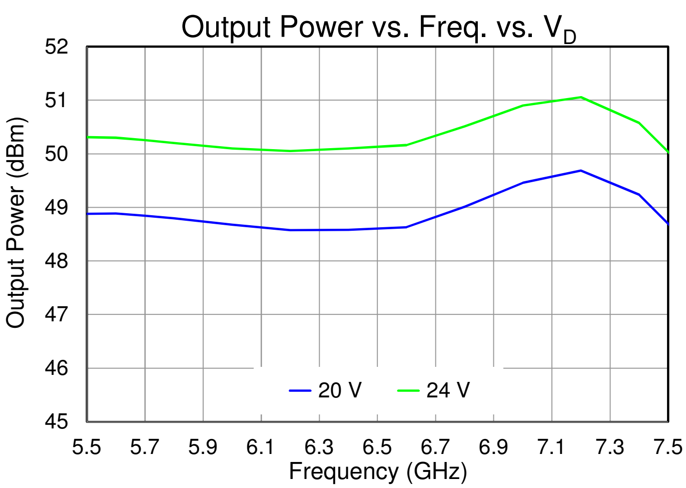
1. Test conditions unless otherwise noted: Pulsed V_D = +24 V, I_{DQ} = 3.4 A, V_G = -2.5V +/- typical, DC = 20%, PW = 150 us, T_{BASE} = +25 ºC, Z_0 = 50 Ω
2. T_{BASE} is back side of QPM1017

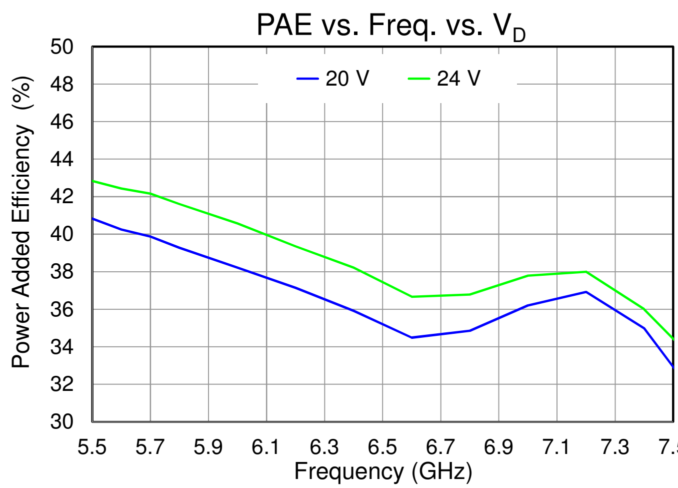
Performance Plots – Large Signal

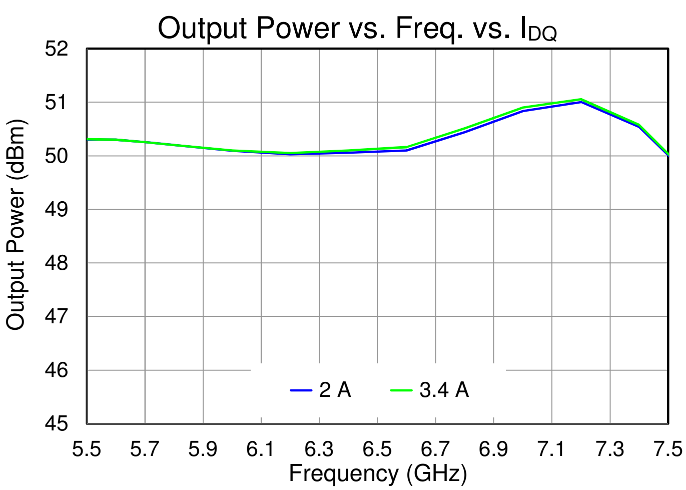
Test conditions, unless otherwise noted: **Pulsed** V_D = 24 V, I_{DQ} = 3.4 A, Duty Cycle = 20%, PW = 150 us, P_{IN} = 32 dBm, T_{BASE} = +25 ºC

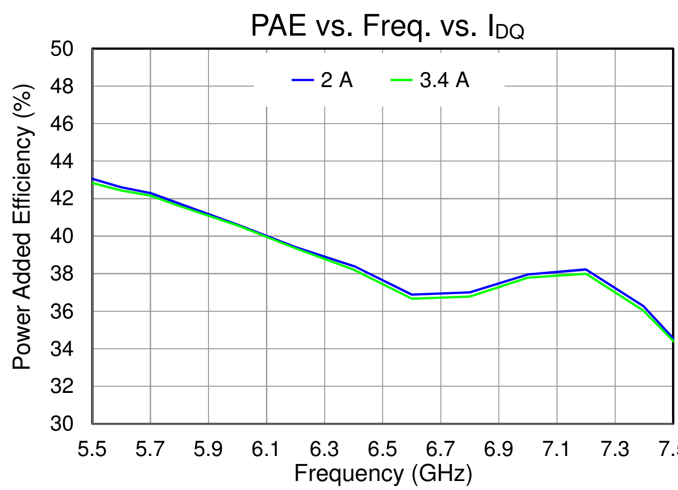








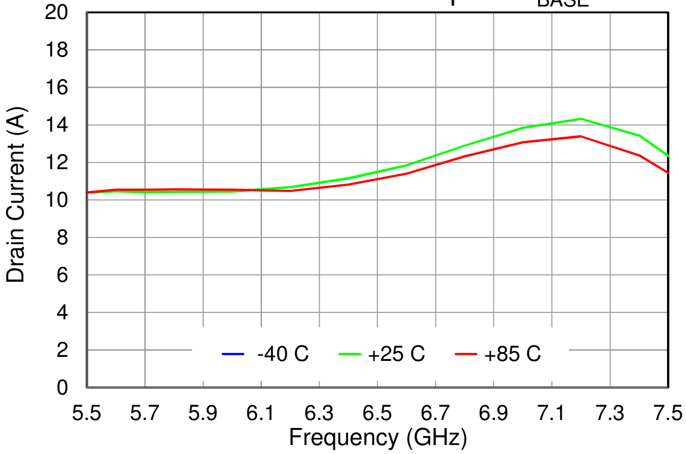




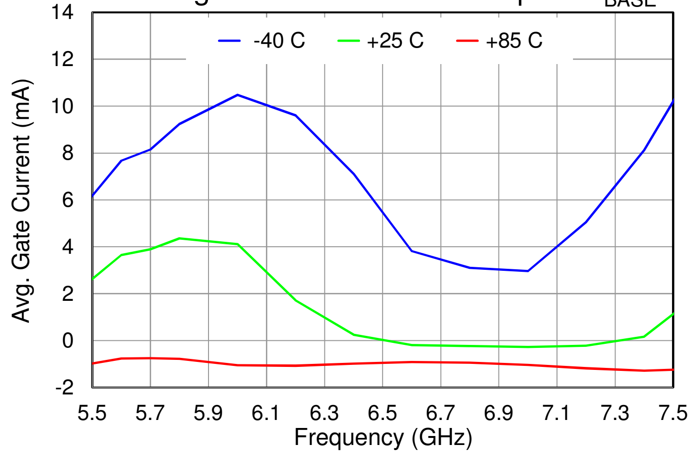
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed** V_D = 24 V, I_{DQ} = 3.4 A, Duty Cycle = 20%, PW = 150 us, P_{IN} = 32 dBm, T_{BASE} = +25 ºC

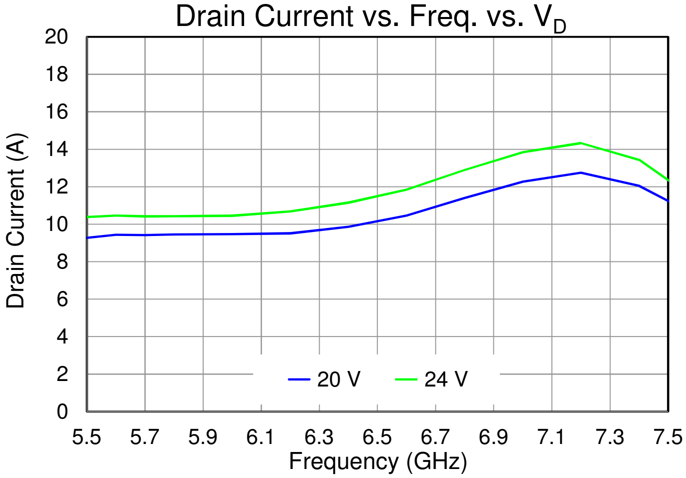
Drain Current vs. Freq. vs. T_{BASE}



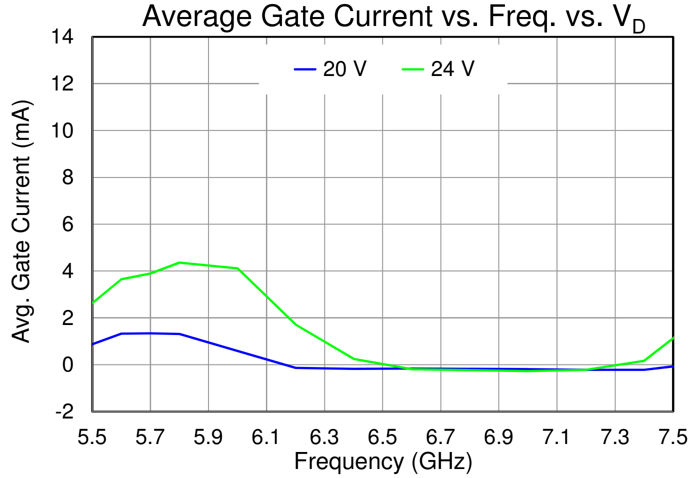
Average Gate Current vs. Freq. vs. T_{BASE}



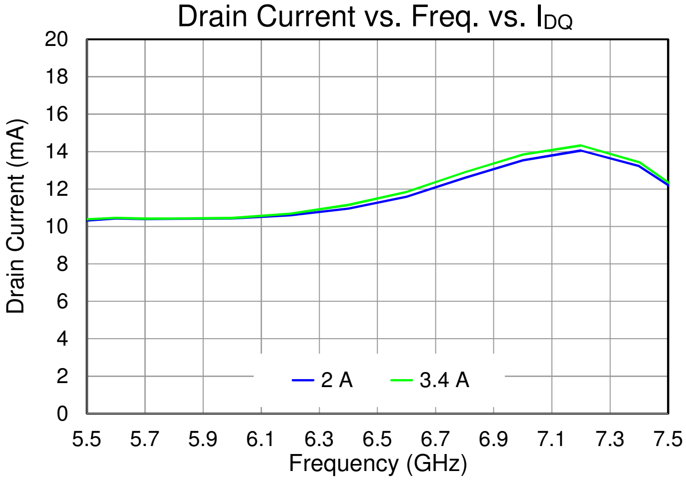
Drain Current vs. Freq. vs. V_D



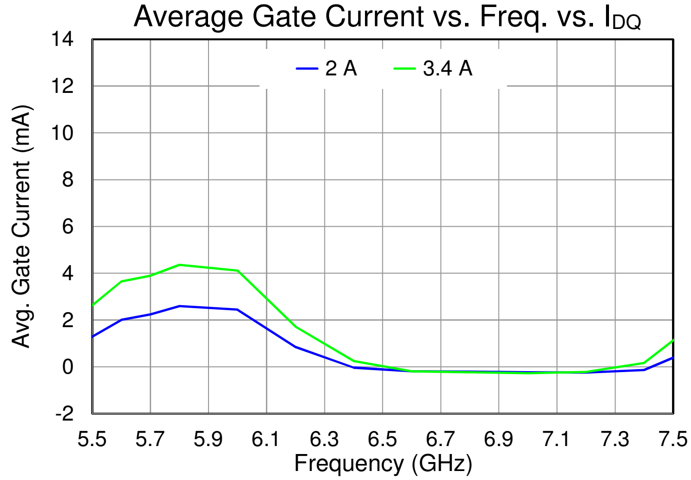
Average Gate Current vs. Freq. vs. V_D



Drain Current vs. Freq. vs. I_{DQ}



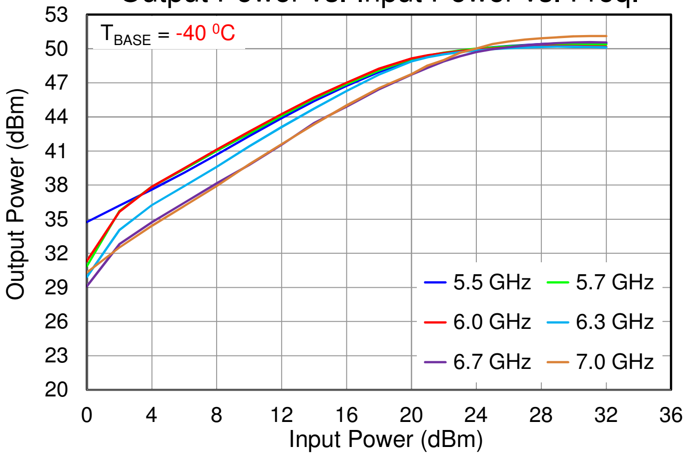
Average Gate Current vs. Freq. vs. I_{DQ}



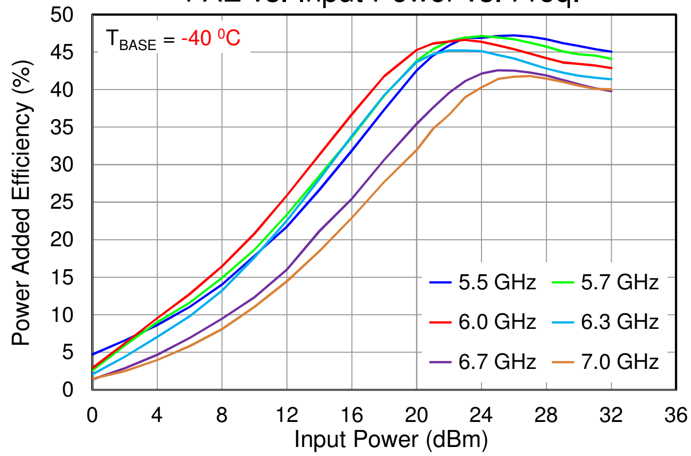
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **Pulsed** V_D = 24 V, I_{DQ} = 3.4 A, Duty Cycle = 20%, PW = 150 us, P_{IN} = 32 dBm, T_{BASE} = +25 ºC

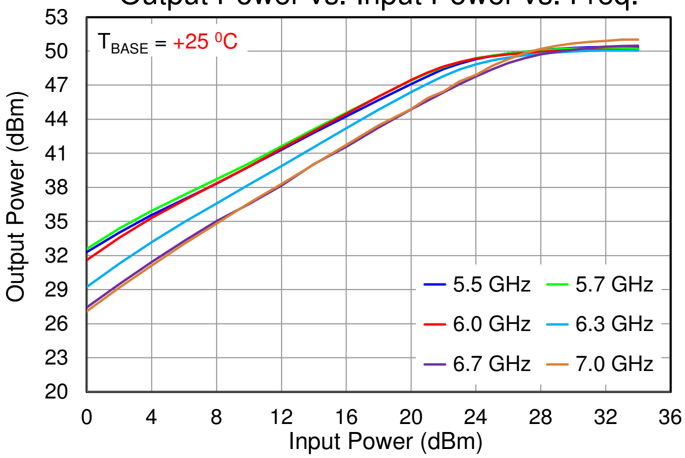
Output Power vs. Input Power vs. Freq.



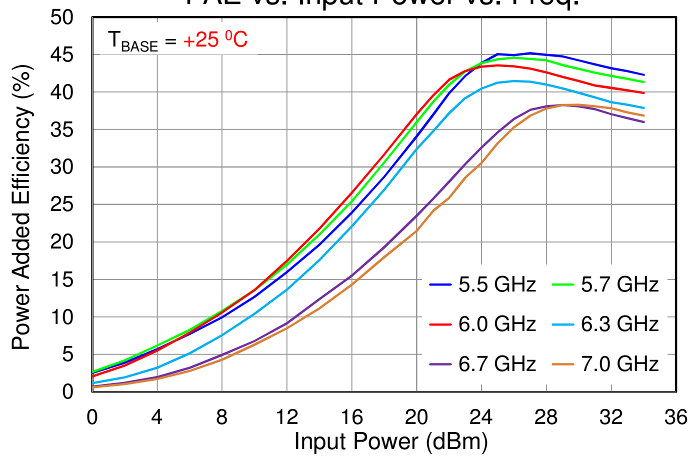
PAE vs. Input Power vs. Freq.



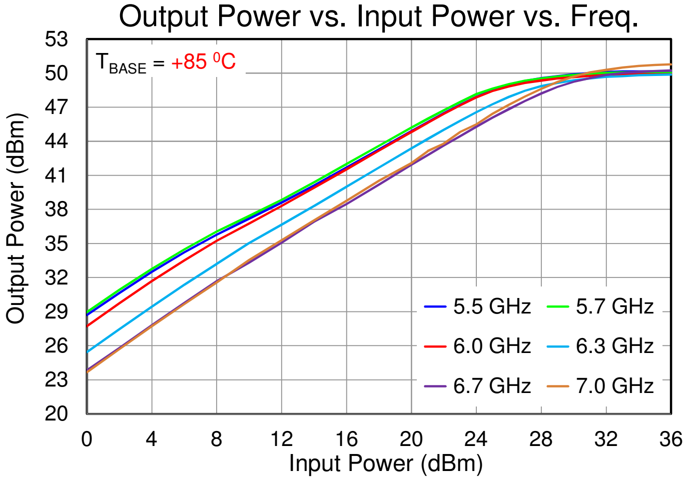
Output Power vs. Input Power vs. Freq.



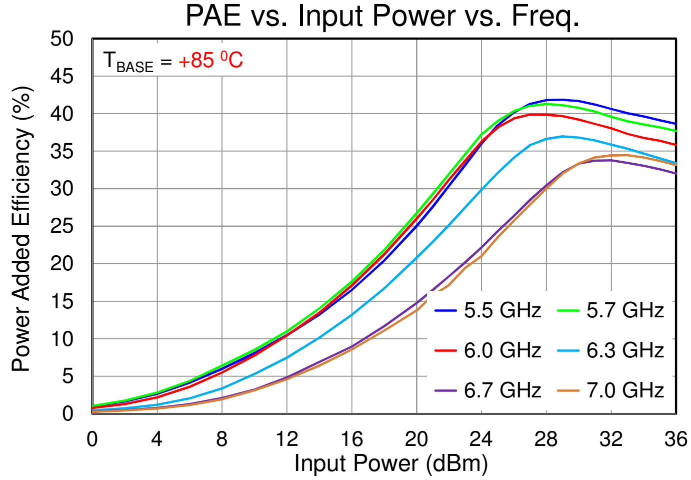
PAE vs. Input Power vs. Freq.



Output Power vs. Input Power vs. Freq.



PAE vs. Input Power vs. Freq.



Performance Plots – Large Signal

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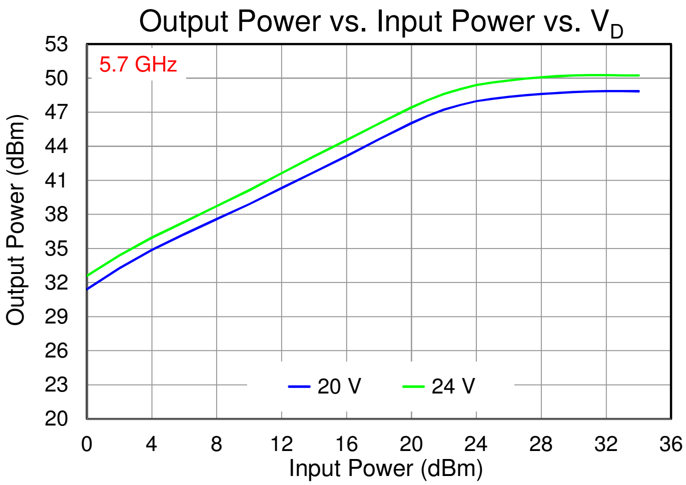

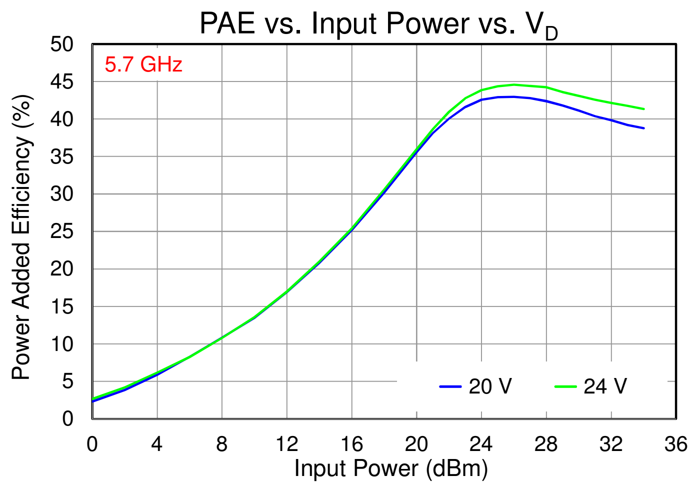

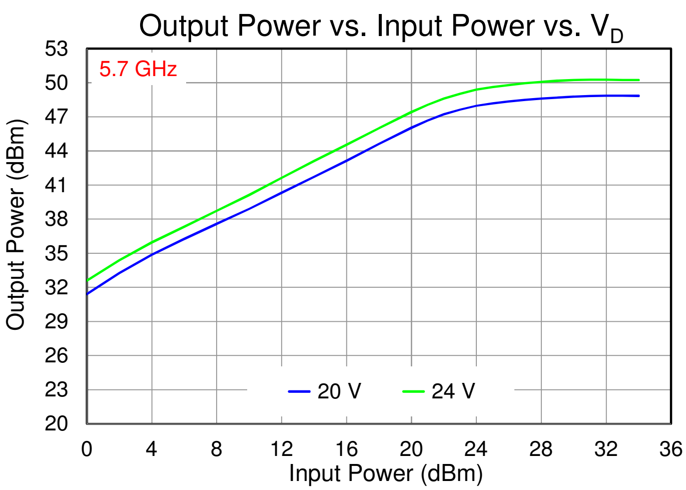

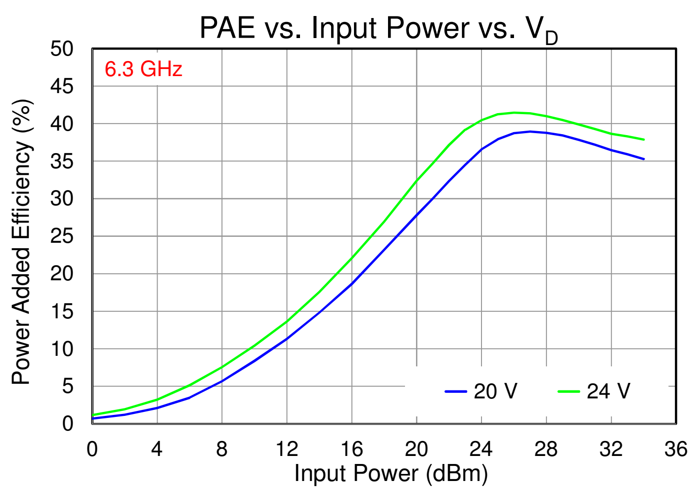

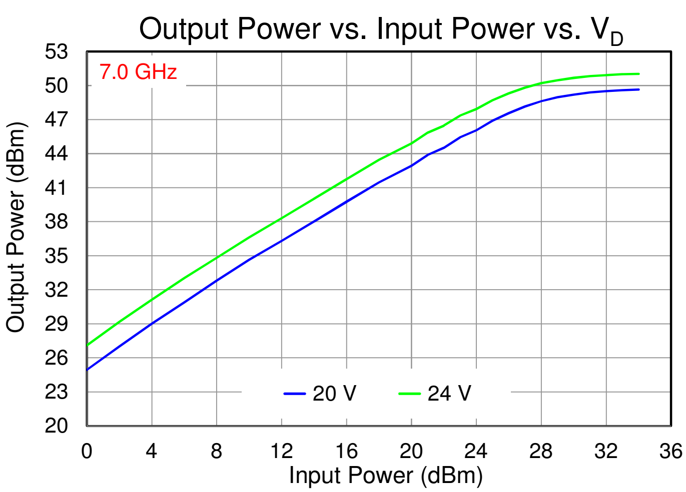

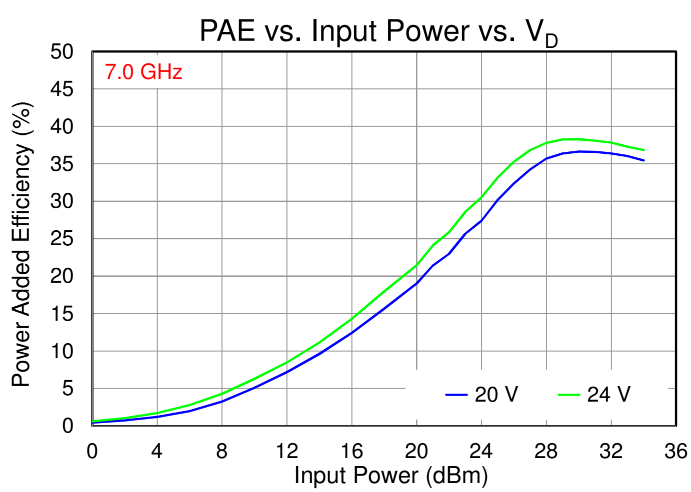

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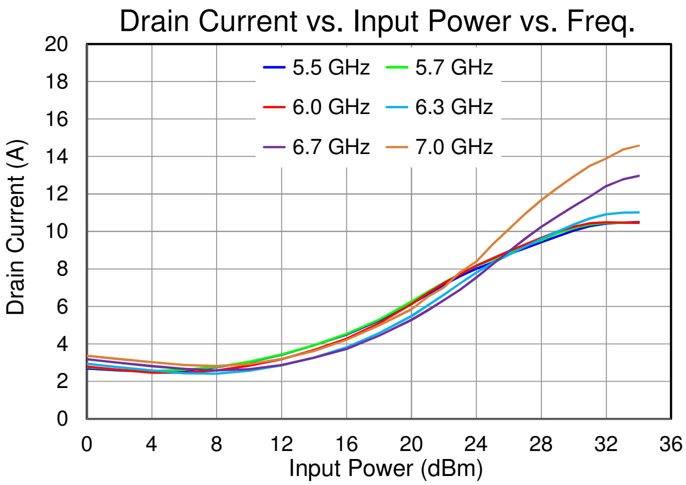

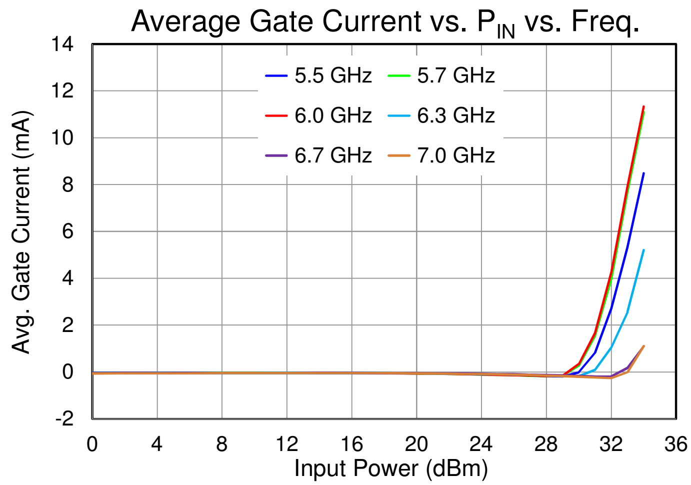

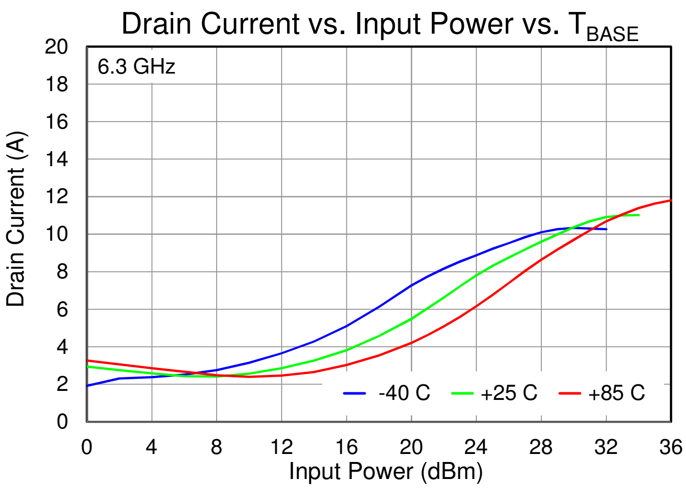

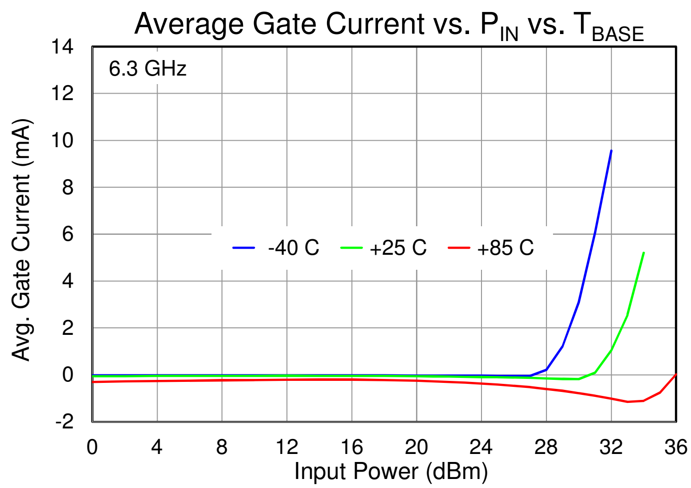

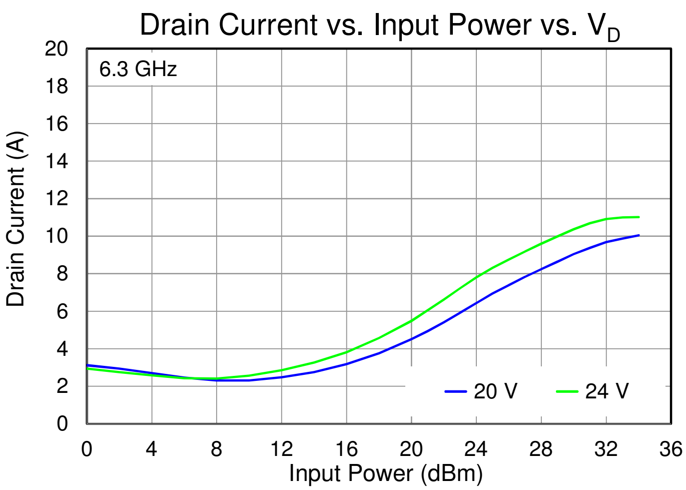

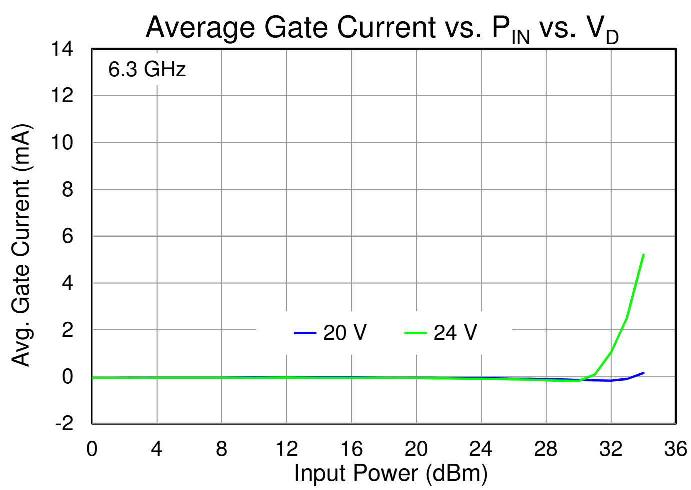

Performance Plots – Large Signal

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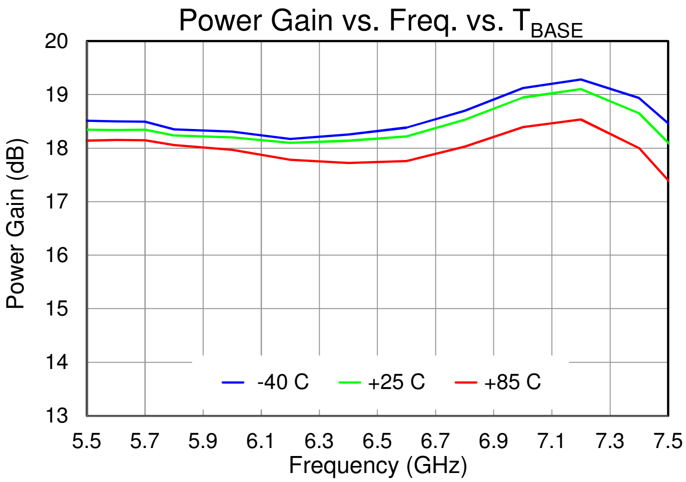
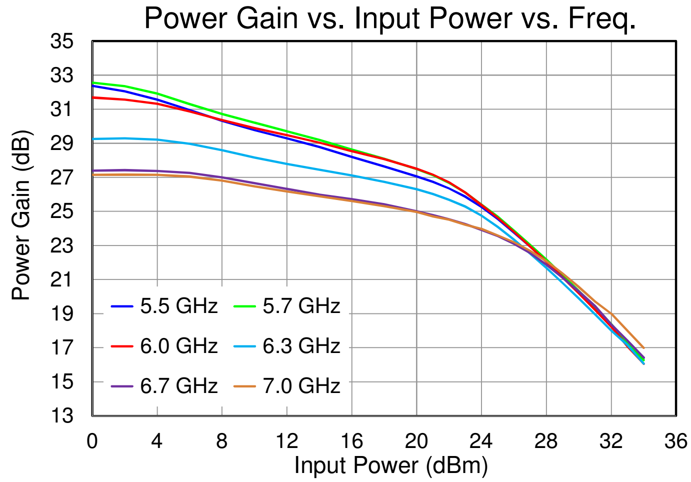
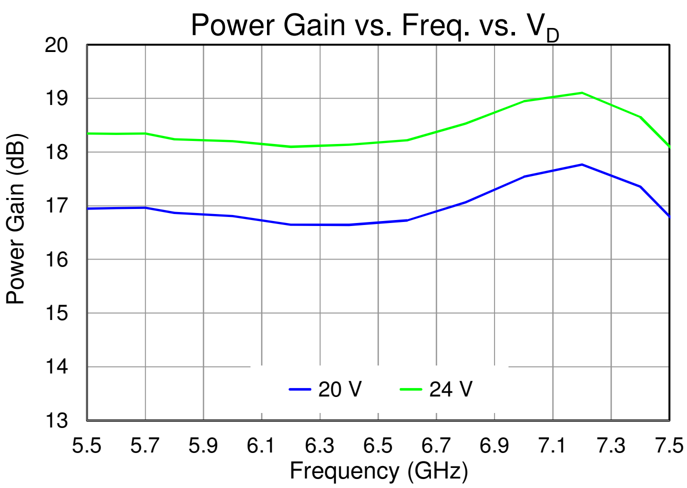
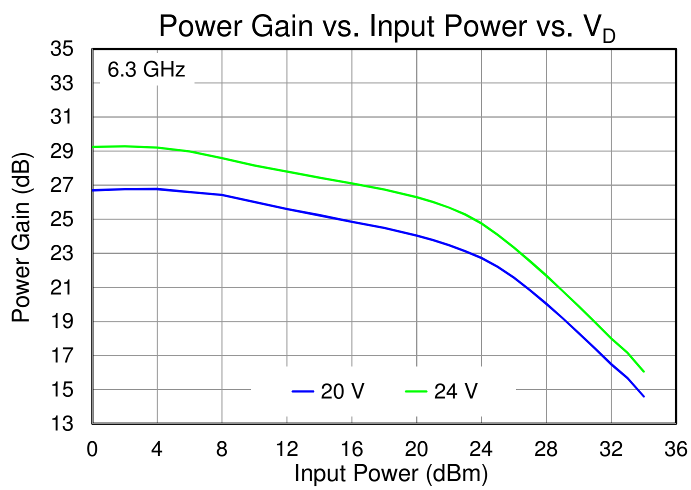
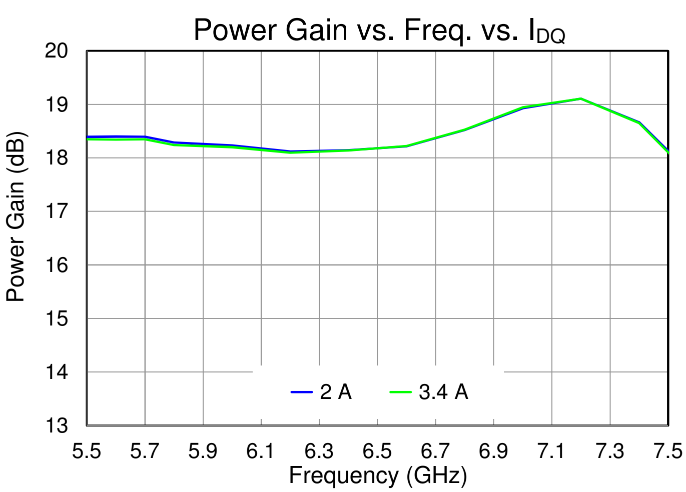
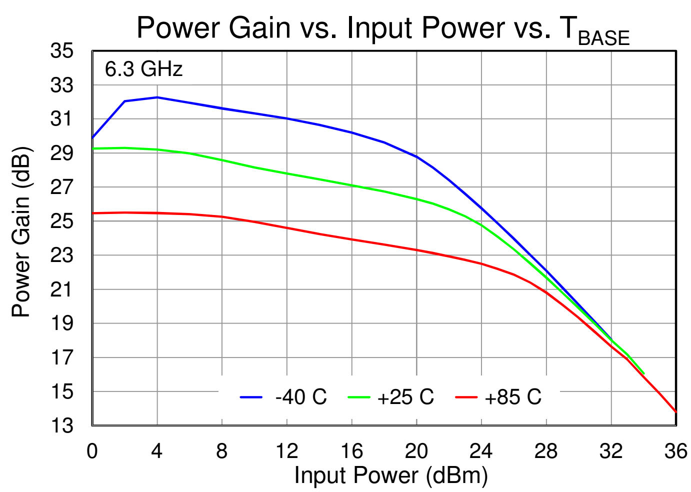






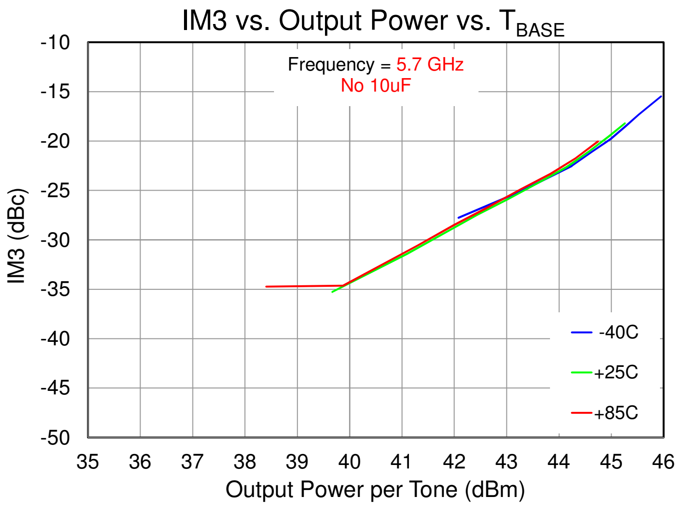


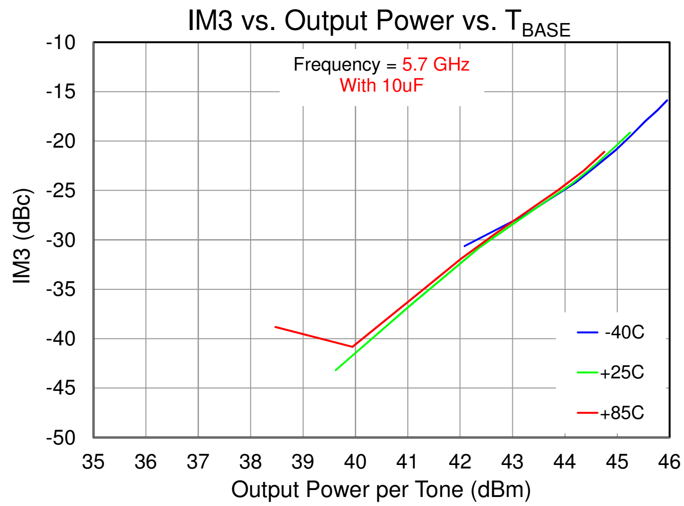


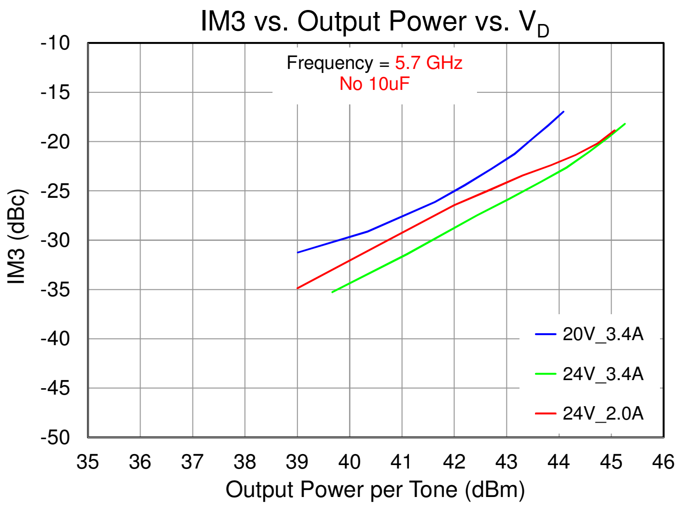


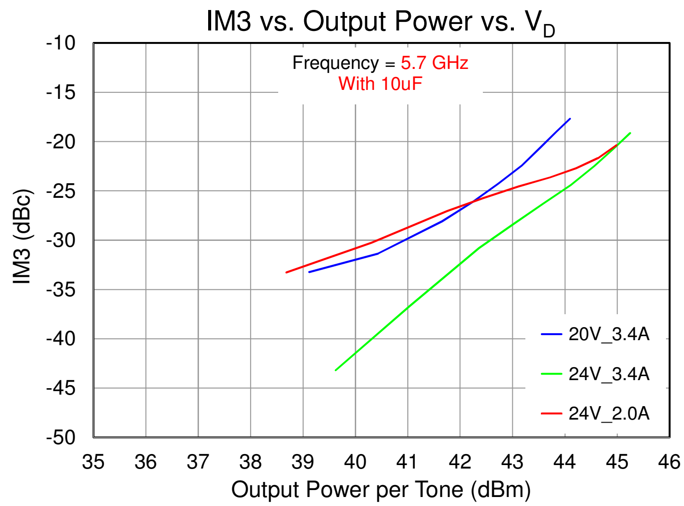
Performance Plots – Large Signal

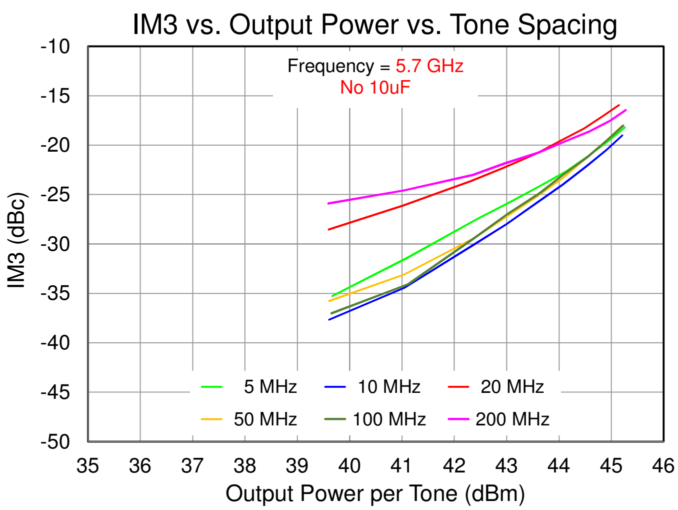
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, Tone Spacing = 5 MHz, T_{BASE} = +25 ºC, with/without 10uF at drain (C9, C12)

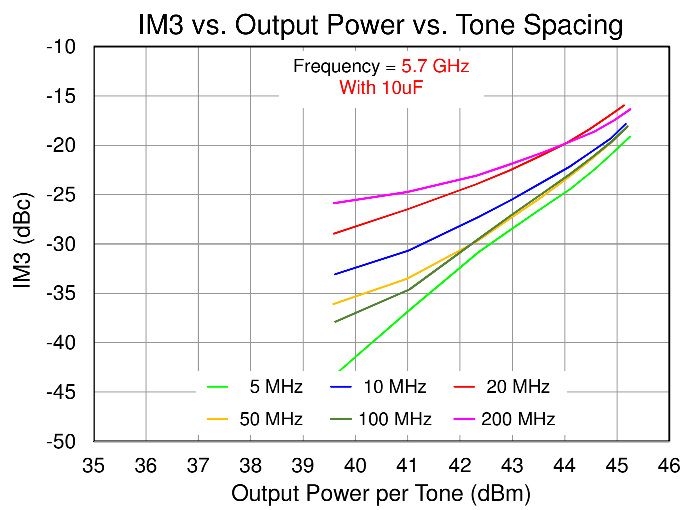






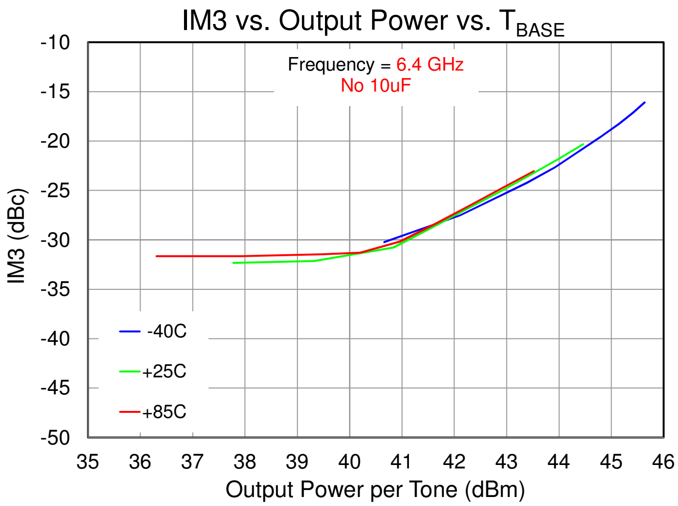


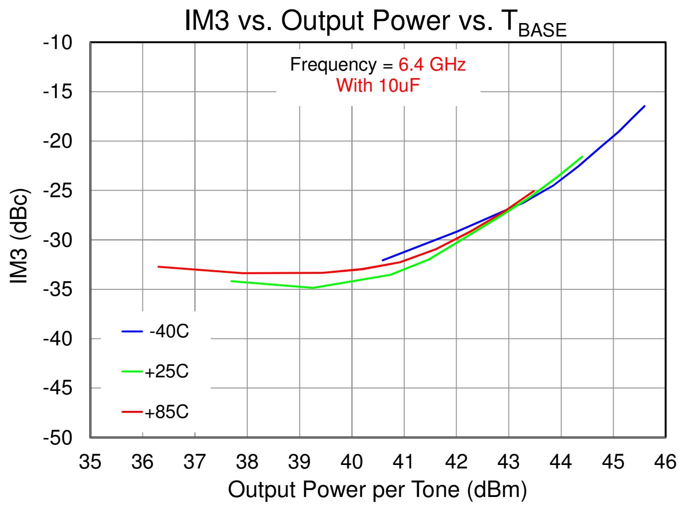


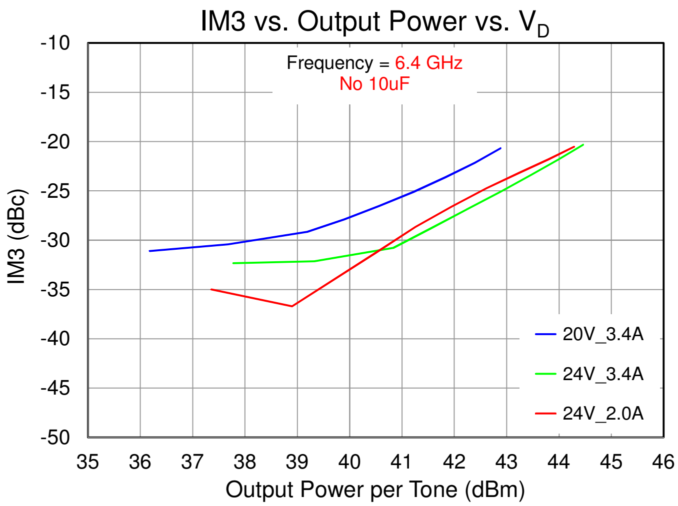


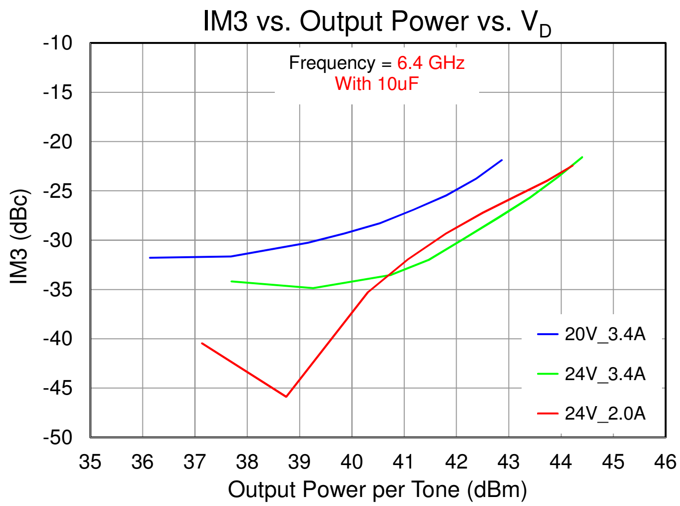
Performance Plots – Large Signal

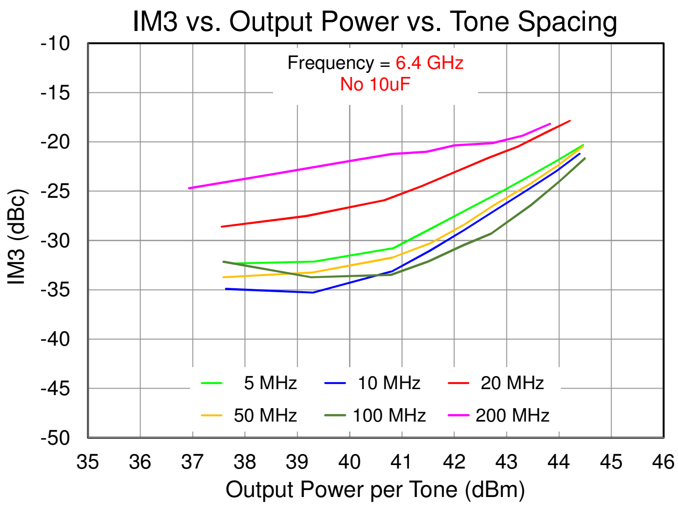
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, Tone Spacing = 5 MHz, T_{BASE} = +25 ºC, with/without 10uF at drain (C9, C12)

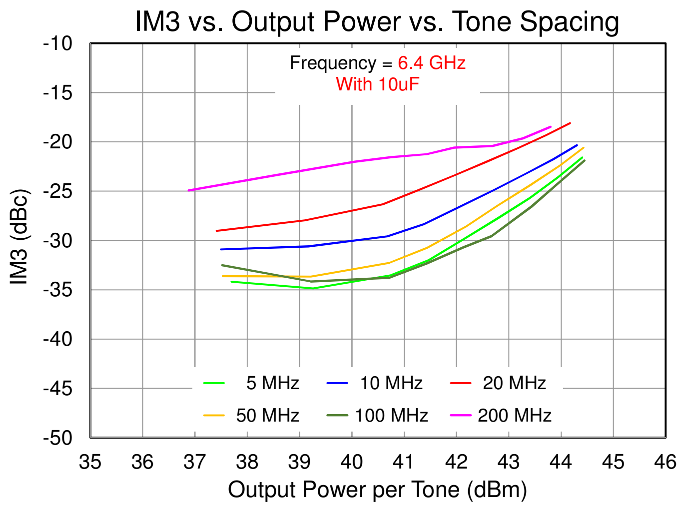








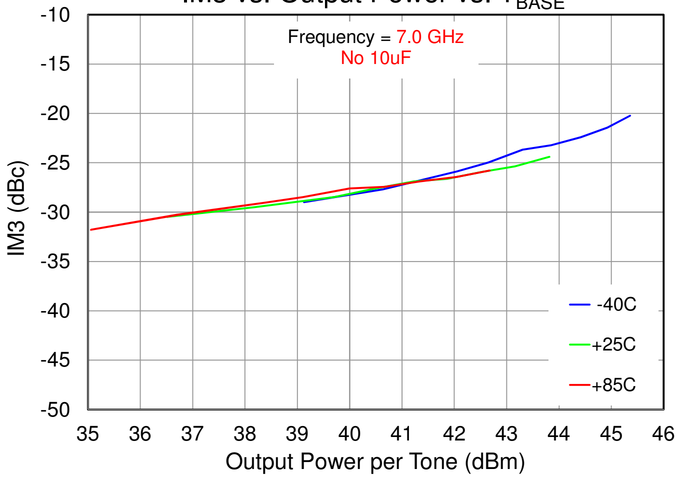




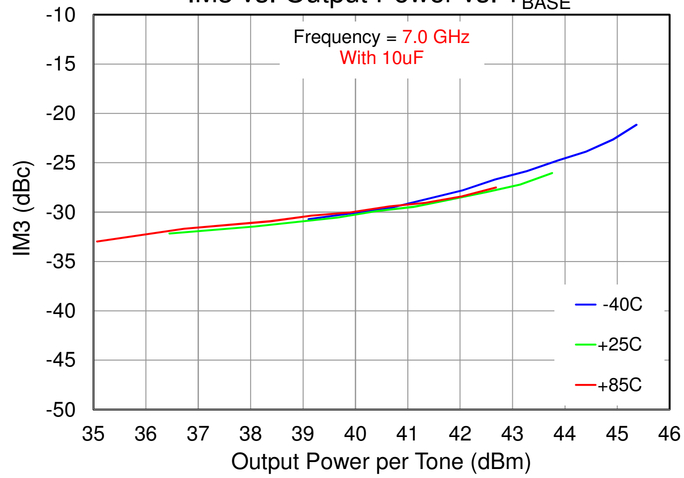
Performance Plots – Large Signal

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, Tone Spacing = 5 MHz, T_{BASE} = +25 ºC, with/without 10uF at drain (C9, C12)

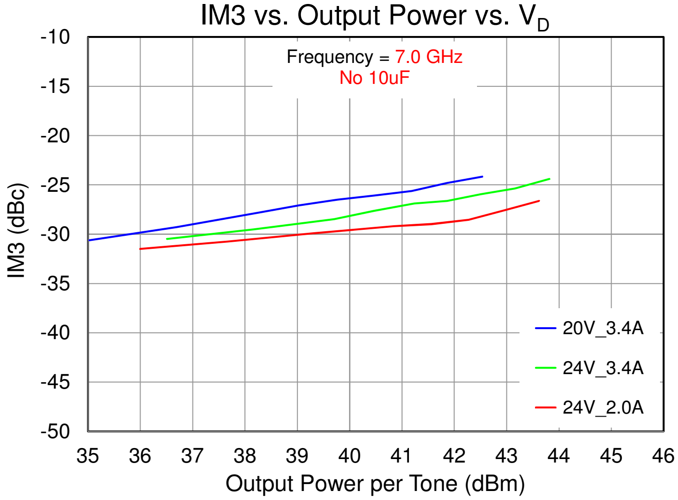
IM3 vs. Output Power vs. T_{BASE}



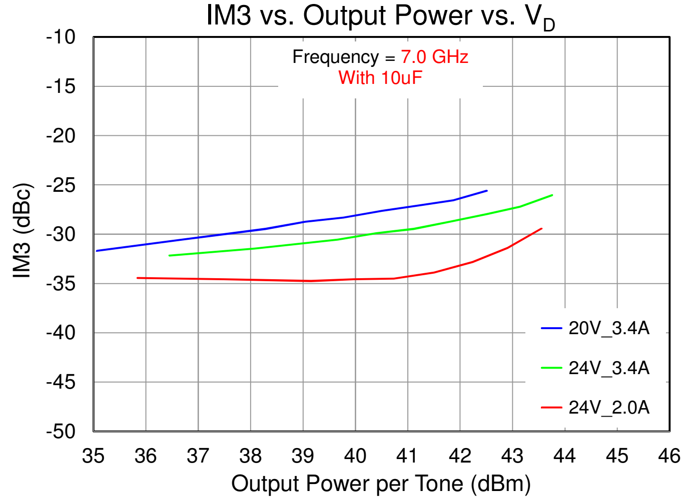
IM3 vs. Output Power vs. T_{BASE}



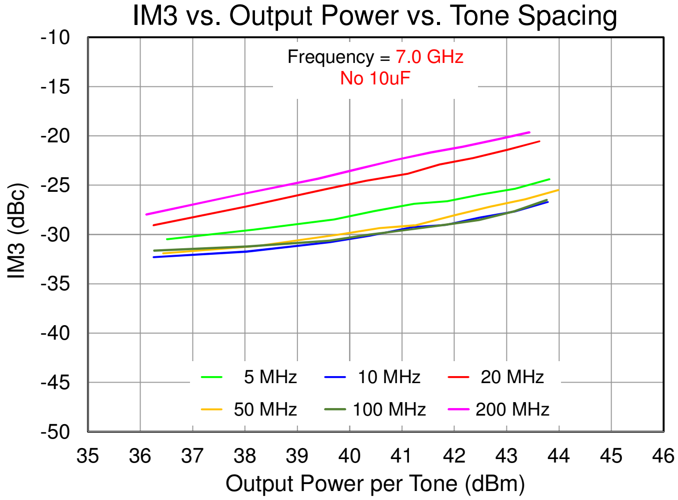
IM3 vs. Output Power vs. V_D



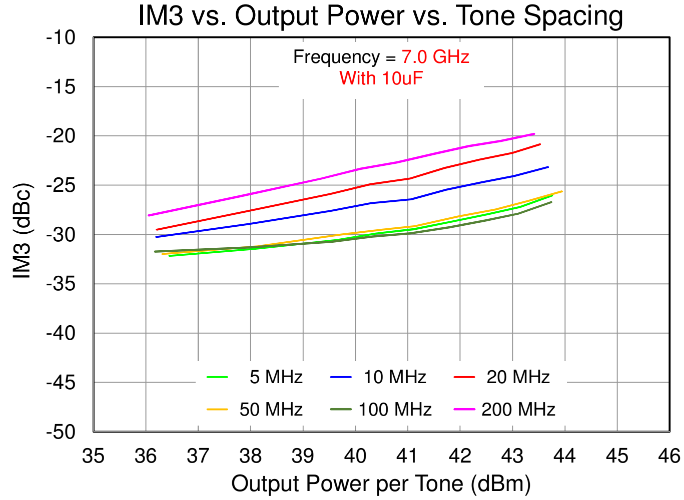
IM3 vs. Output Power vs. V_D



IM3 vs. Output Power vs. Tone Spacing



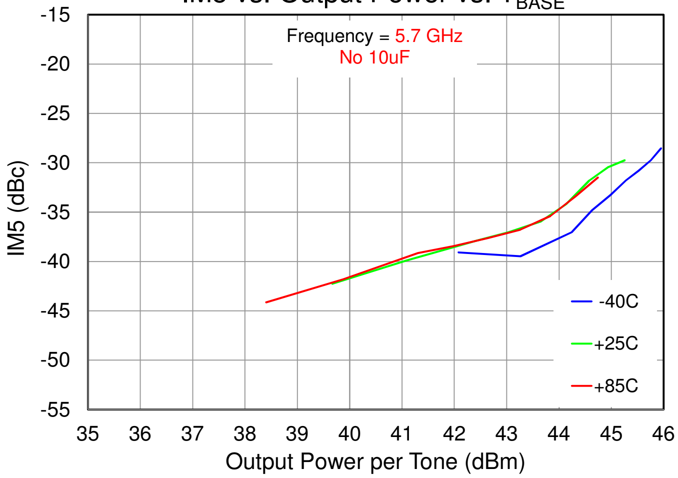
IM3 vs. Output Power vs. Tone Spacing



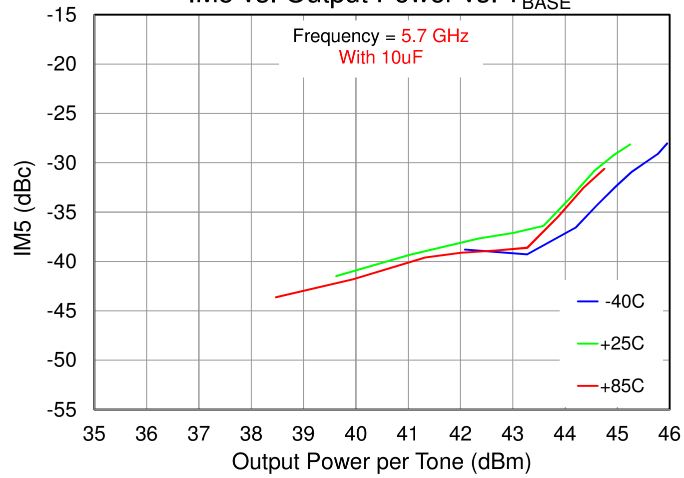
Performance Plots – Linearity

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, Tone Spacing = 5 MHz, T_{BASE} = +25 ºC, with/without 10uF at drain (C9, C12)

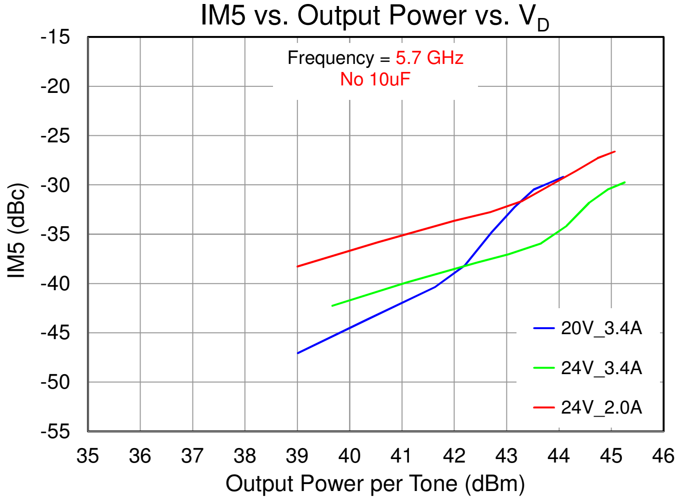
IM5 vs. Output Power vs. T_{BASE}



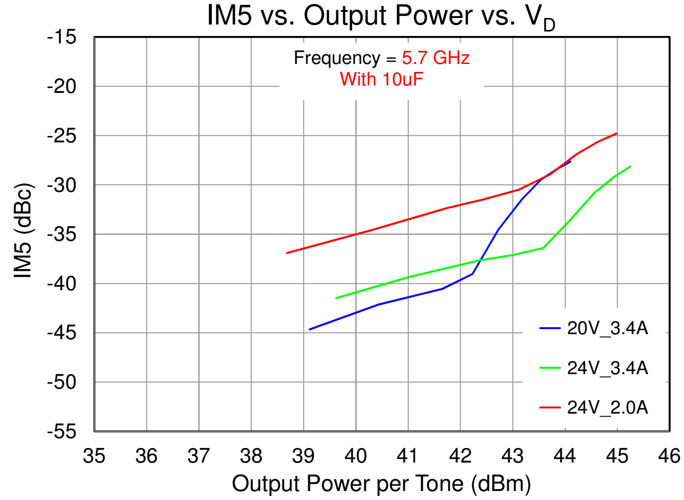
IM5 vs. Output Power vs. T_{BASE}



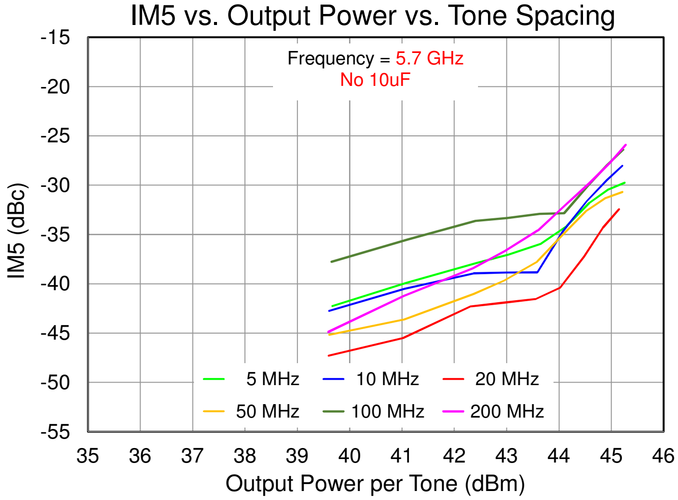
IM5 vs. Output Power vs. V_D



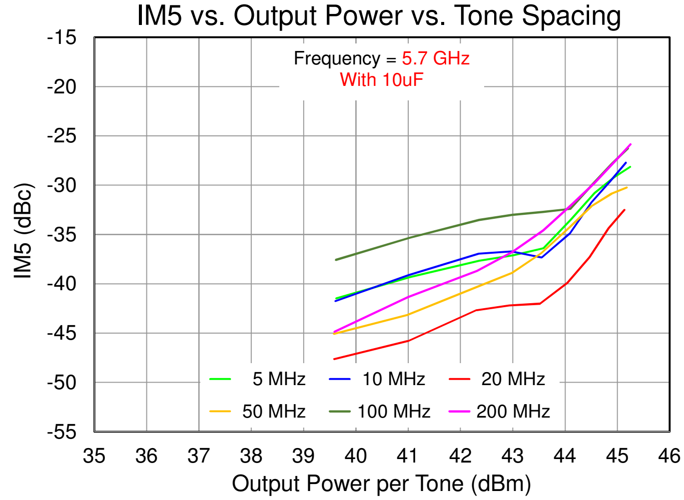
IM5 vs. Output Power vs. V_D



IM5 vs. Output Power vs. Tone Spacing



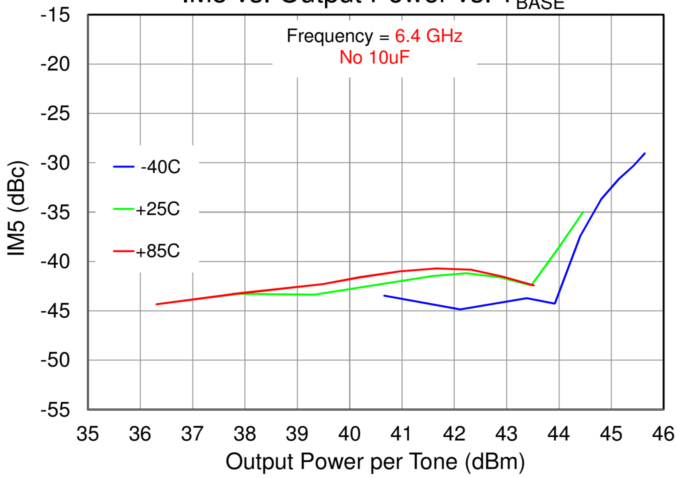
IM5 vs. Output Power vs. Tone Spacing



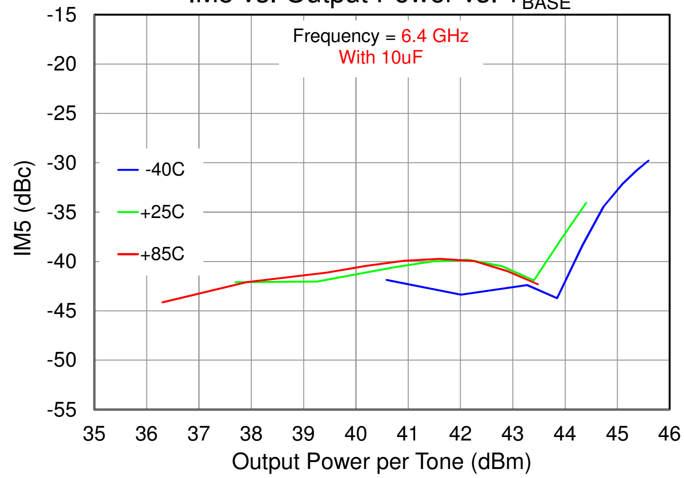
Performance Plots – Linearity

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, Tone Spacing = 5 MHz, T_{BASE} = +25 ºC, with/without 10uF at drain (C9, C12)

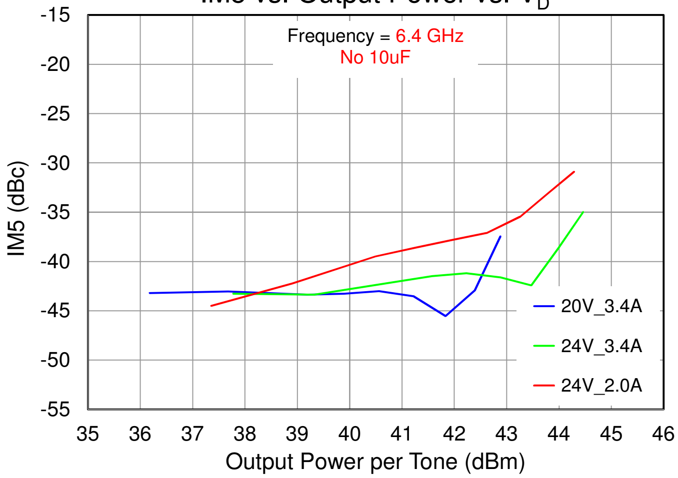
IM5 vs. Output Power vs. T_{BASE}



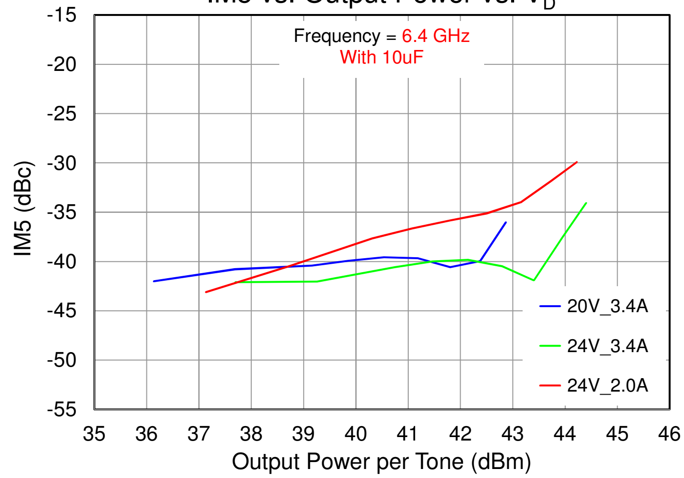
IM5 vs. Output Power vs. T_{BASE}



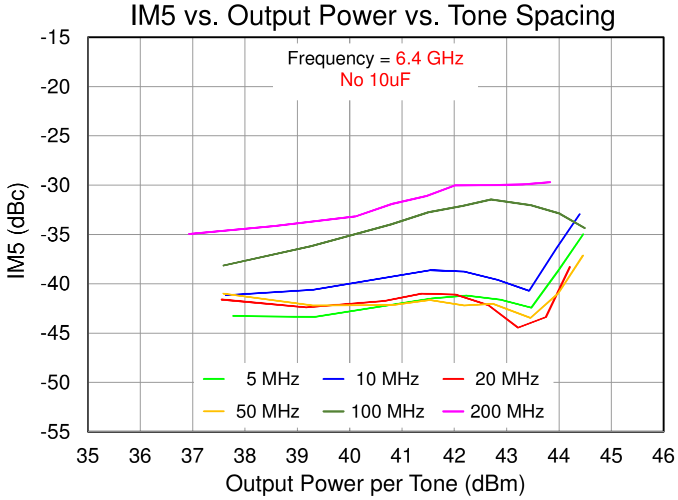
IM5 vs. Output Power vs. V_D



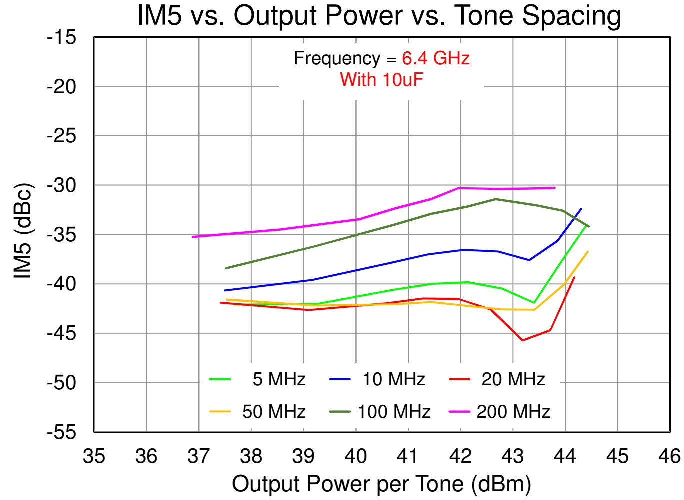
IM5 vs. Output Power vs. V_D



IM5 vs. Output Power vs. Tone Spacing



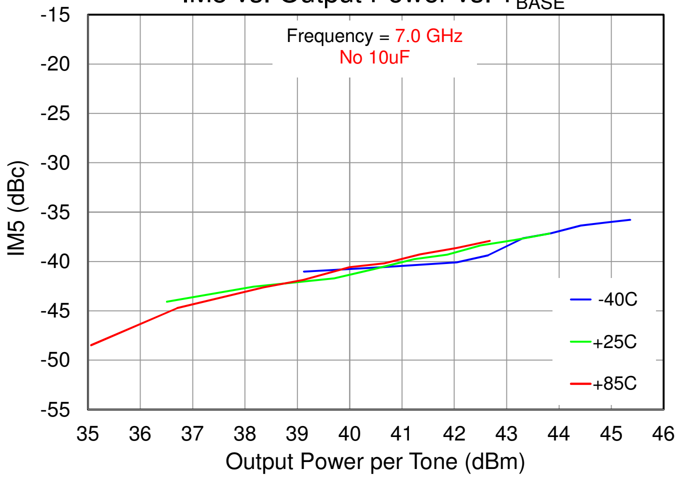
IM5 vs. Output Power vs. Tone Spacing



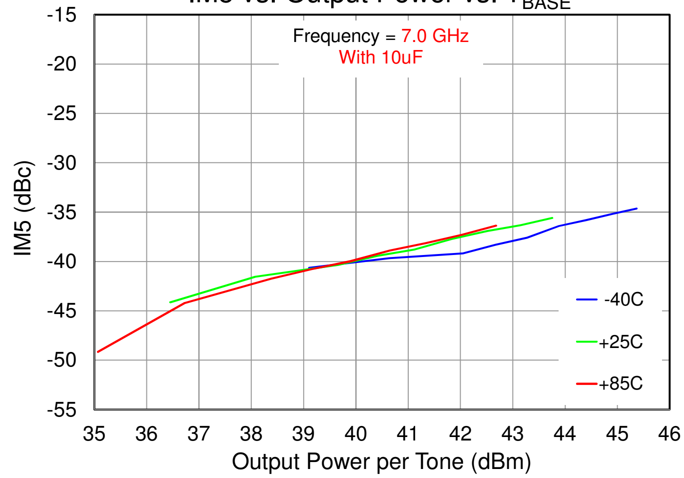
Performance Plots – Linearity

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, Tone Spacing = 5 MHz, T_{BASE} = +25 ºC, with/without 10uF at drain (C9, C12)

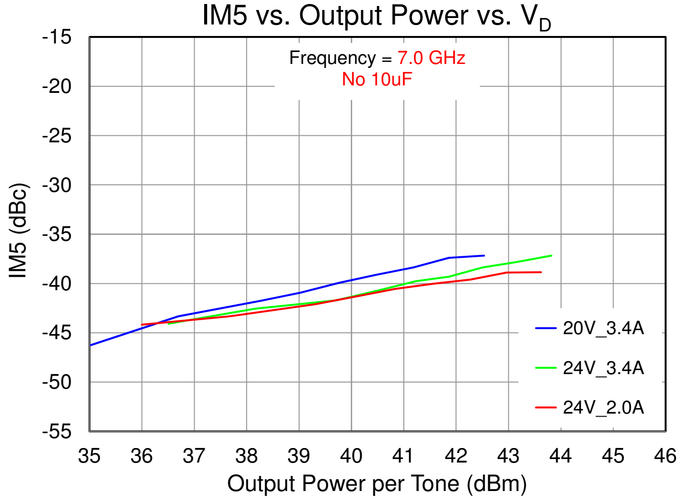
IM5 vs. Output Power vs. T_{BASE}



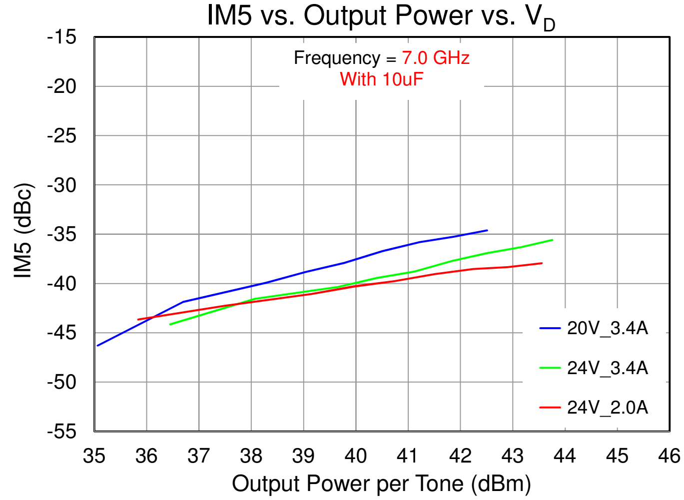
IM5 vs. Output Power vs. T_{BASE}



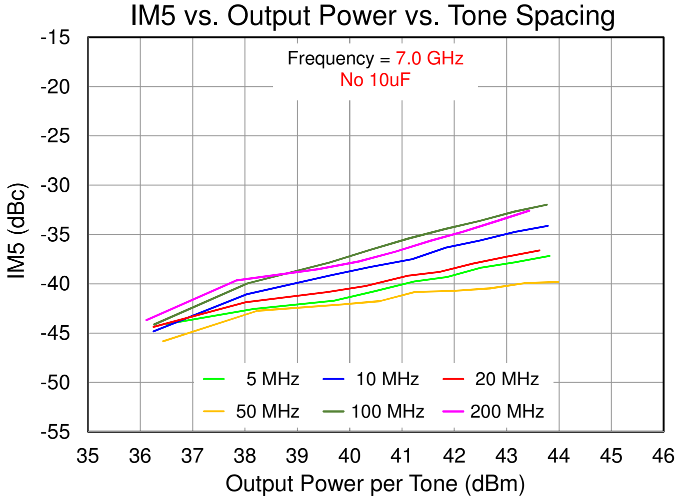
IM5 vs. Output Power vs. V_D



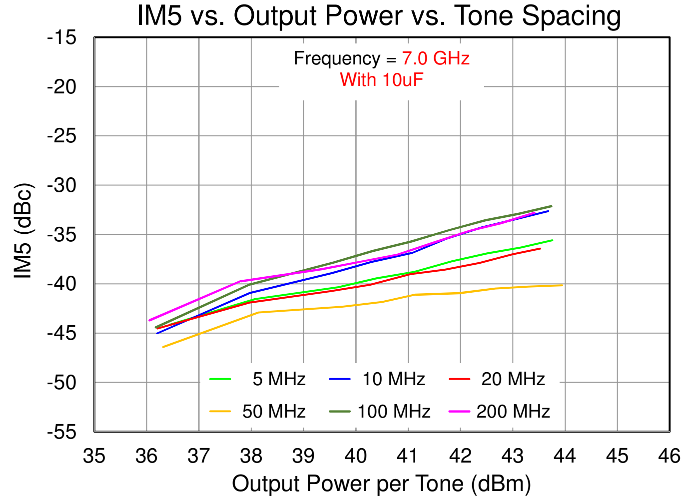
IM5 vs. Output Power vs. V_D



IM5 vs. Output Power vs. Tone Spacing



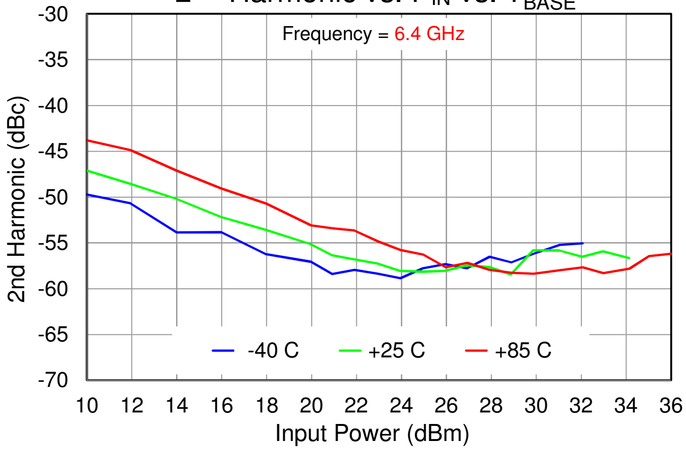
IM5 vs. Output Power vs. Tone Spacing



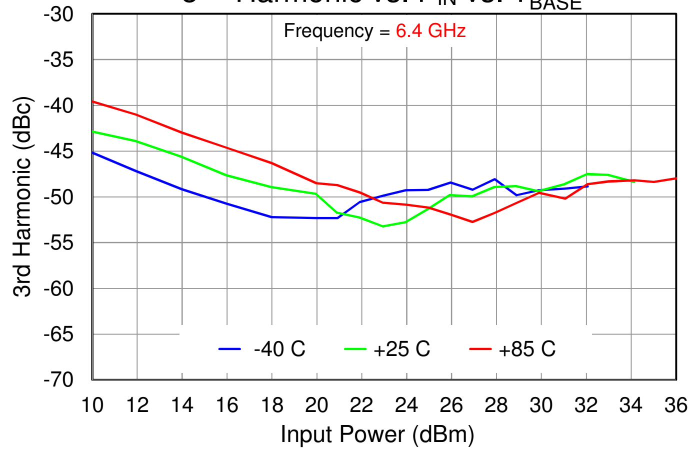
Performance Plots – Harmonics

Test conditions, unless otherwise noted: **Pulsed** V_D = 24 V, I_{DQ} = 3.4 A, Duty Cycle = 20%, PW = 150 us, T_{BASE} = +25 ºC

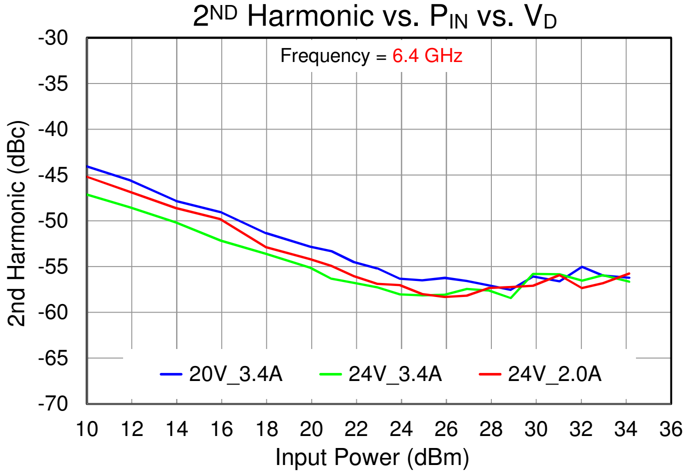
2ND Harmonic vs. P_{IN} vs. T_{BASE}



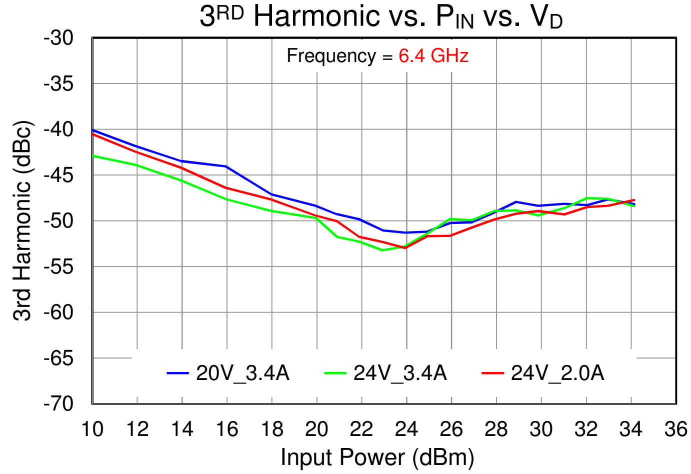
3RD Harmonic vs. P_{IN} vs. T_{BASE}



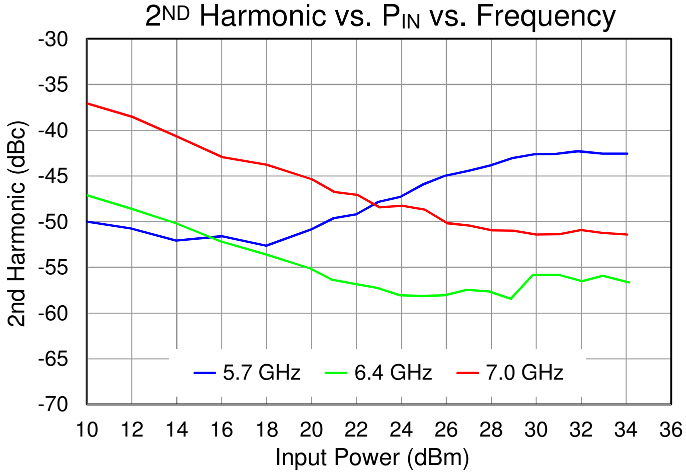
2ND Harmonic vs. P_{IN} vs. V_D



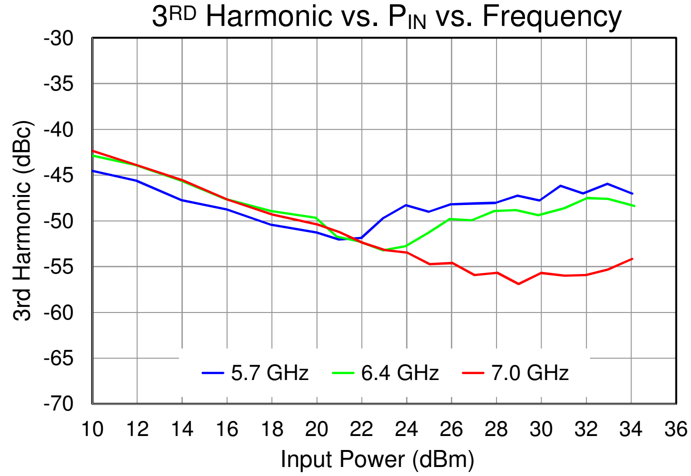
3RD Harmonic vs. P_{IN} vs. V_D



2ND Harmonic vs. P_{IN} vs. Frequency

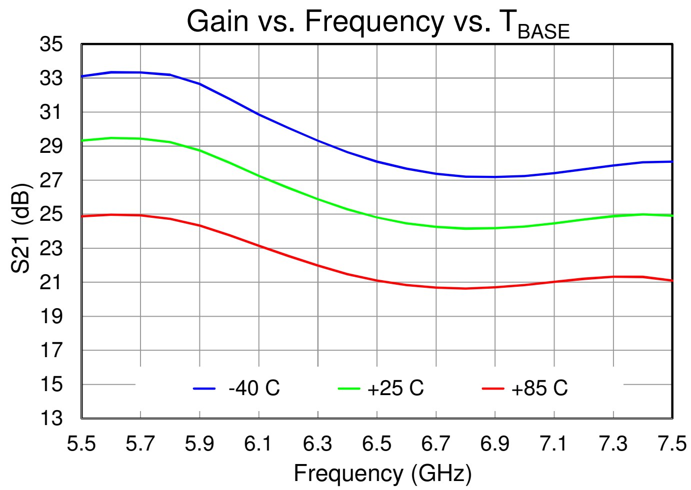


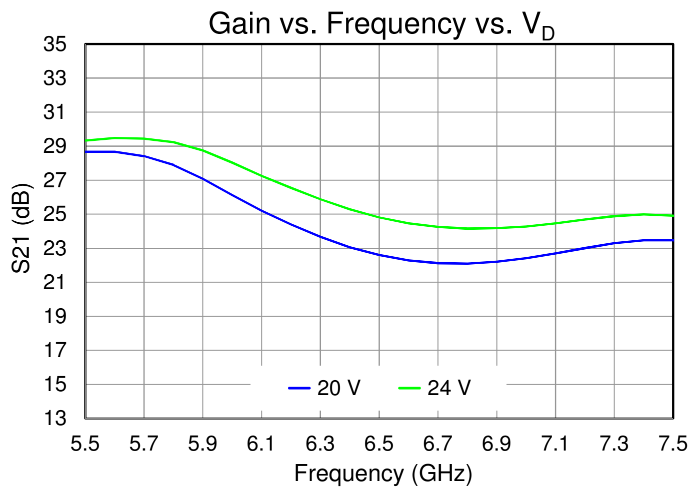
3RD Harmonic vs. P_{IN} vs. Frequency

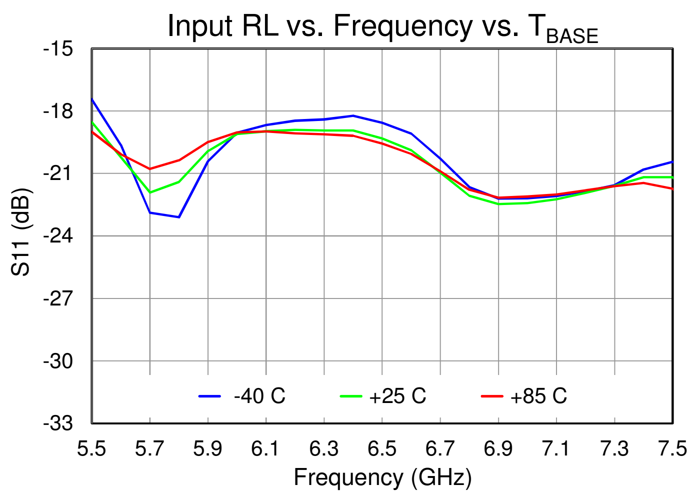


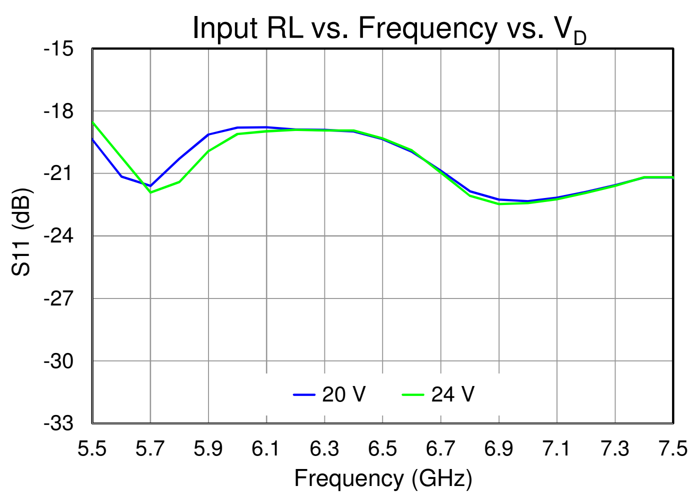
Performance Plots – Small Signal

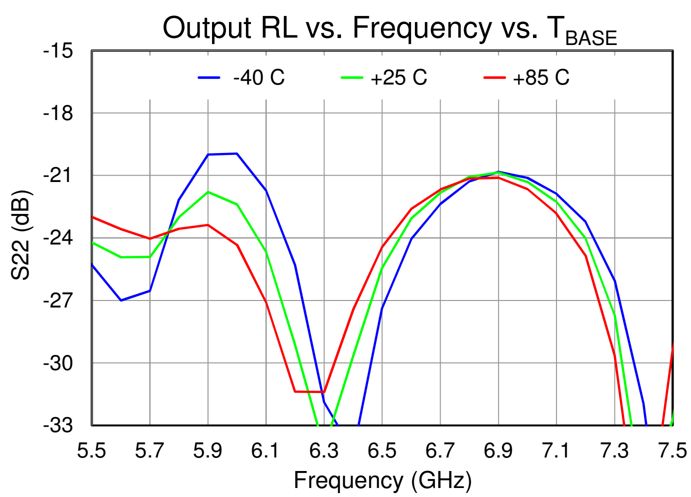
Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, T_{BASE} = +25 ºC

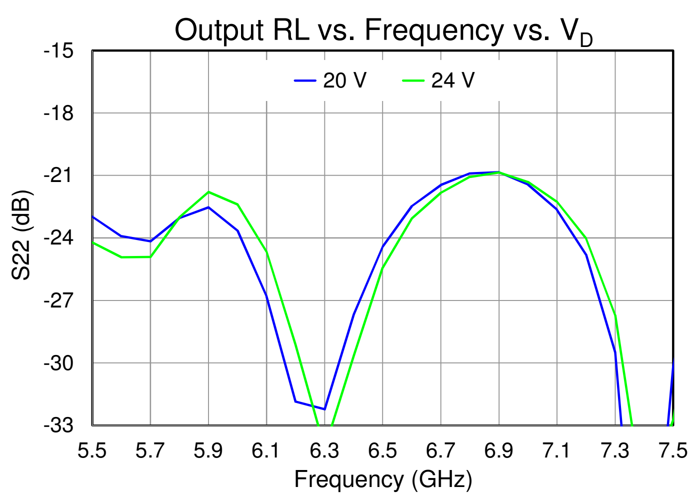






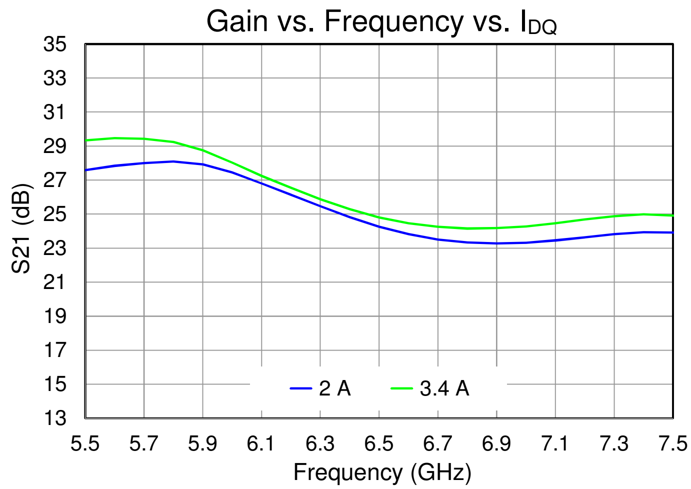


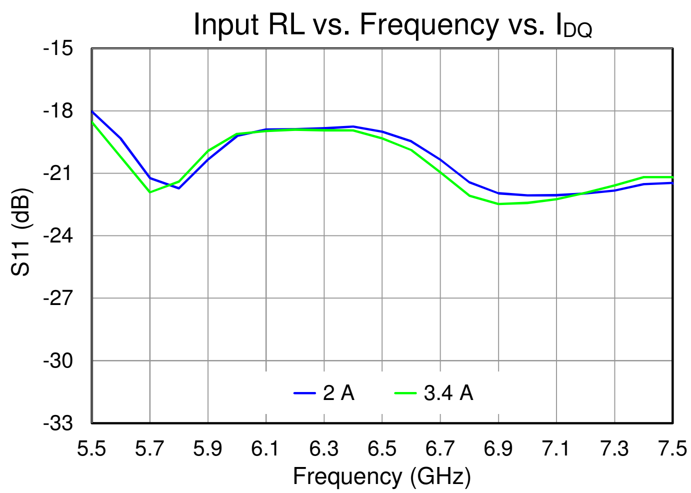


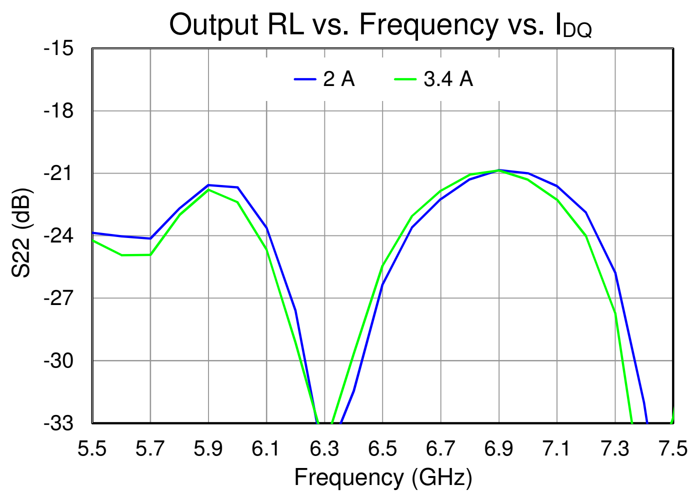


Performance Plots – Small Signal

Test conditions, unless otherwise noted: **CW** V_D = 24 V, I_{DQ} = 3.4 A, T_{BASE} = +25 ºC







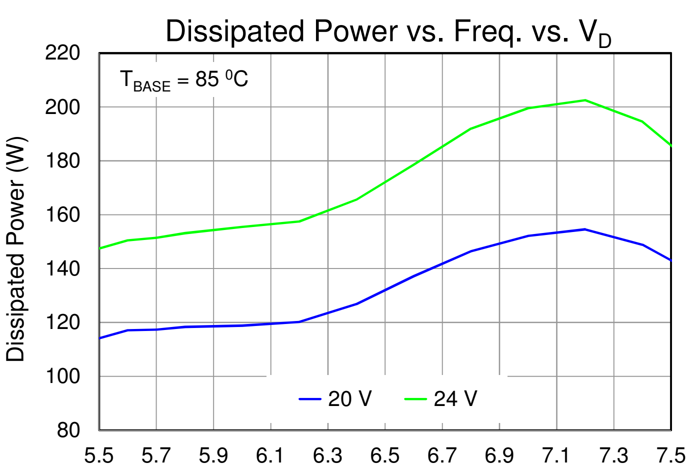
Thermal and Reliability Information

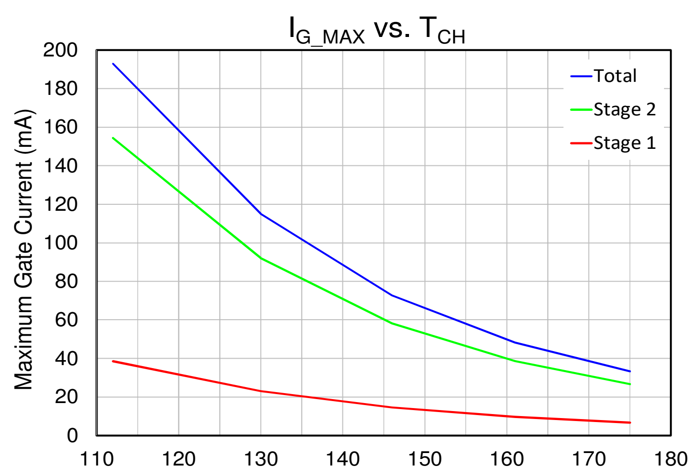
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent T_{base} = 85 °C, V_D = 24 V, I_{DQ} = 3.4 A P_{DISS} = 81.6 W	0.40	ºC/W
Channel Temperature, T_{CH} (2)		118	°C
Thermal Resistance, θ_{JC} (1)	Pulsed, T_{base} = 85 °C, V_D = 24 V, I_{DQ} = 3.4 A, Freq = 7 GHz, I_{D_Drive} = 13 A, DC = 20%, PW = 150 us, P_{IN} = 32 dBm, $P_{OUT,SAT}$ = 50.3 dBm P_{DISS} = 206 W	0.25	ºC/W
Channel Temperature, T_{CH} (2)		137	°C
Thermal Resistance, θ_{JC} (1)	CW, T_{base} = 85 °C, V_D = 24 V, I_{DQ} = 3.4 A, Freq = 7 GHz, I_{D_Drive} = 9 A, P_{IN} = 28 dBm, P_{OUT} = 46 dBm P_{DISS} = 177 W	0.43	ºC/W
Channel Temperature, T_{CH} (2)		161	°C

Notes:

1. Thermal resistance determined to the back of package (85 °C)
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note "GaN Device TCHMAX Theta-JC and Reliability Estimates," located here https://www.qorvo.com/products/d/da006480

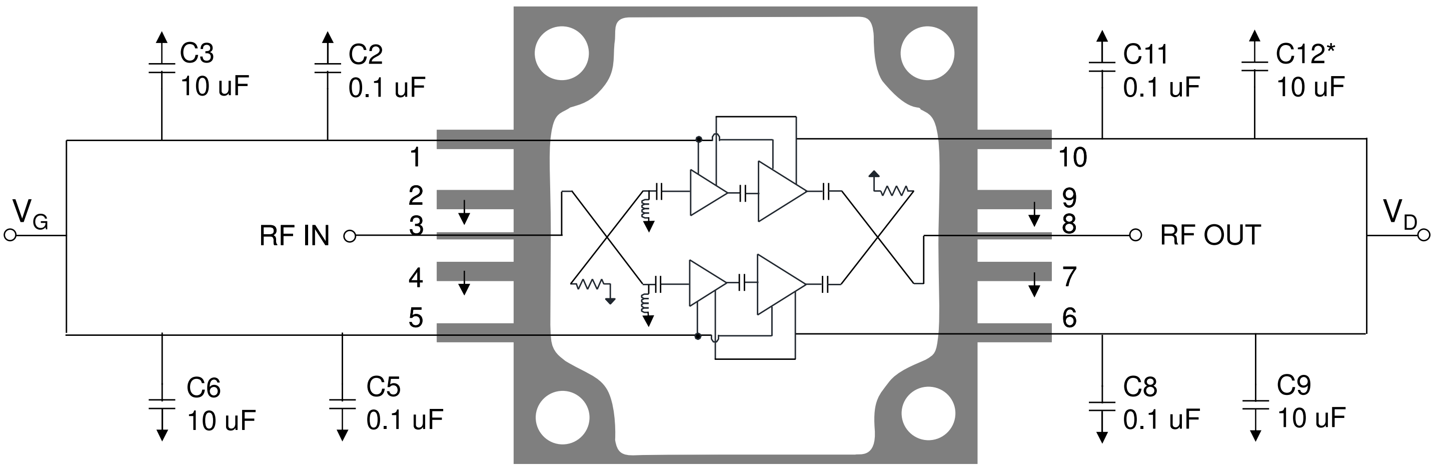
Dissipated Power and Maximum Gate Current





Test conditions, unless otherwise noted: Pulsed, V_D = 24 V, I_{DQ} = 3.4 A, P_{IN} = +32 dBm, T_{BASE} = +85 ºC

Applications Information



*C9, *C12: optional, to optimize linearity depending tone spacing, not populated on Qorvo's EVB, see performances on page 9 – 14

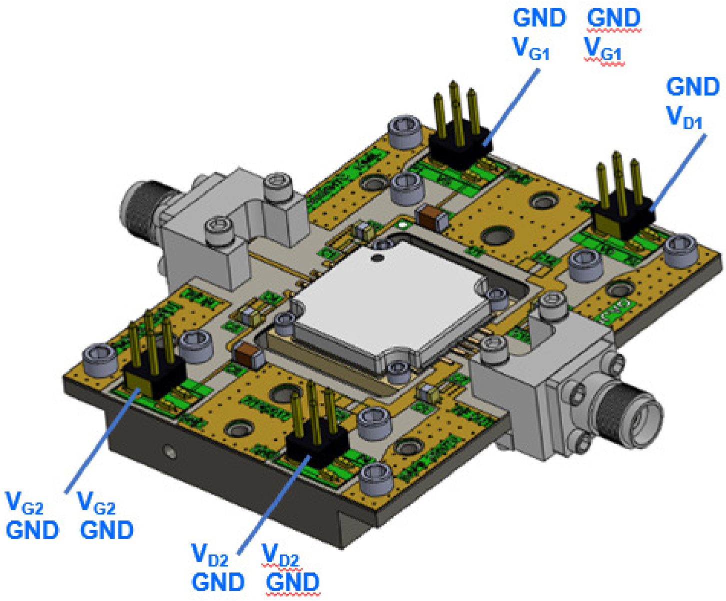
Bias-Up Procedure

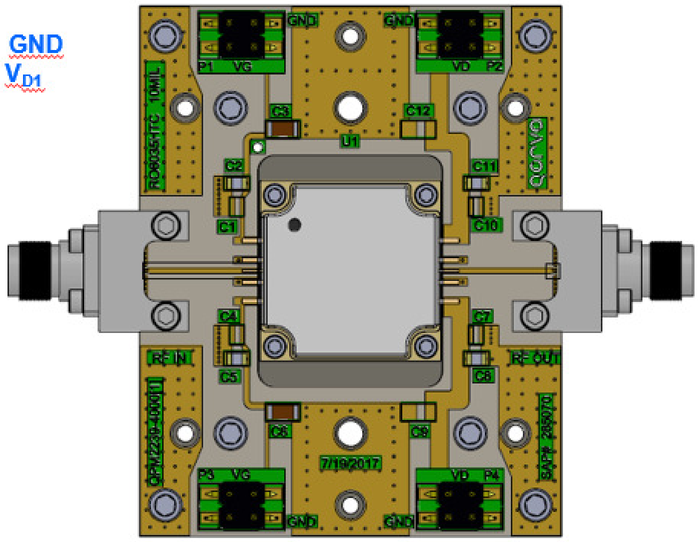
1. Set I_D limit to 18 A, I_G limit to 180 mA
2. Set V_G to –5.0 V
3. Set V_D +24 V
4. Adjust V_G more positive until I_{DQ} = 3.4 A ($V_G \approx$ -2.5V +/- typical)
5. Apply RF signal

Bias-Down Procedure

1. Reduce V_G to –5.0 V. Ensure I_{DQ} ~ 0 mA
2. Set V_D to 0 V
4. Turn off RF signal
5. Turn off V_D supply
6. Turn off V_G supply

Evaluation Board (EVB) Layout Assembly

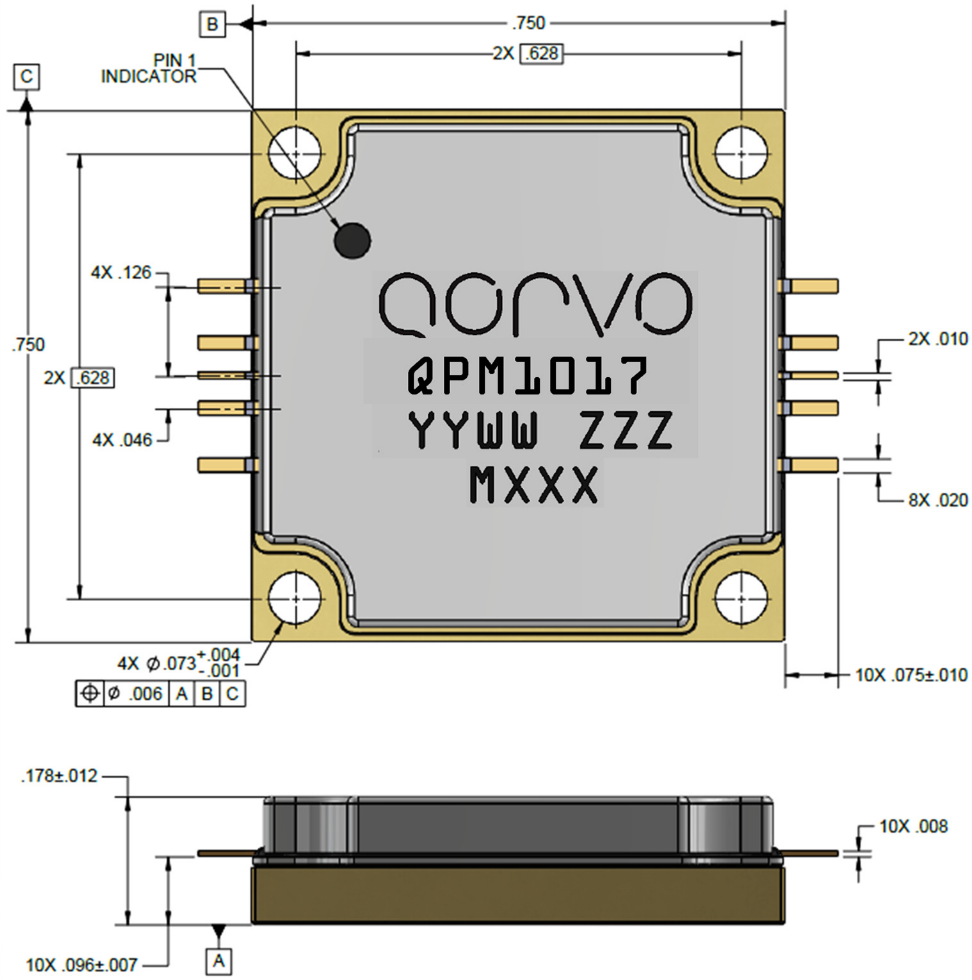




Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
U1	-	100W C-Band GaN Power Amplifier Module	Qorvo	QPM1017
C2, C5, C8, C11	0.1 uF	CAP, 0.1uF, ±10%, 50V, X7R, 0805	Various	
C3, C6	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	Various	
C9, C12	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206 Optional, to optimize linearity depending tone spacing, see page 19 for recommendation, not populated on Qorvo EVB.	Various	
H1, H2, H3, H4	-	CONN, HDR, 4 POS, 2 RAW, SMD, Au	Various	
J1, J2	-	Connector, Female, End Launch, 1092-02A-5	Southwest Microwave	1092-02A-5
S1 – S8		Screw, Cap, Socket Head, 2-56X1/8”	Various	
S9 – S12		Screw, Cap, Socket Head, 0-80X3/32”	Various	
PCB	-	PCB, Rogers 6035 10mils, 1oz Ni/Au plating 2 sides	Various	Custom
H-Block	-	H-Block, Copper C110, 1.744x 2.201 x 0.275T	Various	Custom
Solder		Paste, solder, Syntech, Sn62/Pb36/Ag2	Inventec Performance Chemicals USA	Syntech, SN62, T3, 90.5, 250J
Epoxy		Epoxy, Ablebond 84-1LMI 3cc	Henkel Corporation	84-1LMI
Thermal Compound	-	CHEM, Thermal Compound, Silver 5GR	Artic Silver	Artic Silver 5 AS5-3.5G

Mechanical Information



NOTES:
1. MATERIALS
   PACKAGE BASE: COPPER
   LEADS: ALLOY 194
   LID: PLASTIC
   FINISH: GOLD
2. PART IS EPOXY SEALED
3. UNITS: INCHES
4. TOLERANCES (UNLESS NOTED):
   .XX = ± .01
   .XXX = ± .005
5. MARKINGS
   PART NUMBER: QPM1017
   WORK YEAR: YY
   WORK WEEK: WW
   SERIAL NUMBER: ZZZ
   BATCH ID: MXXX

Pin Description

Pin No.	Symbol	Description
1	V_{G1}	Gate voltage Amp 1. External bypassing required; refer to page 19 for recommendation
2, 4, 7, 9	Ground	Must be grounded to PCB
3	RF_{IN}	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
5	V_{G2}	Gate voltage Amp 2. External bypassing required; refer to page 19 for recommendation
6	V_{D2}	Drain voltage Amp 2. External bypassing required; refer to page 19 for recommendation
8	RF_{OUT}	RF Output. Matched to 50 Ω, DC blocked
10	V_{D1}	Drain voltage Amp 1. External bypassing required; refer to page 19 for recommendation

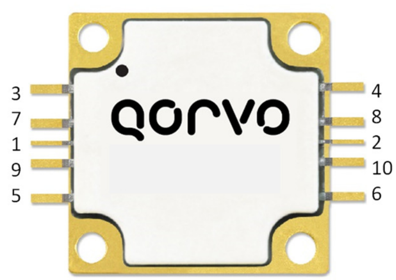
Assembly Notes

1. Carefully clean the PC board, base plate, and package leads with alcohol. Allow it to dry fully.

2. To improve the thermal and RF performance, Qorvo recommends attaching a heat sink to the bottom of the package and apply either a thermal compound (Arctic Silver 5 recommended) or a .004 inch (maximum thickness) Indium shim between the heat sink and the package. Refer to the applications note Application of Arctic Silver 5 Thermal Compound and Indium Shims for Qorvo CP-style Packaged Components for more information.

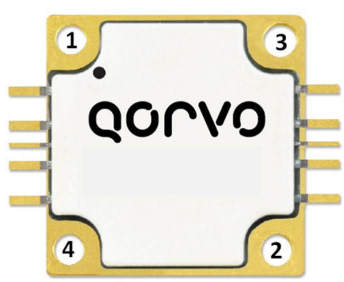
3. The component leads should be manually soldered. Apply a low residue solder alloy meeting J-STD-001 (ROL0, ROL1 or equivalent) with a liquidus temperature below 220 °C to each pin of the TGA/QPA/QPMxxxx. The use of low residue/no-clean flux (ROL0, ROL1) is recommended. The package lead temperature should not exceed 260 deg C. Each solder connection should be completed within 2 to 5 seconds. Adding flux during hand soldering of the component leads with localized spot cleaning is acceptable. Soldering irons meeting the requirements of J-STD-001, Appendix A are acceptable.

4. The leads should be soldered in a staggered or star pattern from side to side, and never solder two adjacent leads. This allows the heat to dissipate on each lead, and not cause the adjacent leads to become de-soldered and damaged or displaced.



5. The packaged part should not be subjected to conventional SMT automated solder reflow processes.

6. (The following is for information only. There are many variables in a second level assembly that Qorvo does not control, so Qorvo does not recommend an absolute torque value.) Use screws to attach the component to the heat sink. A suggested final torque value is 16 in-oz. for a 0-80 screw. Start with screws finger tight, then torque to 8 in-oz., then torque to final value. Use the following tightening pattern:



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C2a	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	N/A	Blank, null, no content

Caution!

ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: **1-844-890-8163**

Email: customer.support@qorvo.com

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