APPLICATION NOTE

PAC55XX PCB Design and Layout Guidelines

Power Application Controller®

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OVERVIEW

BLDC and PMSM applications for consumer and industrial applications is a growing market for inverter-based solutions. These applications often require high-performance control with high-power at high frequencies in a compact size. The PAC55XX family of Power Application Controllers® are an ideal solution for this type of system, due to their high analog integration and high-performance control.

Systems like this with a small form factor, but with high-power and high-frequency components, require special attention to the system design and layout. A poorly designed PCB can lead to bad application performance as well as other issues such as difficulty passing Electromagnetic Interference (EMI) testing.

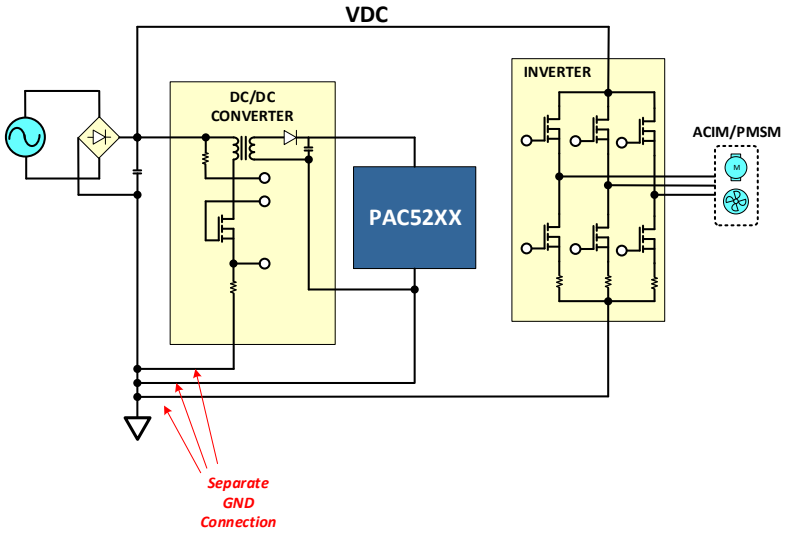
This document provides an overview of the design and layout guidelines, as well as strategies for reducing EMI in designs based on the PAC55XX family of controllers.

GROUNDING

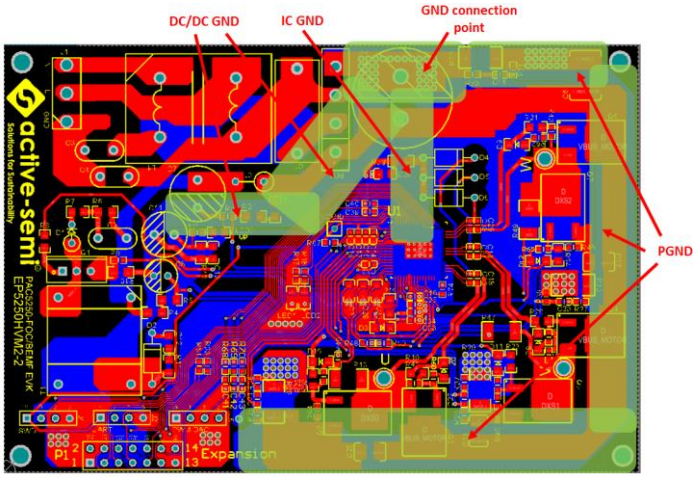
Typical BLDC motor systems implemented with the PAC55XX controller have three different types of grounds for the PCB:

- IC GND – The ground connection to the IC
- DC/DC GND – The ground connection to the DC/DC
- PGND – The ground connection to the inverter

In the design, each of these grounds should be isolated from each other. The three grounds should be connected in a star configuration connected at the main power supply bus capacitor as shown in the diagram below.



As an example, in the PCB layout shown below you can see from the diagram below how the three grounds are connected in a star at the DC/DC bus capacitor.

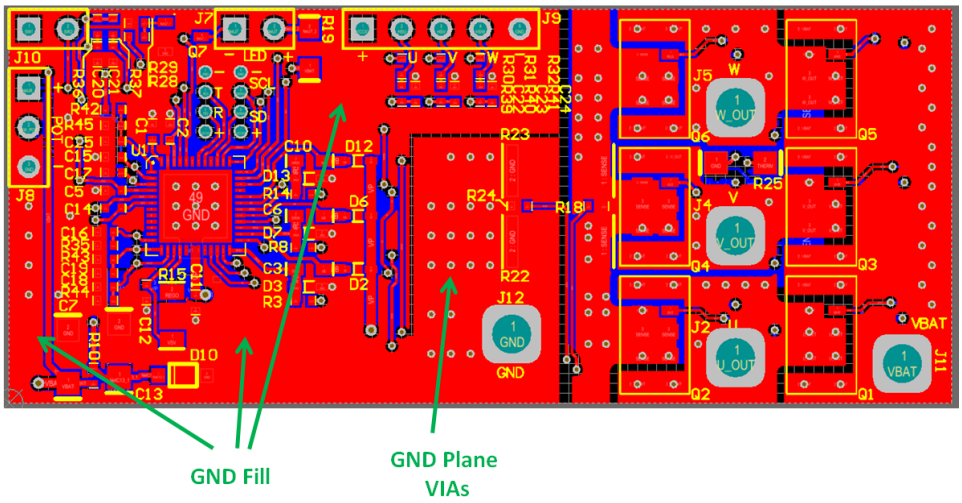


GROUND FILL

In unused areas of the PCB, it is beneficial to fill them with copper connected to the GND plane. This is especially beneficial under high-frequency signals.

Throughout the ground fill, it is helpful to provide enough vias for ground plane connections between layers of the PCB. This allows the energy to flow through multiple paths to the common ground reference, which provides a low impedance path and reduces parasitic components.

The diagram below shows an example based on the EP5223PT reference design for power tool applications.



As shown in this layout, available area on the top and bottom layers (red and blue, respectively) is filled with copper for ground. These ground planes are connected with vias to maximize the benefit of the overall ground plane on both layers.

POWER PAD CONSIDERATIONS

The PAC family of controllers all have power pads on the bottom of the packaged products to help with grounding and thermal resistance.

It is highly recommended using multiple vias inside the thermal pad area to conduct heat from the top layer to the inner or bottom layers. Correct layout of these vias greatly improves the thermal characteristics of the IC as well as electrical performance.

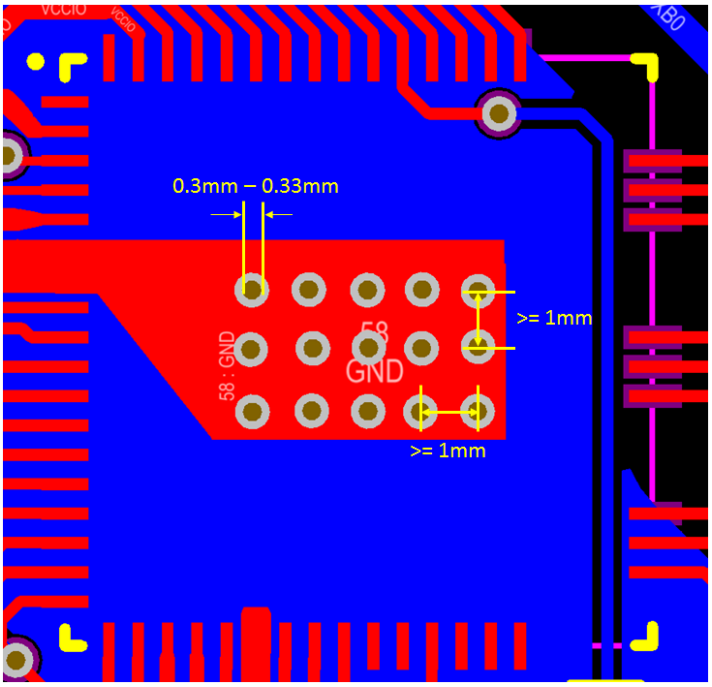
The recommended via pitch and diameter for thermal pad area vias are:

- Pitch: Minimum of 1mm
- Hole diameter: 0.3mm to 0.33mm

The design should include as many vias to ground as can fit, based on the pitch and diameter requirements above.

When designing the footprint for the PAC, the copper area for the pad should match the size of the power pad on the IC to maximize grounding between the IC and PCB.

The diagram below shows an example of the power pad thermal vias.



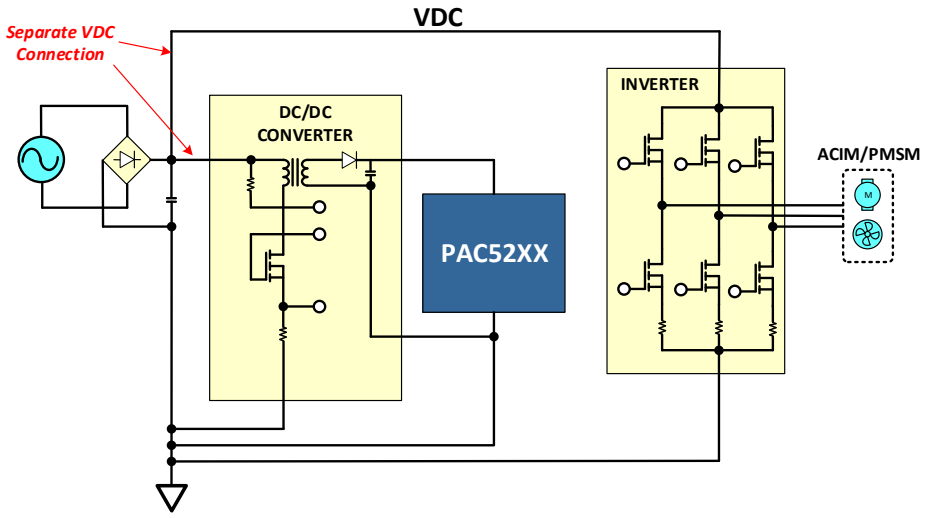
For guidelines on design and layout using Active-Semi products with QFN packages, see the following application note available on http://www.active-semi.com:

PCB Layout Guidelines for QFN Package (AN-104)

POWER SUPPLY DESIGN

In most motor control applications, the main bus power supply serves as the input for the DC/DC converter as well as for the inverter. This supply is typically referred to as VBUS or VDC.

It is recommended to have separate connections for the supply to the DC/DC and the supply to the inverter, as shown below.



POWER DECOUPLING CAPACITORS

The PAC55XX family of controllers generates several power supplies internally to supply the IC and system.

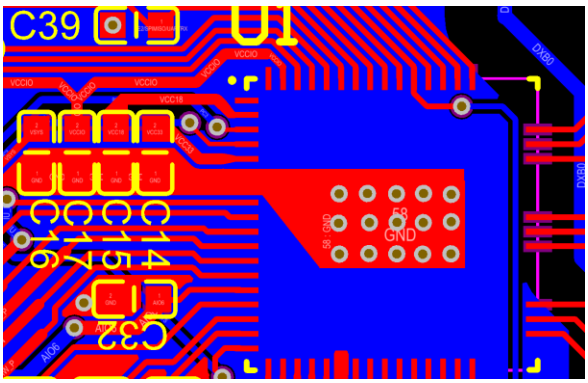
The PAC55XX contains the following power supplies that are internally generated[1]:

- **VSYS** – 5V system supply
- **VCC18** – 1.8V core supply
- **VCCIO** – 3.3V/5V IO supply
- **VCC33** – 3.3V ADC supply

Each of these power supplies should be bypassed to ground via decoupling capacitors.

Each decoupling capacitors should be placed as close as possible to the IC, and routed with the shortest trace possible. There should also be generous copper for these connections. This will help reduce any parasitic components that could cause ringing and other emissions such as electromagnetic interference (EMI).

In the diagram below the decoupling capacitors are shown as components C14 – C17. Note the traces and copper from the IC pins and power pad to these decoupling capacitors in this example.

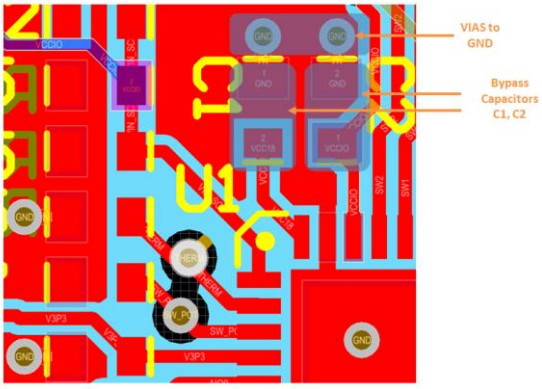


In the example above, the IC has a ground pin that is used for the copper polygon connecting the bypass capacitors to the power pad. The power pad has several vias to the ground plane to decrease impedance to the ground plane.

[1] Note that other PAC family members may have different LDOs, but the guidelines for bypass layout are the same.

Some PAC55XX products do not have pins for ground and must perform all grounding of bypass capacitors through using vias between the copper polygons and ground plane.

The diagram below shows a portion of an example layout that does not have ground pins:

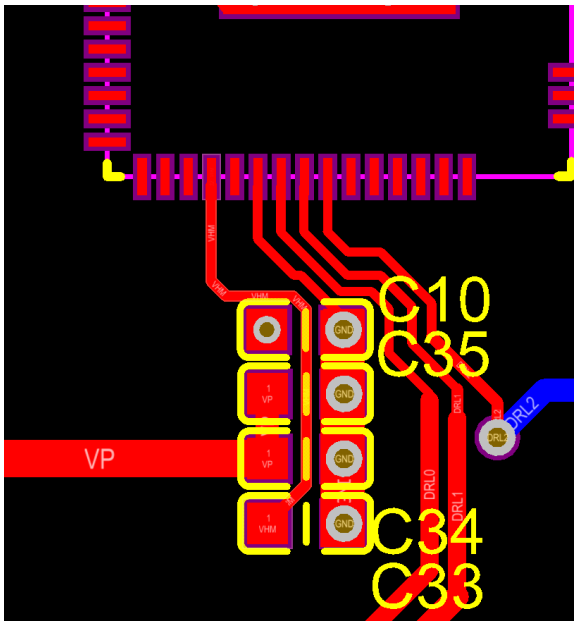


In addition to **VSYS**, **VCC18**, **VCCIO** and **VCC33** supplies, the PAC55XX also contains a DC/DC controller to convert the bus voltage to a system voltage from 9V to 15V to power the IC as well as supply the gate driver.

The DC/DC has the following power supply signals that also need to be bypassed:

- **VHM** – DC/DC Input (C33)
- **VP** – DC/DC Output (C34, C35)

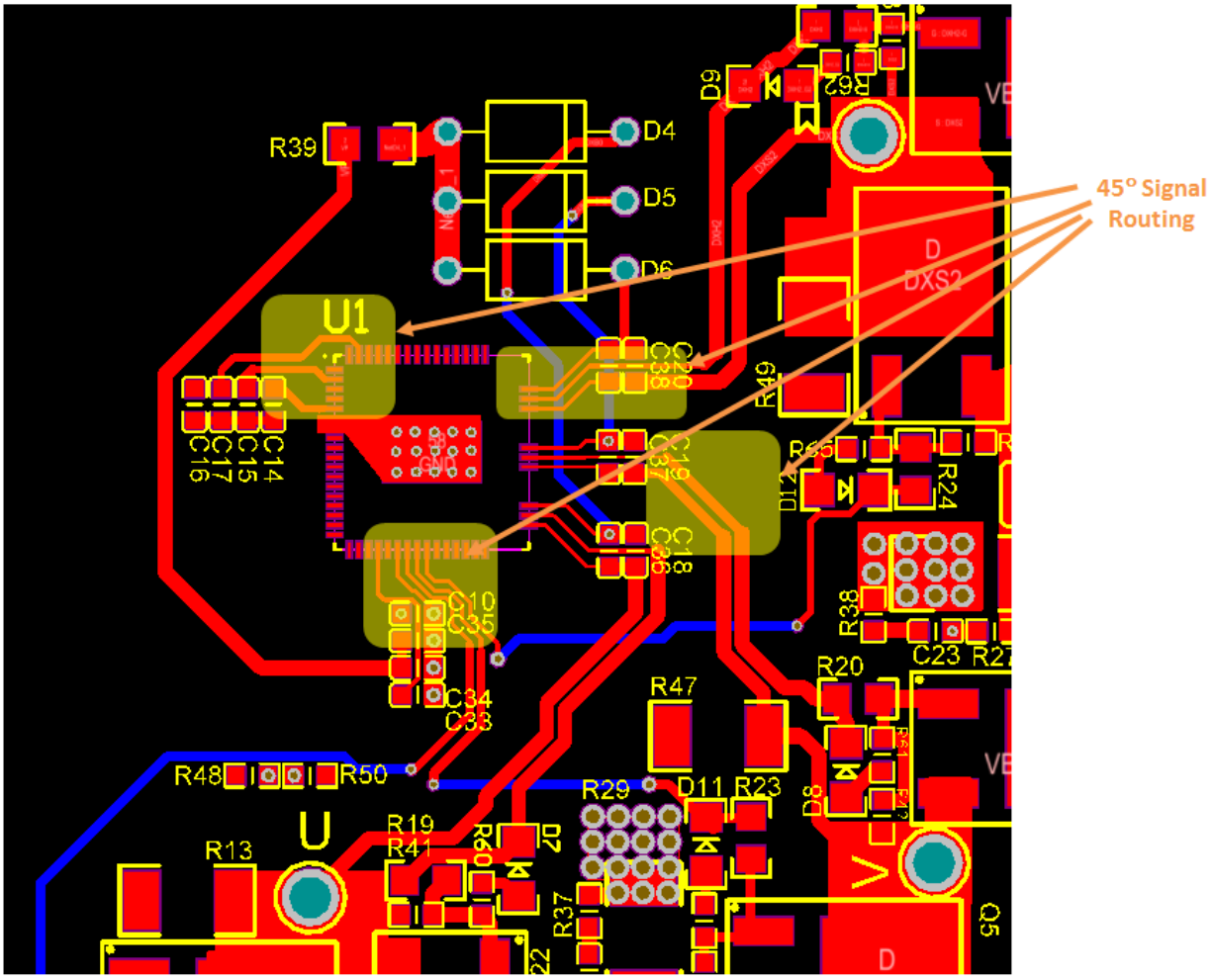
Like with the LDO decouple capacitors above, these also need to be placed as close as possible to the IC, with as much copper as possible connecting to the IC and to ground to reduce any parasitic components.



ROUTING SIGNALS

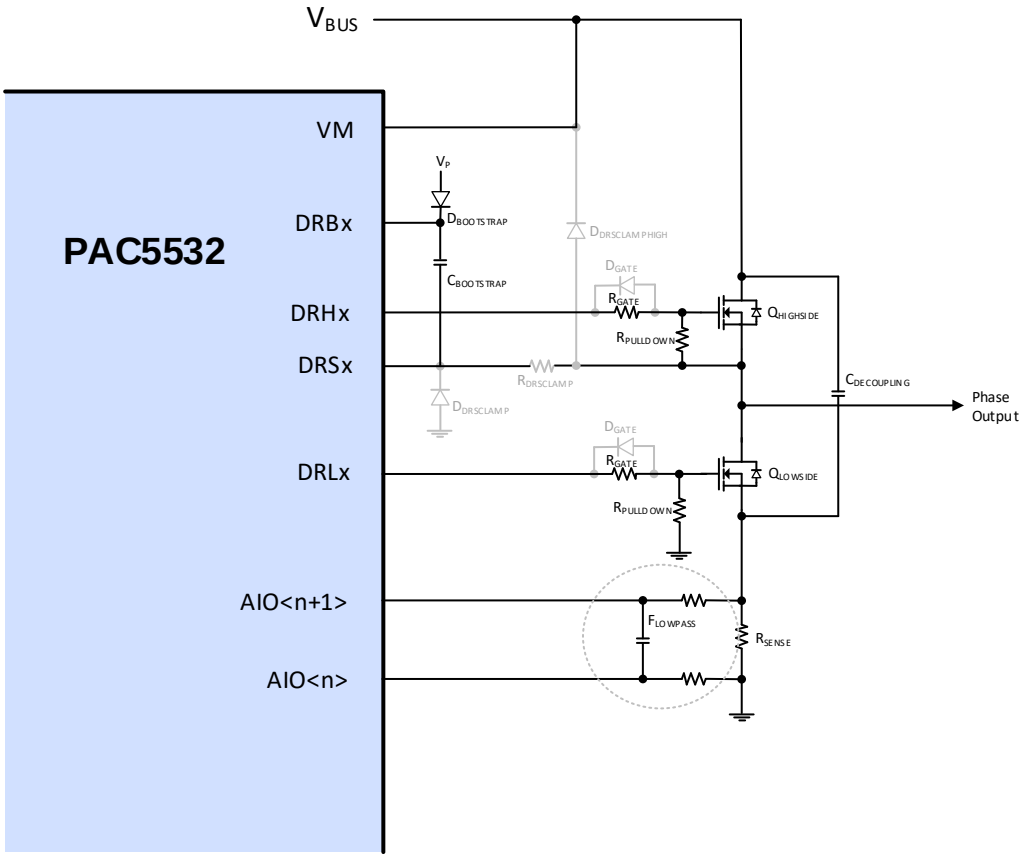
When routing both analog and digital signals, it may be beneficial to use 45° angles when routing traces rather than 90° angles. Using sharp corners to traces may increase emissions at the corners, so it is recommended to use 45° angles whenever possible.

The diagram below shows an example of how several signals, including analog ADC inputs are routed using 45° angles.



GATE DRIVER DESIGN

Below are the recommendations to follow for the PCB connection to the gate drivers. Please refer to the figure below for reference.



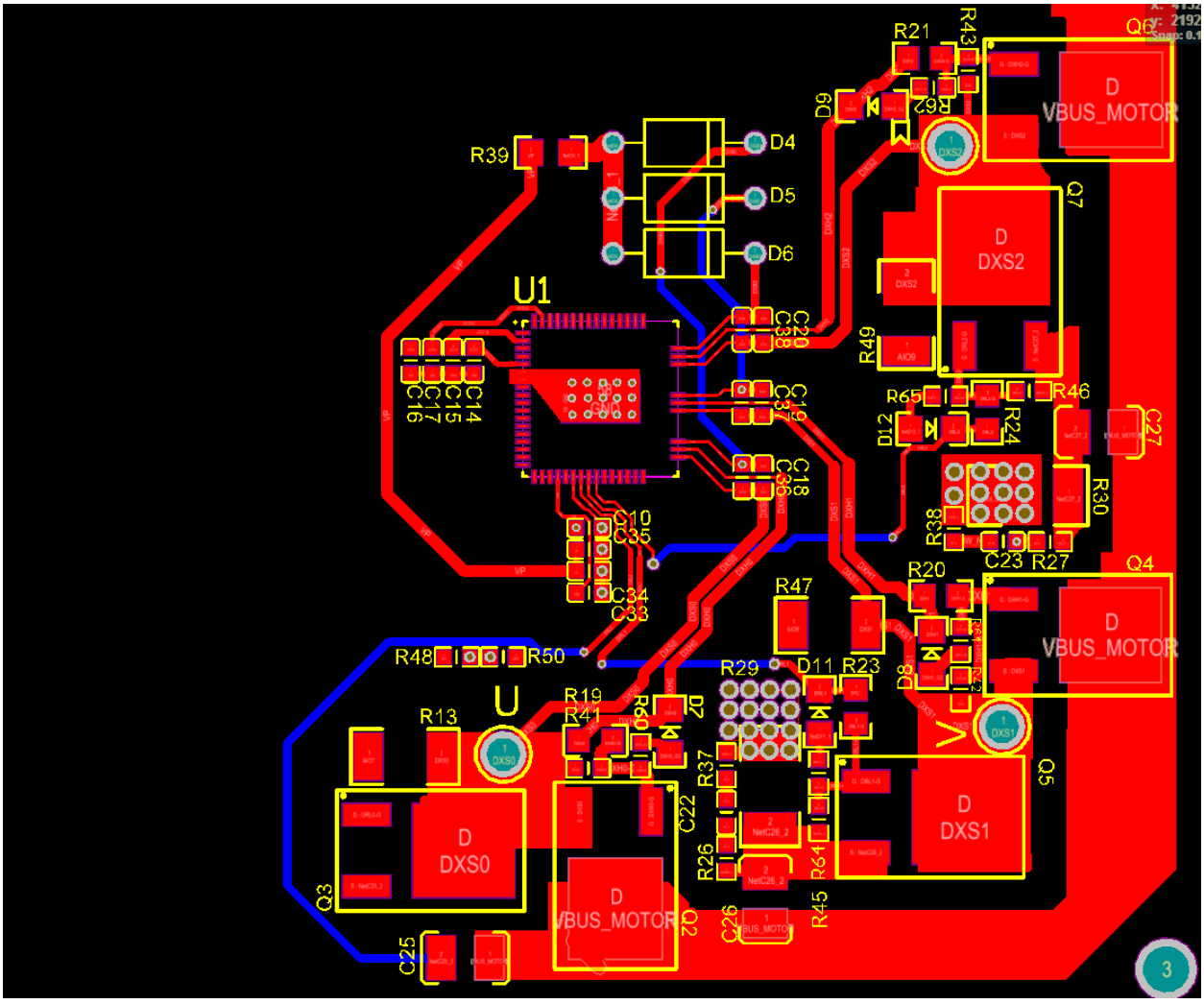
In the gate driver design for the PAC55XX, the following are recommended:

- In the gate driver design for the PAC55XX, the gate driver bootstrap capacitor ($C_{BOOTSTRAP}$) and the boot-strap diode ($D_{BOOTSTRAP}$) should be placed as close as possible to the device.
- The user can control the gate driver rise time by using a series gate resistor (R_{GATE}) to control the rise time of the gate driver. To reduce the fall time of the gate driver, the user can optionally use diode (D_{GATE}) in parallel to R_{GATE}.
- Both R_{GATE} and gate driver pull-down resistor ($R_{PULLDOWN}$) should be placed as close as possible to the Power FET ($Q_{HIGHSIDE}$ or $Q_{LOWSIDE}$). The Half-Bridge decoupling capacitor $C_{DECOUPLING}$ should be placed as close as possible to $Q_{HIGHSIDE}$ and $Q_{LOWSIDE}$.
- Both $Q_{HIGHSIDE}$ and $Q_{LOWSIDE}$ should be placed as close to each other as possible, and with as much copper as possible on their shared phase output, to minimize phase output ringing which can affect both performance and emissions.
- The motor voltage input to the drain of $Q_{HIGHSIDE}$ and the source of $Q_{LOWSIDE}$ should also use plenty of copper to reduce resistance.

The PAC55XX allows the user to program the dead-time for each complementary PWM output independently. Dead-time that is too aggressive can also cause shoot-through and ringing on the phase node of each half-bridge.

These can lead to FET failure and potentially EMI emissions, so the user should select a dead-time value that works for their system that maintains stable performance without ringing or shoot-through on the phase.

The diagram below shows the layout of the gate driver section, showing the above examples.



In this diagram, the reference designators for each of these nodes for the top motor phase are:

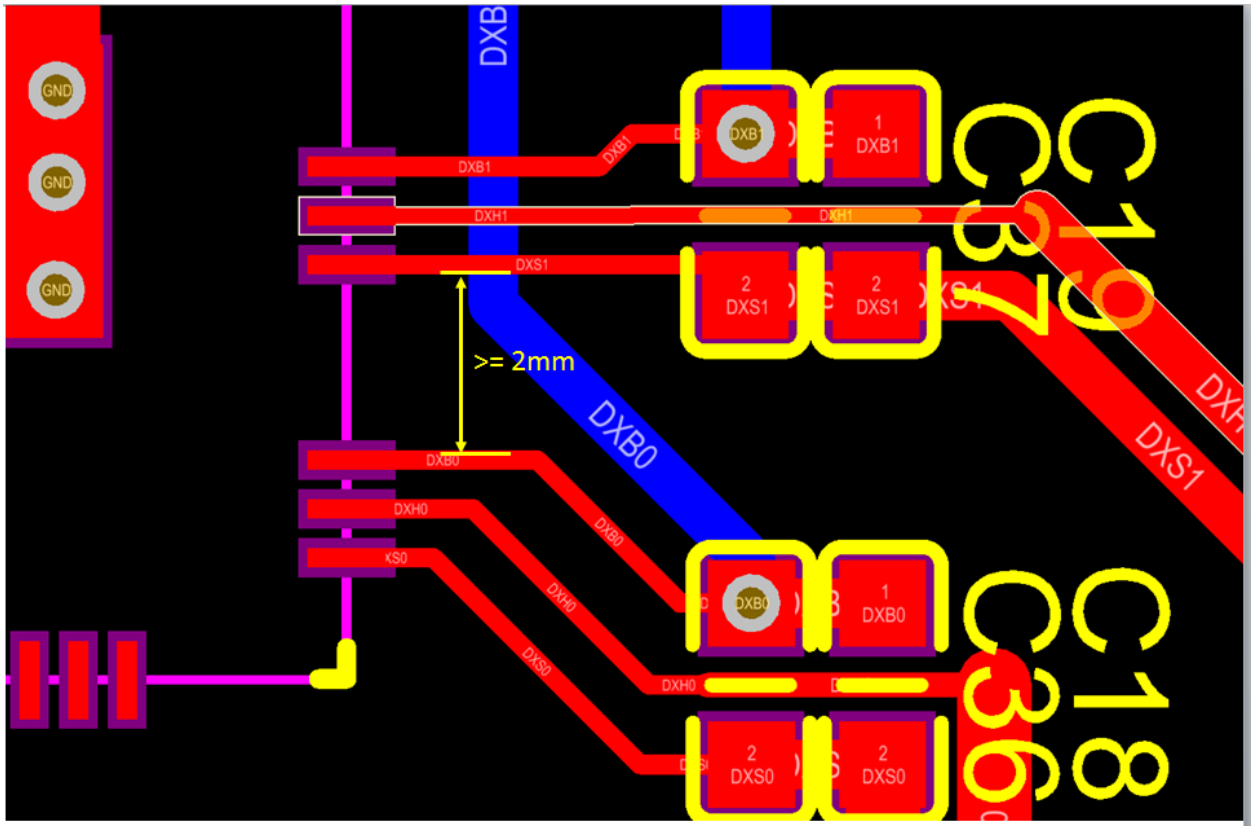
- $D_{BOOTSTRAP}$: D4
- $C_{BOOTSTRAP}$: C38
- R_{GATE}: R21 (High-side), R24 (Low-side)
- $R_{PULLDOWN}$: R43
- $Q_{HIGHSIDE}$: Q6
- $Q_{LOWSIDE}$: Q7
- $C_{DECOUPLING}$: C27

- D_{GATE}: D9 (High-side), D12 (Low-side)

In addition, the controller IC should be placed closely to the inverter FETs, to reduce parasitic components and gate signal ringing that can result as a consequence.

For high-voltage signals, the design should consider the creepage and clearance recommendations from the IPC-2221A and UL standards. This can help prevent voltage arcing between high-voltage nodes on the PCB.

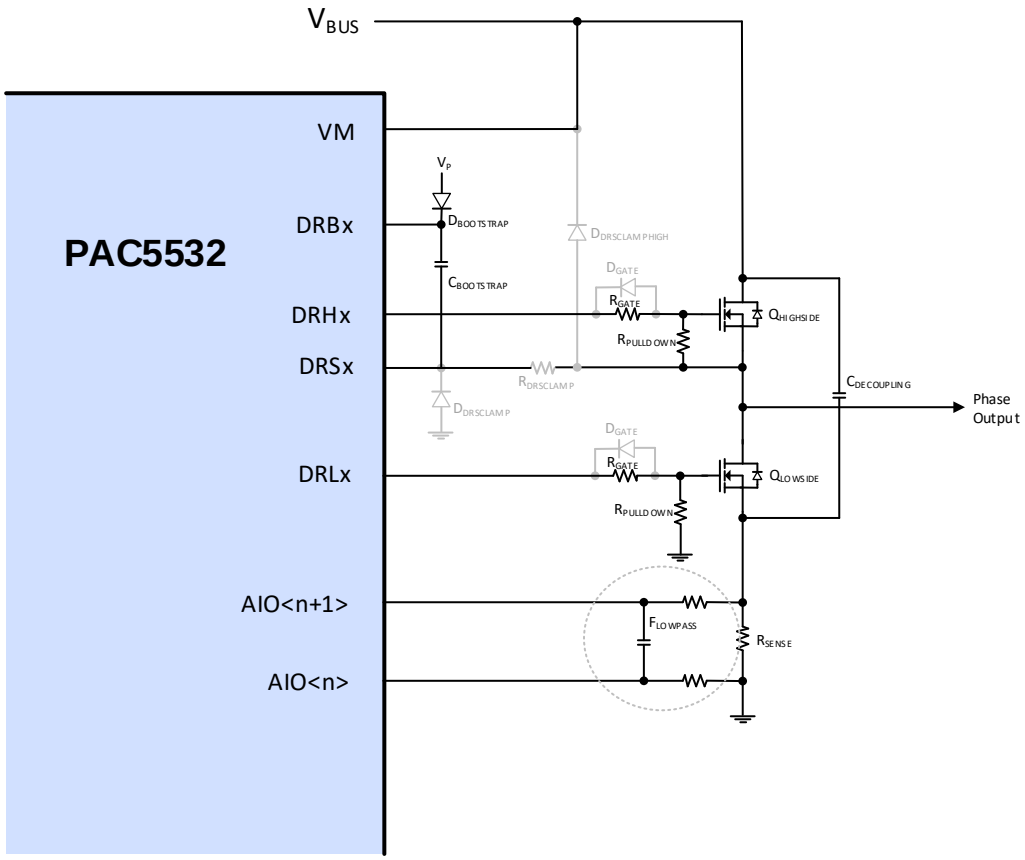
For the EP5250HVM design (600V), a 2mm clearance between HV signals is used, as is shown in the diagram below.



GATE DRIVER VOLTAGE CLAMPS

In each gate driver, there is also an optional resistor and diode ($R_{DRSCLAMP}$ and $D_{DRSCLAMP}$) that can be used to clamp the DRS voltage and limit the current to prevent it from going too far negative.

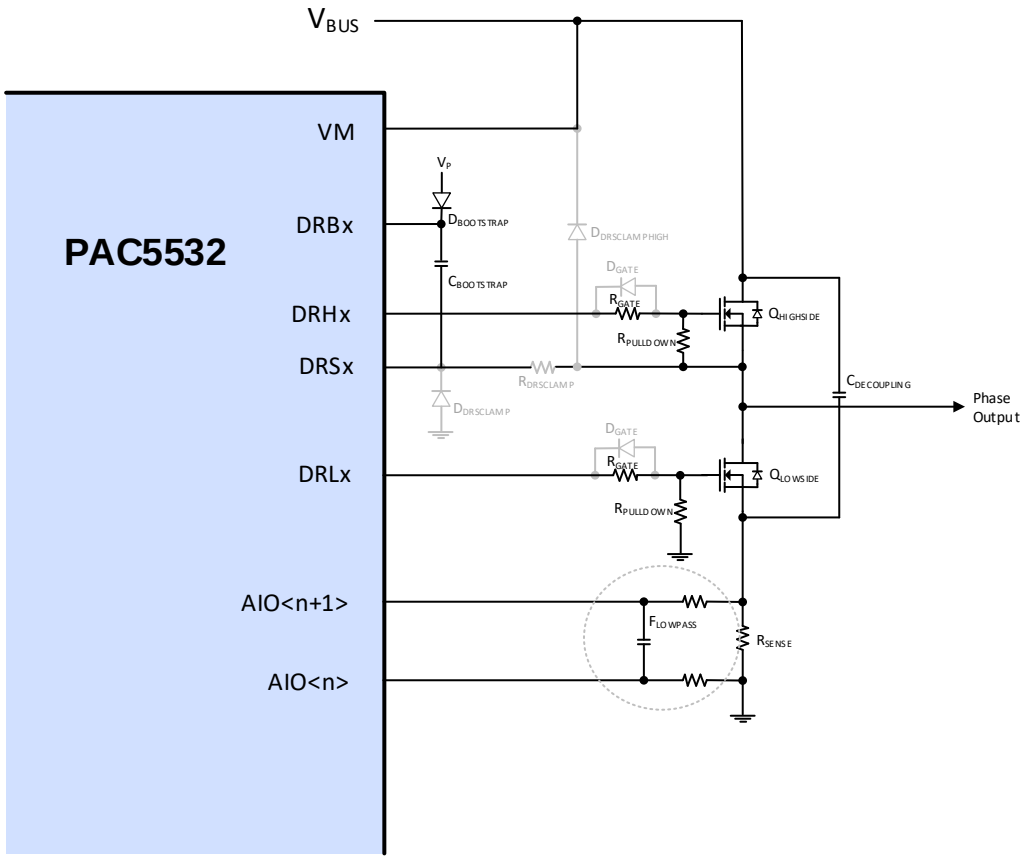
Below is a diagram that shows a gate driver design with this clamp on the DRS node.



Some of the PAC552X low-voltage (< 70V) devices have a small tolerance for negative-going voltage on the DRS node, so this diode helps prevent this situation.

For higher voltage devices, the tolerance on this pin is greater so this diode is generally not required on high-voltage applications, depending on the amount of phase current. Very high current applications at high-voltage may still require this clamp to prevent a large amount of negative-going voltage on DRS.

Other high-voltage applications that directly connect the motor voltage to the IC (such as PAC5532) that are very high current may also require a clamp between DRSx and VM ($D_{DRSCLAMPHIGH}$).



As the current load increases, voltage transients on DRS also can increase. These transients typically happen during the dead-time, when the current must find an asynchronous path to continue flowing.

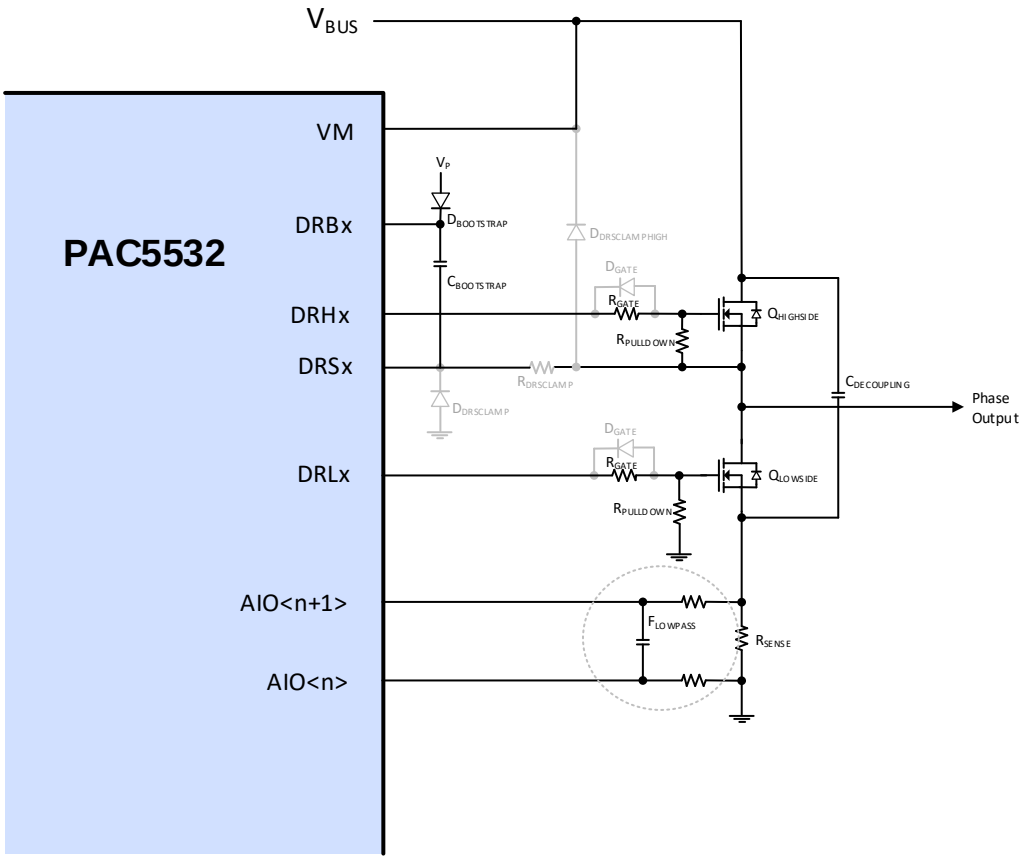
If these transients are too far above the motor voltage (VM), then damage may occur to the IC as well as the FETs. In these cases, it may be necessary to clamp the DRS voltage with respect to VM to prevent this from occurring.

Note that this scenario is generally more of a problem on high-voltage, high-current applications that directly connect the motor voltage to the IC.

SIGNAL CONDITIONING DESIGN

The PAC55XX contains integrated signal conditioning, such as programmable gain Differential Amplifiers. These Differential Amplifiers are often used for measuring motor phase current for both control and protection of the inverter (OC).

The diagram below shows an example of an inverter with the Differential Inputs to the PAC55XX for measuring phase current:



The value of the current sense resistor (R_{SENSE}) is selected based on the power requirements of the application. R_{SENSE} should be placed as close as possible to the Low-Side Power FET ($Q_{LOWSIDE}$).

The low-pass filter for the current sense circuit should be placed close to the IC for best performance. If the low-pass filter for the current sense circuit cannot be placed close to the IC, then at least the capacitor portion of this filter should be close to the IC.

The differential signals for the current sense circuit should be routed as symmetrically as possible from the current sense circuit's low-pass filter to the analog input channels on the IC. The trace widths should also be the same for each of these differential signals.

EMI CONSIDERATIONS

When designing motor control applications, it is best to consider the tradeoffs between cost, application performance and EMI.

In these applications, EMI may be generated by the following:

- Any signals leaving the PCB (such as IO to a another controller module)
- Aggressive dead-time configuration for the gate driver
- Low values for R_{GATE}
- 90° edges for high-frequency signals

For signals between the PCB and another sub-system, IOs may carry emissions from the IC to the system resulting in spikes at certain frequencies. To prevent this, the designer may consider adding resistor beads or resistors to attenuate any high-frequency noise from the IC into the cabling between PCBs.

For signals not carrying a lot of current, series resistors can be adequate attenuators for the high frequency noise on these cables. There are though a few situations where resistors may not be adequate. High-speed signals cannot afford to have series resistors due to bandwidth reduction, and wires carrying current such as power supply lines would experience a voltage drop if a series resistor is used. In these cases it may be necessary to use beads to attenuate the high frequency noise while leaving the lower frequencies mostly unaffected.

To increase efficiency, designers sometimes reduce the R_{GATE} resistor value as much as possible. This will decrease the turn-on time of the FET through the gate, but too sharp an edge may result in ringing at the phase node. This ringing may cause emissions, which will manifest itself as noise at certain frequency bands. To reduce this noise, a higher value R_{GATE} is necessary which will slow the turn-on time of the FET, and reduce the ringing on the phase, and the related emissions during turn on of the FET.

Another technique sometimes used to increase efficiency is to reduce the amount of dead-time in the half-bridge. In the PAC55XX, the dead-time is configurable in the firmware to give users a range of choices to suit the needs of the applications. If the dead-time is too low, there may also be ringing on the phase, which will cause emissions that can create noise at certain frequencies. To mitigate this, the user may increase the dead-time in the PAC55XX to decrease the ringing and emissions.

As shown above, using 45° angles rather than sharper 90° may reduce the amount of emissions from high-frequency signals as well. It is recommended when possible to use 45° angles when routing of high-frequency signals.

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For more information on this and other products, contact sales@active-semi.com or visit www.active-semi.com.