PAC5527 Device User Guide

Power Application Controller®

Multi-Mode Power Manager™

Configurable Analog Front End™

Application Specific Power Drivers™

Arm® Cortex®-M4F Controller Core

Rev 1.2 – Jan 17, 2019

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1 OVERVIEW

This document is the PAC5527 Device User Guide. It details the operation of the analog peripherals in the PAC5527.

For detailed information on the MCU and Digital Peripherals in the PAC5527, see the *PAC55XX Family User Guide*.

2 STYLE AND FORMATTING CONVENTIONS

This chapter describes the formatting and styles used throughout this document.

2.1 Number Representation

Numbers other than decimal will have a postfix indicator. All numbers use little endian formatting, with the most significant bit/digit to the left. Digits for binary and hexadecimal representation are grouped with a single space every four digits to improve readability. Binary numbers use “b” as a postfix and hexadecimal numbers use “h” as a postfix.

For example, 1011b binary = Bh hexadecimal = 11 decimal.

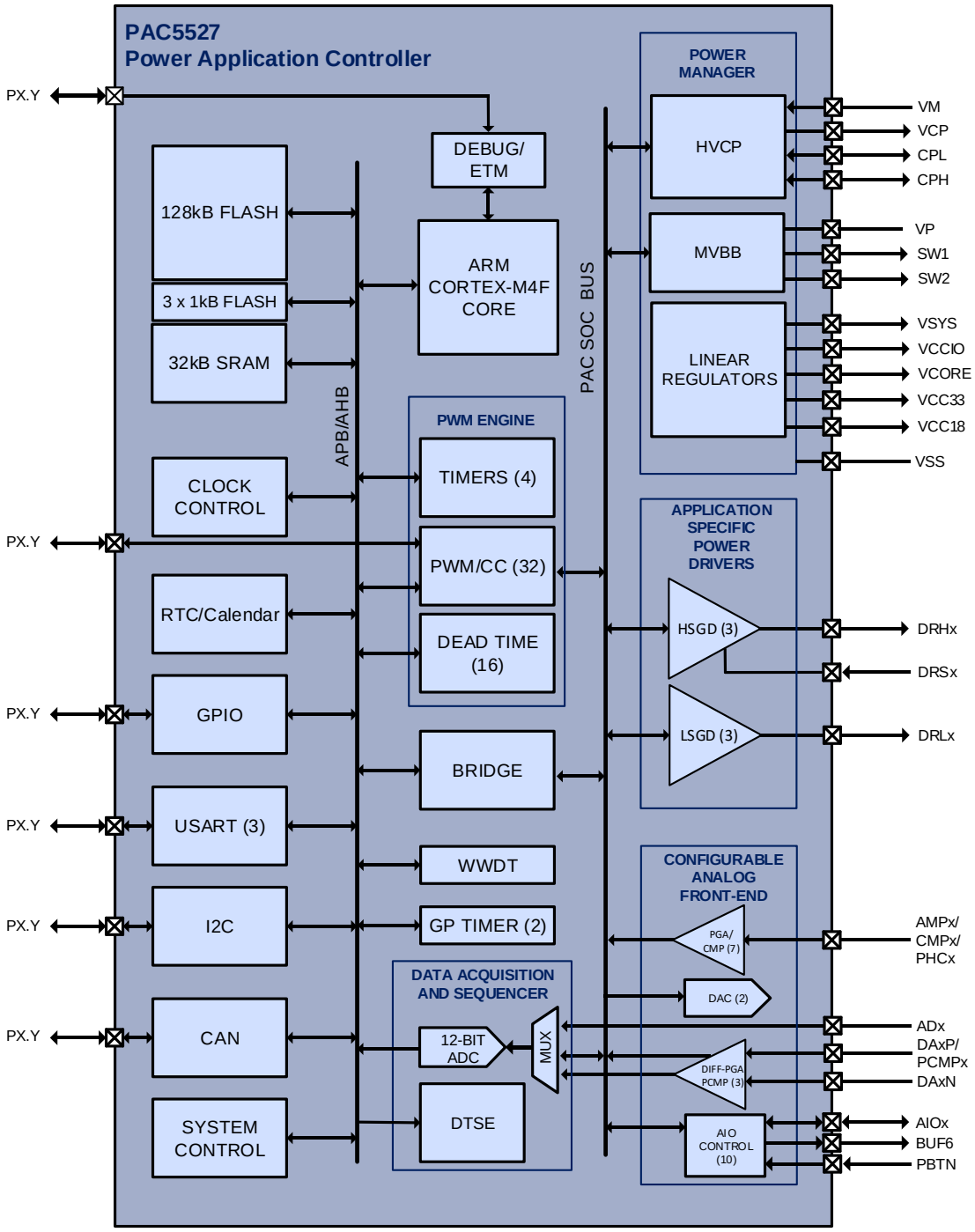
2.2 Formatting Styles

TYPE	EXAMPLE	DESCRIPTION
Register Name	**RTCCTL**	Register names use a capital letter and **boldface** type.
Register Bit(s)	**RTCCTL.RTCCLKDIV**	Register bits are always represented with the register name separated with a period.
Function selected by register bit(s)	**[RTCCTL.RTCCLKDIV]**	Within text blocks, functions selected with a register bit setting are set in brackets. For example **[RTCCTL.RTCCLKDIV]** means divider settings /2 to /65536.
Pin Function	PA5	Pin functions use capital letters
Internal signals	*PWMA3*	Internal signals use *italicized* font.
Formulas	`CLK = FCLK / DIV`	Formulas use `monospaced` text.
Links	Link	Hyperlinks are underlined and blue.
CPU Mnemonic	`MRS`	CPU Mnemonic uses `monospaced` text.
Operands	*`{Rd, }, Rn, Rm`*	Operands use *`monospaced italic`* text.
Code examples	`b loopA`	Code examples use monospaced text.

3 ARCHITECTURAL BLOCK DIAGRAM

For Below is an architecture block diagram of the PAC5527 device.

Figure 3-1 PAC5527 Architectural Block Diagram



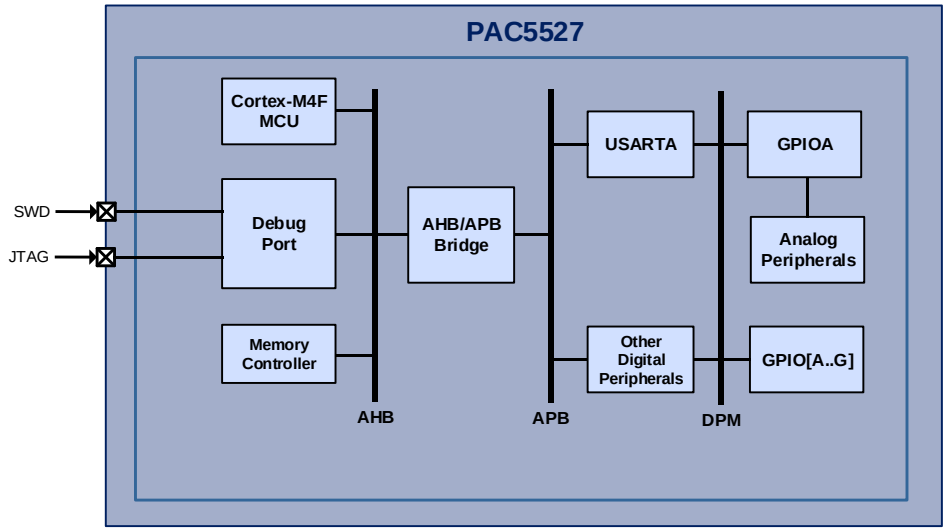
4 ANALOG REGISTER ACCESS

4.1 Overview

All analog registers in the PAC5527 are accessible through a SOC bus in the device. Unlike registers in the MCU (SRAM and digital peripheral registers), these analog registers are not memory mapped.

The block diagram below shows the different system busses that the MCU uses to access the different system registers.

Figure 4-1 PAC5527 Register Access



The PAC5527 contains two register buses: the AHB bus and the APB bus.

The AHB bus allows the MCU and Debug Port access to FLASH and SRAM via the Memory Controller. To access other digital peripheral connected to the APB bus, there is a bridge from the AHB to the APB bus so that the MCU or Debug Port can perform memory-mapped register access to all digital peripherals. Some digital peripherals such as timers are flexibly connected to IO using the DPM bus.

To access the Analog peripherals, the USARTA SPI peripheral is used to generate read and write transactions to the Analog registers using the DPM and GPIOA.

4.2 Functional Description

External programming interfaces such as JTAG and SWD or the Arm® Cortex®-M4F MCU may perform memory-mapped accesses to USART A through the AHB and APB busses on the device.

USART A is a serial communication peripheral that supports a SPI-like protocol that can be used to communicate to the Analog Peripherals for read and write transactions. The Digital Peripheral MUX (DPM) may be configured to connect the USART A SPI signals to GPIO A, where they are connected to the Analog peripherals.

4.3 USART Configuration

USART A acts as a SPI bus master to communicate with the Analog Peripherals. The USART A signals that are used for this communication are:

- *USASCLK* – USART A SPI Clock
- *USAMOSI* – USART A Master-Out/Slave-In
- *USAMISO* – USART A Master-In/Slave-Out
- *USASS* – USART A Slave Select

In order to communicate with the Analog Peripherals, the USART A should have the following configuration:

- 8-bit mode
- SCLK active high
- CPH is sample/setup
- SS active low

When communicating with the Analog Peripherals, the maximum SCLK frequency is 25MHz.

4.4 Protocol

The protocol for communicating with the Analog Peripherals is a simple two-byte protocol.

The first byte is always the address, which includes a 7-bit address [7:1] and a write bit [0]. For write operations, the write bit [0] is set to 1b. For read operations, the write bit [0] is set to 0b.

For write operations, the 2nd byte will be the 8-bit data to write to the given address.

For read operations, the 2nd byte is ignored and MISO will contain the 8-bit data read from the given address.

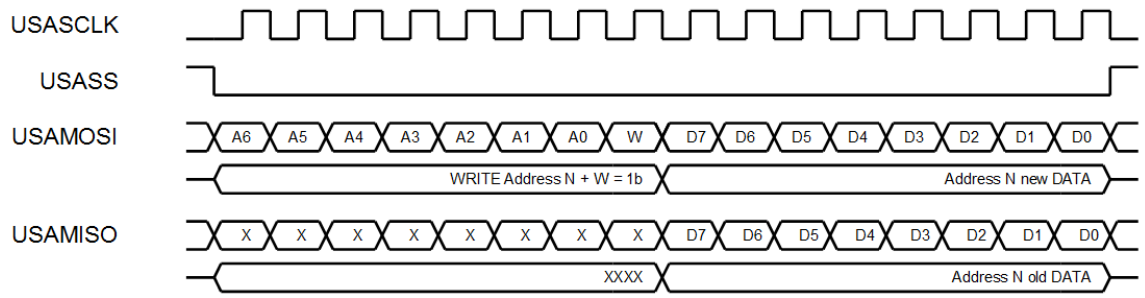
4.5 Write Register Example

To write the **HPDAC** register (address 2Bh) with the value 28h, issue the following transactions to USART A:

- Write **SSPADAT** with the value 57h (2Bh << 1 | 1b for write transaction)
- Write **SSPADAT** with the value 28h

The timing diagram from a write operation is shown below.

Figure 4-2 Analog Peripheral Register Write Timing



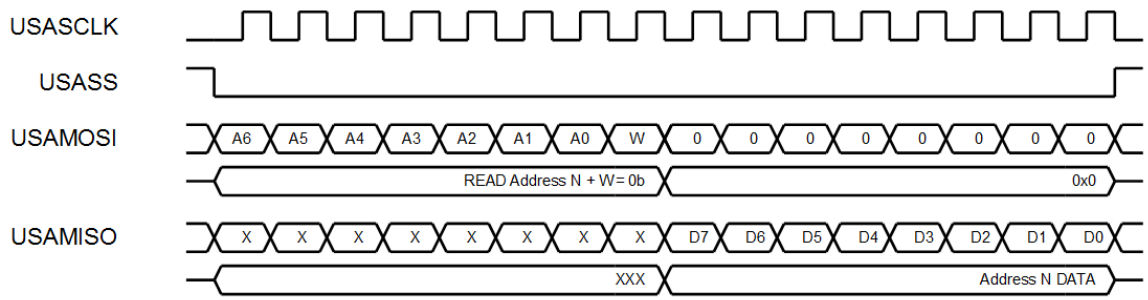
4.6 Read Register Example

To read the contents of the **HPDAC** register, issue the following transactions to USART A:

- Write **SSPADAT** with the value 56h (2Bh << 1 | 0b for read transaction)
- Write **SSPADAT** with a dummy character
- Read last data from MISO from **SSPADAT**, this is the register value

The timing diagram from a read operation is shown below.

Figure 4-3 Analog Peripheral Register Read Timing



For more information on how to configure the DPM to support the USART A peripheral for communicating with the Analog Registers, see the PAC55XX Family User Guide.

5 PAC5527 IO

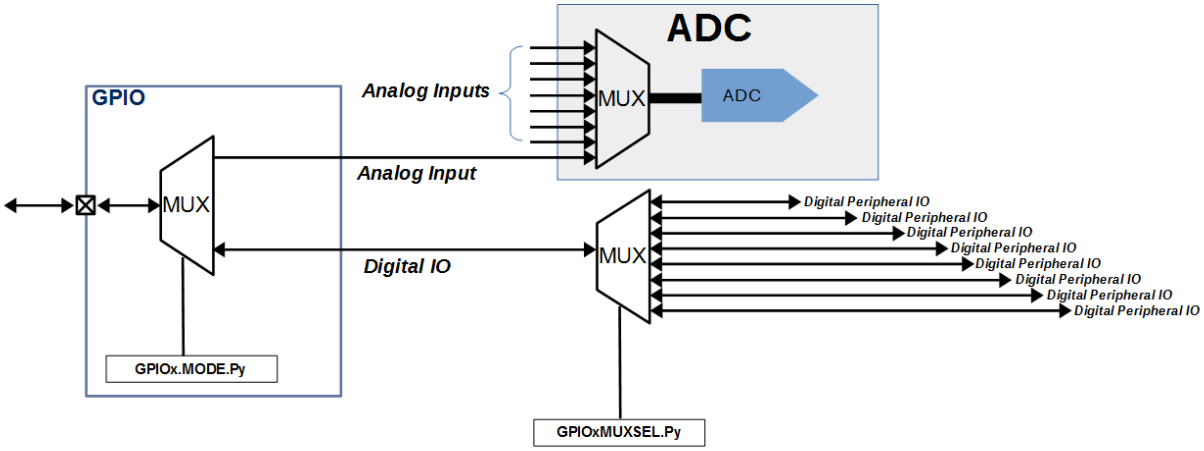
5.1 Overview

The Digital Peripheral MUX (DPM) on the PAC55XX family allows flexible assignment of peripheral functions to IO pins.

Each member of the family has a different set of IO pins that are available. It is important during application design that the designer consider the available IO pins to make sure the necessary peripherals will be available.

Below is a diagram of the GPIO and MUX structure.

Figure 5-1 GPIO and DPM Block Diagram



Each IO can be configured to select 1 of up to 8 digital peripheral signals. Some IOs also may be used as an ADC input. For information on how to configure the IO for each of these situations, see the PAC55XX Family User Guide.

The PAC5527 has the following IO pins available for application use:

- PA[7:0] – Reserved for MMPM, ASPD, CAFE
- PB[7:0] – Reserved for ASPD
- PD[7:4]
- PE[3:0]
- PF[7:0]

5.2 ADC Channels

The ADC channels that are available on the PAC5527 are shown in the table below.

Table 5-1 PAC5527 ADC Input Pins

ADC Channel	IO PIN
ADC0	PG7[1]
ADC4	PF4
ADC5	PF5
ADC6	PF6
ADC7	PF7

[1] Available for sampling channels in the CAFE only

5.3 Digital Peripheral Pins

The digital peripheral functions that are available in the PAC5527 are shown below.

Table 5-2 PAC5527 Digital Peripheral Pins

PORT	Pin	GPIOxMUXS.Py							
		000b	001b	010b	011b	100b	101b	110b	111b
GPIOA	P0	**GPIOA0**							
	P1	GPIOA1	**EMUXD**						
	P2	GPIOA2	**EMUXC**						
	P3	GPIOA3	**USASCLK**	USBSCLK					
	P4	GPIOA4	**USAMOSI**	USBMOSI					
	P5	GPIOA5	**USAMISO**	USBMISO					
	P6	GPIOA6	**USASS**	USBSS					
	P7	**GPIOA7**							
GPIOB	P0	**GPIOB0**	TAPWM0	TBPWM0		TCPWM0	TDPWM0		
	P1	**GPIOB1**	TAPWM1	TBPWM1		TCPWM1	TDPWM1		
	P2	**GPIOB2**	TAPWM2	TBPWM2		TCPWM2	TDPWM2		
	P4	**GPIOB4**	TAPWM4	TBPWM4		TCPWM4	TDPWM4		
	P5	**GPIOB5**	TAPWM5	TBPWM5		TCPWM5	TDPWM5		
	P6	**GPIOB6**	TAPWM6	TBPWM6		TCPWM6	TDPWM6		
GPIOD	P4	**GPIOD4**	TBPWM4	TCPWM4	TDQEPIDX	TBQEPIDX	USDSCLK	TRACED3	USDMOSI
	P5	**GPIOD5**	TBPWM5	TCPWM5	TDQEPPHA	TBQEPPHA	USDSS	CANRXD	USDMISO
	P6	**GPIOD6**	TBPWM6	TCPWM6	TDQEPPHB	TBQEPPHB	USDMOSI	CANTXD	I2CSDA
	P7	**GPIOD7**	TBPWM7	TCPWM7			USDMISO	CANRXD	
GPIOE	P0	**GPIOE0**	TCPWM4	TDPWM0	TAIDX	TBIDX	USCSCLK	I2CSCL	EMUXC
	P1	**GPIOE1**	TCPWM5	TDPWM1	TAPHA	TBPHA	USCSS	I2CSDA	EMUXD
	P2	**GPIOE2**	TCPWM6	TDPWM2	TAPHB	TBPHB	USCMOSI	CANRXD	EXTCLK
	P3	**GPIOE3**	TCPWM7	TDPWM3	FRCLK		USCMISO	CANTXD	
GPIOF	P0	GPIOF0	TCPWM0	TDPWM0	**TMS/SWDCLK**	TBIDX	USBSCLK	TRACECLK	
	P1	GPIOF1	TCPWM1	TDPWM1	**TMS/SWDIO**	TBPHA	USBSS	TRACED0	
	P2	GPIOF2	TCPWM2	TDPWM2	**TDI**	TBPHB	USBMOSI	TRACED1	
	P3	GPIOF3	TCPWM3	TDPWM3	**TDO**	FRCLK	USBMISO	TRACED2	
	P4	**GPIOF4**	TCPWM4	TDPWM4		TCIDX	USDSCLK	TRACED3	EMUXC
	P5	**GPIOF5**	TCPWM5	TDPWM5		TCPHA	USDSS		EMUXD
	P6	**GPIOF6**	TCPWM6	TDPWM6		TCPHB	USDMOSI	CANRXD	I2CSCL

	P7	**GPIOF7**	TCPWM7	TDPWM7			USDMISO	CANTXD	I2CSDA

For more information on how to configure the DPM for the PAC5527, see the PAC55XX Family User Guide.

5.4 Analog Interrupts

The Analog Front-end may interrupt the MCU during operation when certain system conditions occur. There are two analog interrupts available:

- IRQ1 (MCU PA7)
- IRQ2/POS (MCU PA0)

The IRQ1 interrupt is available on the MCU on the PA7 IO. To receive this interrupt, the MCU must configure PA7 as an edge triggered, active-low interrupt. Error conditions such as power management faults, temperature faults and gate driver faults may assert the IRQ1 interrupt.

The IRQ2/POS interrupt is available on the MCU on the PA0 IO. To receive this interrupt, the MCU must configure PA0 as an edge triggered, active-low interrupt. This interrupt is asserted for AIO<9:6> are configured for digital input and interrupts, or when AIO<9:7> are configured for BEMF zero-cross comparisons (special mode).

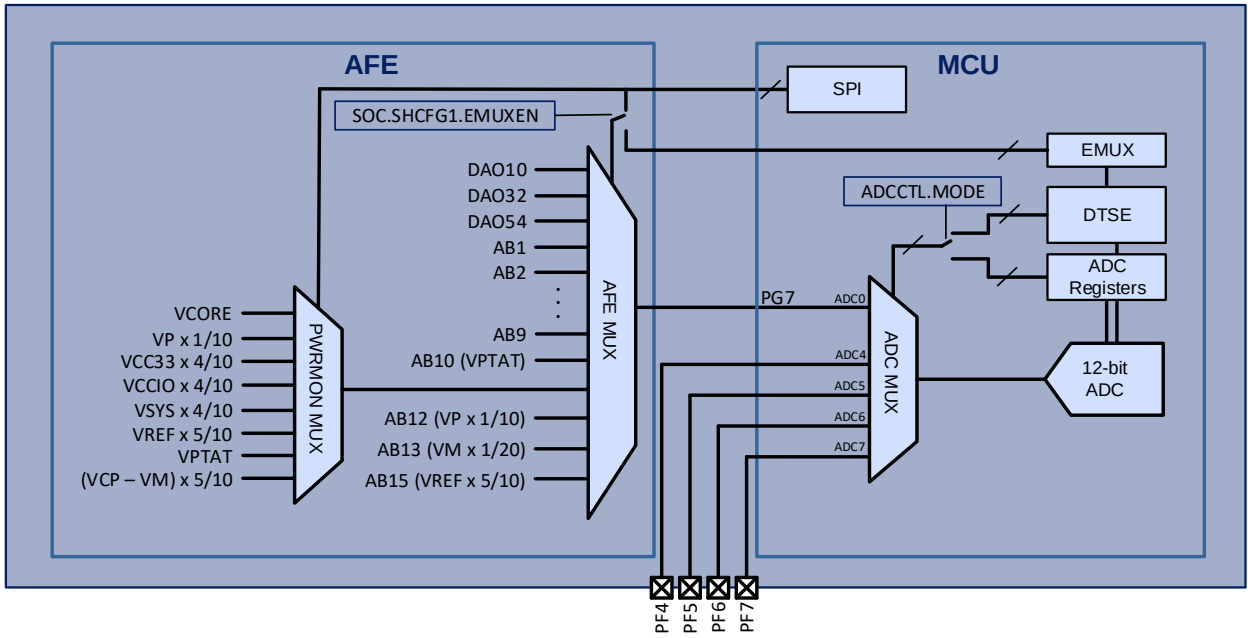
6 PAC5527 ADC MUXes

The PAC5527 allows the user to internally monitor the various internal and external analog channels through a series of MUXes on the MCU and AFE.

6.1 System Block Diagram

The various MUXes that are used for signal sampling are shown in the diagram below.

Figure 6-1 PAC5527 ADC MUX inputs



There are three main MUXes in the PAC5527:

- ADC MUX
- AFE MUX
- PWRMON MUX

6.2 ADC MUX

The ADC MUX is an 8-channel MUX local to the ADC on MCU that is directly controlled by either by registers in the MCU, or automatically by the ADC DTSE.

To configure the ADC for manual mode, set **ADCCTL.MODE** to 00b. When the ADC is in manual mode, **ADCCTL** may be used to enable and configure the ADC, including selecting the MUX channel that is used for sampling.

To configure the ADC for DTSE mode, set **ADCCTL.MODE** to 01b. In DTSE mode, the operation of the ADC and ADC MUX are done automatically in hardware according the DTSE and ADC configuration.

In the PAC5527, there are 4 external pins and one internal ADC channel that may be configured for ADC analog input that are shown in the table below.

Table 6-1 PAC5527 ADC MUX channels

ADC Channel	MCU I/O PIN	Description
ADC0	PG7	Connected to AFE MUX
ADC4	PF4	Package pin
ADC5	PF5	Package pin
ADC6	PF6	Package pin
ADC7	PF7	Package pin

The ADC0 channel is always used for analog input from the AFE and is connected to the AFE MUX on MCU internal pin PG7. ADC channels ADC<7:4> are directly connected to package pins on the device as shown in the table above.

To use any of these channels as analog inputs to the ADC the IO controller configuration for these pins must be configured as analog input. See the IO Controller section in the PAC55XX User Guide for more information on IO configuration.

6.3 AFE MUX

The AFE MUX is a 16-channel MUX that resides in the AFE. The AFE MUX is used for the internal analog bus that is connected to the output of the differential amplifier, single-ended amplifiers and other channels found in the CAFE.

The MUX select for the AFE MUX may also be controlled directly through the SOC registers or through the EMUX from the MCU's DTSE.

When the ADC is configured for manual mode, the EMUX enable function in the AFE should be disabled. To select the AFE MUX channel using the SOC registers, set **SOC.SHCFG1.EMUXEN** to 0b (disabled). The MUX channel may be selected from **SOC.SHCFG2.MUXA**.

When the ADC is configured for DTSE mode, the EMUX enable function in the AFE should be enabled. To select the AFE MUX channel using the EMUX set **SOC.SHCFG1.EMUXEN** to 1b (enabled). The AFE MUX channel may be selected from the EMUX data sent from the DTSE.

The channels available on the AFE MUX are shown in the table below.

Table 6-2 PAC5527 ADC MUX channels

AFE MUX Channel	Value	Description
DAO10	0000b	Output of Differential Amplifier for AIO10.
DAO32	0001b	Output of Differential Amplifier for AIO32.
DAO54	0010b	Output of Differential Amplifier for AIO54.
AB1	0011b	Analog bus AB1.
AB2	0100b	Analog bus AB2.
AB3	0101b	Analog bus AB3.
AB4	0110b	Analog bus AB4.
AB5	0111b	Analog bus AB5.
AB6	1000b	Analog bus AB6.
AB7	1001b	Analog bus AB7.
AB8	1010b	Analog bus AB8.
AB9	1011b	Analog bus AB9.
AB10 (VPTAT)	1100b	Internal temperature sensor (VPTAT).
AB11 (PWRMON)	1101b	Power Monitor MUX input.
AB12 (VP / 10)	1110b	VP voltage / 10.
AB13 (VM / 20)	1111b	VM voltage / 20.

For more information on the configuration and use of the EMUX, see the section below.

6.4 PWRMON MUX

The PWRMON MUX is an 8-channel MUX that resides in the AFE. The PWRMON MUX allows the user to sample internal power regulators for diagnostic purposes without dedicating an external ADC channel.

The MUX select for the PWRMON MUX is always controlled through the SPI bus by writing **SOC.PWRCTL.PWRMON**.

The PWRMON MUX output is on the analog bus channel AB11, which is directly connected to the AFE MUX.

The channels available on the PWRMON MUX are shown in the table below.

Table 6-3 PAC5527 ADC MUX channels

Channel	SOC.PWRCTL.PWRMON	Description
VCORE	000b	V_{CORE} LDO output voltage.
VP x 1/10	001b	V_P MVBB output voltage, scaled by 1/10.
VCC33 x 4/10	010b	V_{CC33} LDO output voltage scaled by 4/10.
VCCIO x 4/10	011b	V_{CCIO} LDO output voltage scaled by 4/10.
VSYS x 4/10	100b	V_{SYS} LDO output voltage scaled by 4/10.
VREF x 5/10	101b	ADC V_{REF} scaled by 5/10.
VPTAT	110b	Internal temperature sensor voltage.
(VCP – VM) x 5/10	111b	(V_{CP} – V_M) scaled by 5/10.

7 EMUX

The EMUX is a dedicated high-speed, low-latency serial interface to control the ADMUX, AIO7, AIO8, AIO9 POS S/H and the DAOxy S/H using the ADC DTSE sequencing engine.

To enable the EMUX set **SOC.SHCFG1.EMUXEN** = 1b. This will enable the DTSE to command control of the AFE MUX using EMUX data sent by the DTSE.

The EMUX allows high-speed control over the following:

- AFE MUX channel select
- DAO10, DAO32 and DAO54 sample and hold engine
- POS/BEMF sample and hold engine

The format of the EMUX command used to control the AFE MUX is the same as is shown in **SOC.SHCFG2**. The EMUX data is transmitted MSB first.

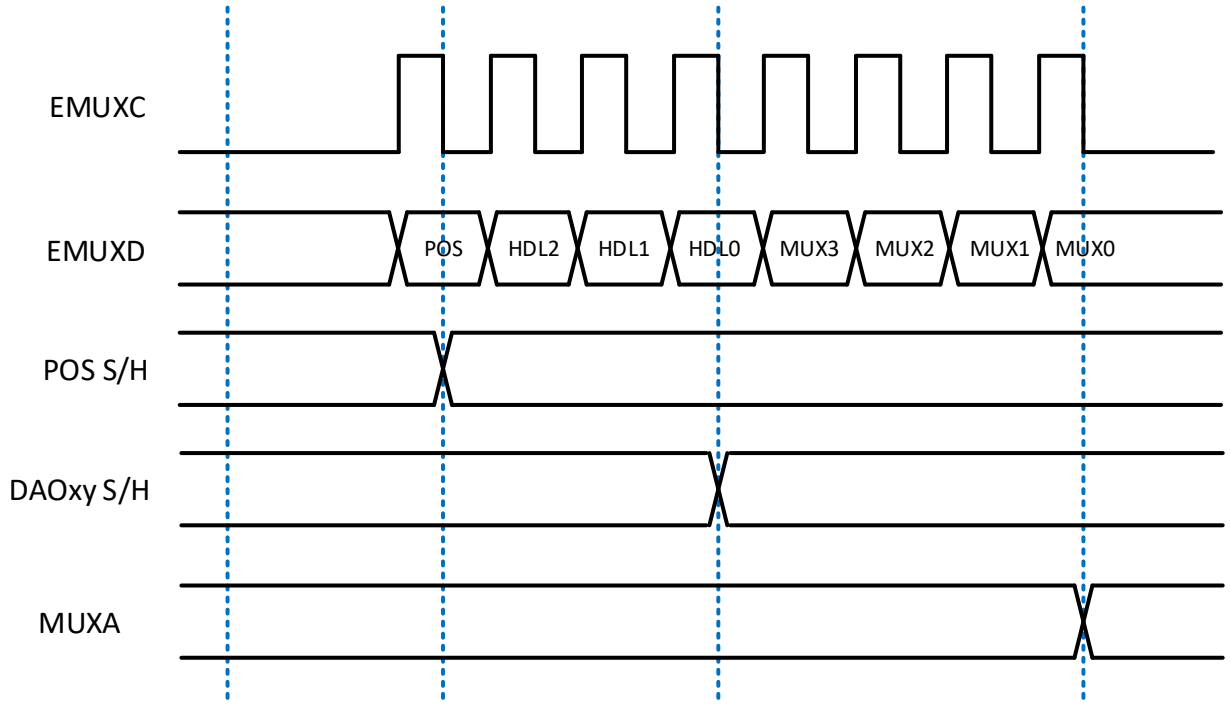
BIT	NAME	DESCRIPTION
7	POS	BEMF POS Sample and Hold: 0b: Sample POS value 1b: Hold POS value
6	HLD2	DAO54 Sample and Hold Output: 0b: Sample 1b: Hold
5	HLD1	DAO32 Sample and Hold Output: 0b: Sample 1b: Hold
4	HLD0	DAO10 Sample and Hold Output: 0b: Sample 1b: Hold
3:0	MUXA	AFE MUX channel selector when **SHCFG1.EMUXEN** = 1b. 0000b: DAO10 0001b: DAO32 0010b: DAO54 0011b: AB1 0100b: AB2 0101b: AB3 0110b: AB4 0111b: AB5 1000b: AB6 1001b: AB7 1010b: AB8 1011b: AB9 1100b: AB10 (VPTAT) 1101b: AB11 (PWRMON) 1110b: AB12 (VP / 10) 1111b: AB13 (VM / 20)

The BEMF POS sample and hold circuits are toggled based on the POS bit in the EMUX packet with the falling edge of the 1st clock cycle.

The AIO10, AIO32 and AIO54 sample and hold circuits are toggled based on the HLD<2:0> bits with the falling edge of the 4th clock cycle.

The AFE MUX select is switched with the falling edge of the 8th clock based on the data of bits 3:0 of the EMUX packet.

Figure 7-1 EMUX Timing Diagram



8 POWER MANAGER

8.1 Overview

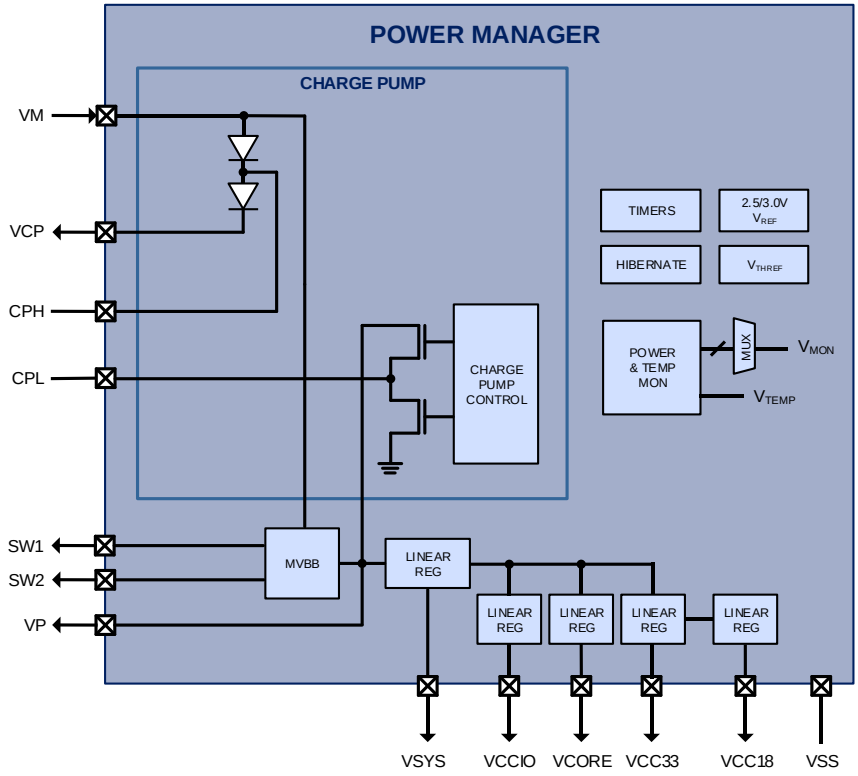
The Multi-Mode Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a High-Voltage Charge Pump (HVCP) efficiently convert power from a DC input source to generate a gate driver VCP. There is also a medium-voltage Buck-Boost (MVBB) that generates a 10V o 12V low-side gate driver supply. Five linear regulators provide VSYS, VCCIO, VCC33, VCC18 and VCORE supplies for 5V system, 3.3V I/O, 3.3V mixed signal,1.8V FLASH and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

8.2 Features

- Charge Pump for high-side gate driver supply
  - Input Voltage: 6V - 48V
- Configurable Buck-Boost converter for low-side gate driver supply (10V/12V)
- 5 additional Linear regulators with power and hibernate management
- High-accuracy voltage reference for ADC and comparators
- Power and temperature monitor, warning, fault detection
- Extremely low hibernate mode I_Q of 10µA

8.3 System Block Diagram

Figure 8-1 Power Manager System Block Diagram



8.4 Functional Description

The Power Manager is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a High-Voltage charge pump (HVCP) DC/DC to generate the supply for the integrated high-side gate drivers and a Medium-Voltage Buck-Boost Converter (MVBB) to generate the supply for the integrated low-side gate drivers.

Five additional linear regulators provide V_{SYS}, V_{CCIO}, V_{CC33}, V_{CC18} and V_{CORE} supplies for 5V system, 3.3V I/O, 3.3V mixed signal, MCU FLASH and 1.2V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

8.5 VP Low Warning

If the VP low-side gate driver supply (output of the MVBB) is below the power good state, then the following actions are taken:

- **SOC.STATUS.VPLOW** is set to 1b
- **SOC.STATUS.VPLOW_LATCH** is set to 1b
- If the **SOC.FAULTEN.nVPFLT** bit is set to 1b, the IRQ1 interrupt to the MCU is asserted

This allows the any VPLOW event to be captured in the latch register, even if VP returns to normal operation. When **SOC.STATUS.VPLOW_LATCH** is set to 1b, then this bit will be cleared and the IRQ1 signal to the MCU will be de-asserted.

As soon as VP rises above the power good threshold, **SOC.STATUS.VPLOW** will be set to 0b.

8.6 Power Manager Faults

The power manager monitors all the power supplies and LDOs for faults during operation.

During a power management fault condition such as under-voltage or over-current each of the power supplies will set a fault bit and certain power supplies will be disabled as a result of the fault. During all power supply faults, **SOC.ENSIG.ENSIG**, **SOC.ENDRV.ENDRV** and **SOC.MISC.MCUALIVE** are all set to 0b.

Table 8-1 Power Manager Fault Handling

FAULT	ACTION	FAULT BIT
VP	Disable VP, VSYS, VCCIO, VCORE and VCC33.	**SOC.FAULT.VPFLT**
VSYS	Disable VSYS, VCCIO, VCORE and VCC33	**SOC.FAULT.VSYSFLT**
VCCIO	Disable VCCIO, VCORE, VCC33	**SOC.FAULT.VCCIOFLT** **SOC.FAULT.VCOREFLT** **SOC.FAULT.VCC33FLT**
VCORE	Disable VCCIO, VCORE, VCC33	**SOC.FAULT.VCCIOFLT** **SOC.FAULT.VCOREFLT** **SOC.FAULT.VCC33FLT**
VCC33	Disable VCCIO, VCORE, VCC33	**SOC.FAULT.VCCIOFLT** **SOC.FAULT.VCOREFLT** **SOC.FAULT.VCC33FLT**

To reset the fault condition, the corresponding fault bit(s) should be written to a 1b and then the power supplies will be re-started according to the power supply sequence.

8.7 Temperature Warnings and Faults

The PAC5527 monitors the device temperature for two different thresholds:

- Temperature Warning
- Temperature Fault

When the die temperature exceeds the temperature warning threshold of 140°C, the **SOC.FAULT.TMPWARN** bit and the **SOC.FAULT.TMPWARN_LATCH** bits are both set to 1b. If the **SOC.FAULTEN.TMPWARNINT** bit is set to 1b (interrupt not masked), then an interrupt on IRQ1 will be asserted to the MCU. Writing **SOC.FAULT.TMPWARN_LATCH** to 1b will reset this bit to 0b and will de-assert the IRQ1 signal.

When the temperature falls below 140°C minus the hysteresis, the **SOC.FAULT.TMPWARN** bit will be cleared.

When the die temperature exceeds the fault threshold of 165°C, the **SOC.FAULT.TMPFAULT** bit is set to 1b. When this fault occurs, the PAC5527 is forced into hibernate mode and will stay in hibernate mode until the push-button or wake-up timer (if configured) is received.

If the user has not configured the push-button or wake up timer to exit hibernate mode, the PAC5527 will stay in hibernate mode until powered off and on again.

8.8 Register Summary

Table 8-2 Power Manager Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
00h	**SOC.FAULT**	Fault condition indication register	00h
01h	**SOC.STATUS**	Hardware status condition register	00h
02h	**SOC.MISC**	Miscellaneous features register	00h
03h	**SOC.PWRCTL**	Power Manager control register	00h
04h	**SOC.FAULTEN**	Power Manager fault mask register	00h
05h	**SOC.WATCHDOG**	SOC Watchdog configuration register	00h
2Bh	**SOC.SYSCONF**	Power Manager system configuration register	C5h

8.9 Register Detail

8.9.1 SOC.FAULT

Register 8-1 SOC.FAULT (Fault Condition, 00h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**TMPWARN**	R	0x0	Real-time temperature warning status. When the temperature is greater than the warning threshold, this bit is set to 1b. When the temperature less than the warning threshold, this bit is set to 0b. 0b: No temperature warning 1b: Temperature warning
6	**TMPWARN_LATCH**	R	0x0	Latched temperature warning status. If the temperature reaches the warning threshold and the **SOC.FAULTEN.nTMPWARN** is not masked, this bit is set and IRQ1 is asserted. Write 1b to clear when not masked. 0b: No temperature warning 1b: Temperature warning
5	**TMPFLT**	R	0x0	Temperature fault status. If the temperature reaches the fault threshold, this bit is set to 1b. Write 1b to clear. 0b: No temperature fault 1b: Temperature fault
4	**VPFLT**	R	0x0	DC/DC fault when VP is below UVLO or over-voltage. Set on fault, and cleared when written to 1b. 0b: No VP fault 1b: VP fault
3	**VSYSFLT**	R	0x0	VSYS fault when VSYS is below UVLO or over-voltage. Set on fault, and cleared when written to 1b. 0b: No VSYS fault 1b: VSYS fault
2	**VCCIOFLT**	R	0x0	VCCIO fault. Set on fault, and cleared when written to 1b. 0b: No VCCIO fault 1b: VCCIO fault
1	**VCC33FLT**	R	0x0	VCC33 fault. Set on fault, and cleared when written to 1b. 0b: No VCC33 fault 1b: VCC33 fault
0	**VCOREFLT**	R	0x0	VCORE fault. Set on fault, and cleared when written to 1b. 0b: No VCORE fault 1b: VCORE fault

8.9.2 SOC.STATUS

Register 8-2 SOC.STATUS (System Status, 01h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HWRSTAT**	R/W	0x0	Hardware Reset Status. Bit is set on hardware reset and is cleared when written to 1b. 0b: No hardware reset 1b: Hardware reset
6	**SRSTSTAT**	R/W	0x0	Soft Reset Event. Bit is set on software reset event and is cleared when written to 1b. 0b: No software reset 1b: Software reset
5	**WDTRSTAT**	R/W	0x0	Watchdog Timer Reset Status. When enabled, this bit is set on Watchdog Timer Reset and cleared when written to 1b. 0b: No WDT reset 1b: WDT Reset
4	**RFU**	R	0x0	Reserved
3	**VPLOW**	R	0x0	Real-time VP Low Status. When set, the VP supply is below the power good threshold. 0b: No VP low 1b: VP low
2	**VPLOW_LATCH**	R/W	0x0	Latched VP Low Status. During VP low condition, this bit is set and the IRQ1 signal is asserted. To clear this bit, write to 1b. 0b: No latched VP low 1b: Latched VP low
1	**PBSTAT**	R	0x0	Real-time Push-button Status. 0b: Push-button not active 1b: push-button active
0	**PBSTAT_LATCH**	R	0x0	Latched Push-button Status. This bit is set in normal operation as long as the push button is enabled and on for more than the deglitch time, if not masked. When this bit is set, it will assert the IRQ signal. 0b: Latched push-button not active 1b: Latched push-button active

8.9.3 SOC.MISC

Register 8-3 SOC.MISC (SOC Miscellaneous Configuration, 02h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HIB**	R/W	0x0	Hibernate Mode. This bit is automatically cleared when the power up sequence is initiated, or in hibernate mode after wake-up timer delay or after push-button wake-up. 0b: Normal 1b: Shutdown mode
6	**PBEN**	R/W	0x0	AIO6 Push-button Enable. 0b: Push-button not enabled 1b: Push-button enabled
5	**VREFSET**	R/W	0x0	ADC Reference Voltage Setting. 0b: 2.5V 1b: 3.0V
4	**RFU**	R	0x0	Reserved
3	**MCUALIVE**	R/W	0x0	MCU Alive. Set by the MCU to indicate that it is alive. Before this bit is set, ignore all MCU commands (EMUX, gate driver) except SPI register commands. This bit will automatically be cleared when the reset signal to the MCU is asserted. 0b: MCU not alive 1b: MCU alive
2	**TPBD**	R/W	0x0	Push-button deglitch time: 0b: 32ms 1b: 1ms
1	**PB_POL**	R/W	0x0	Push-button polarity: 0b: Active-low. The push-button is internally pulled high using a 50k resistor. Drive low externally to wake-up. 1b: Active-high. The push-button is internally pulled down to ground. Drive high externally to wake-up.
0	**SMEN**	R/W	0x0	Signal Manager Enable. This bit is automatically cleared when the reset signal to the MCU is asserted. 0b: Not enabled 1b: Enabled

8.9.4 SOC.PWRCTL

Register 8-4 SOC.PWRCTL (Power Control, 03h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**RFU**	R	0x0	Reserved
5:3	**PWRMON**	R/W	0x0	Power Monitor Signal. This field selects the signal to use for AB11 for ADC monitoring (buffered). 000b: VCORE 001b: VP x 1/10 010b: VCC33 x 4/10 011b: VCCIO x 4/10 100b: VSYS x 4/10 101b: VREF/2 110b: VPTAT 111b: (VCP-VM) x 5/10
2:0	**WUTIMER**	R/W	0x0	Wake-up Timer: 000b: infinite 001b: 8ms 010b: 16ms 011b: 32ms 100b: 64ms 101b: 1s 110b: 2s 111b: 4s

8.9.5 SOC.FAULTINTEN

Register 8-5 SOC.FAULTINTEN (Fault interrupt enable, 04h)

BIT	NAME	ACCESS[2]	RESET	DESCRIPTION
7	**RFU**	R/W	0x0	Reserved
6	**TMPWARNINT**	R/W	0x0	Temperature Warning Interrupt. 0b: Not enabled 1b: Enabled (asserts IRQ1)
5	**VPFLTINT**	R/W	0x0	VP Fault Interrupt Enabled. 0b: Not enabled 1b: Enabled
4	**VSYSFLTINT**	R/W	0x0	VSYS Fault Interrupt Enabled. 0b: Not enabled 1b: Enabled
3	**RFU**	R	0x0	Reserved
2	**LDOFLTINT**	R/W	0x0	LDO Fault Interrupt Enabled for VCCIO, VCC33 and VCORE. 0b: Not enabled 1b: Enabled
1	**PBINT**	R/W	0x0	Push-button Interrupt Enabled. 0b: Not enabled 1b: Enabled (asserts IRQ1)
0	**VPINT**	R/W	0x0	VP Low Interrupt Enabled. 0b: Not enabled 1b: Enabled (asserts IRQ1)

[2] This byte is unlocked for writing when **UNLOCK** = 1b.

8.9.6 SOC.WATCHDOG

Register 8-6 SOC.WATCHDOG (SOC Watchdog Configuration, 05h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**SRST**	R/W	0x0	Soft Reset. This bit can be set to issue a system soft reset. This bit is always read as 0b. When set, the **STATUS.SRST** bit will be latched to a 1b so the MCU knows the system is being started after a soft reset. 0b: Do not issue soft reset 1b: Issue soft reset
6:4	**RFU**	R	0x0	Reserved
3	**WDTEN**	R/W	0x0	Watchdog Timer Enable. Cleared during hard reset. 0b: disabled 1b: enabled
2:0	**TWD**	R/W	0x0	Watch-dog Timer. 000b: 62.5ms 001b: 125ms 010b: 250ms 011b: 500ms 100b: 1s 101b: 2s 110b: 4s 111b: 8s

8.9.7 SOC.SYSCONF

Register 8-7 SOC.SYSCONF (System Configuration, 2Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**RFU**	R	0011 0b	Reserved
2	**VPSET**	R/W	1b	VP Output Voltage Setting. 0b: 10V 1b: 12V (default)
1	**MVBB_ILIM**	R/W	0b	MVBB Inductor Current Limit Range: 0b: 440mA-540mA (default) 1b: 600mA-750mA
0	**CP_EN**	R/W	1b	Charge Pump Enable: 0b: Disabled 1b: Enabled

9 CONFIGURABLE ANALOG FRONT-END

9.1 Overview

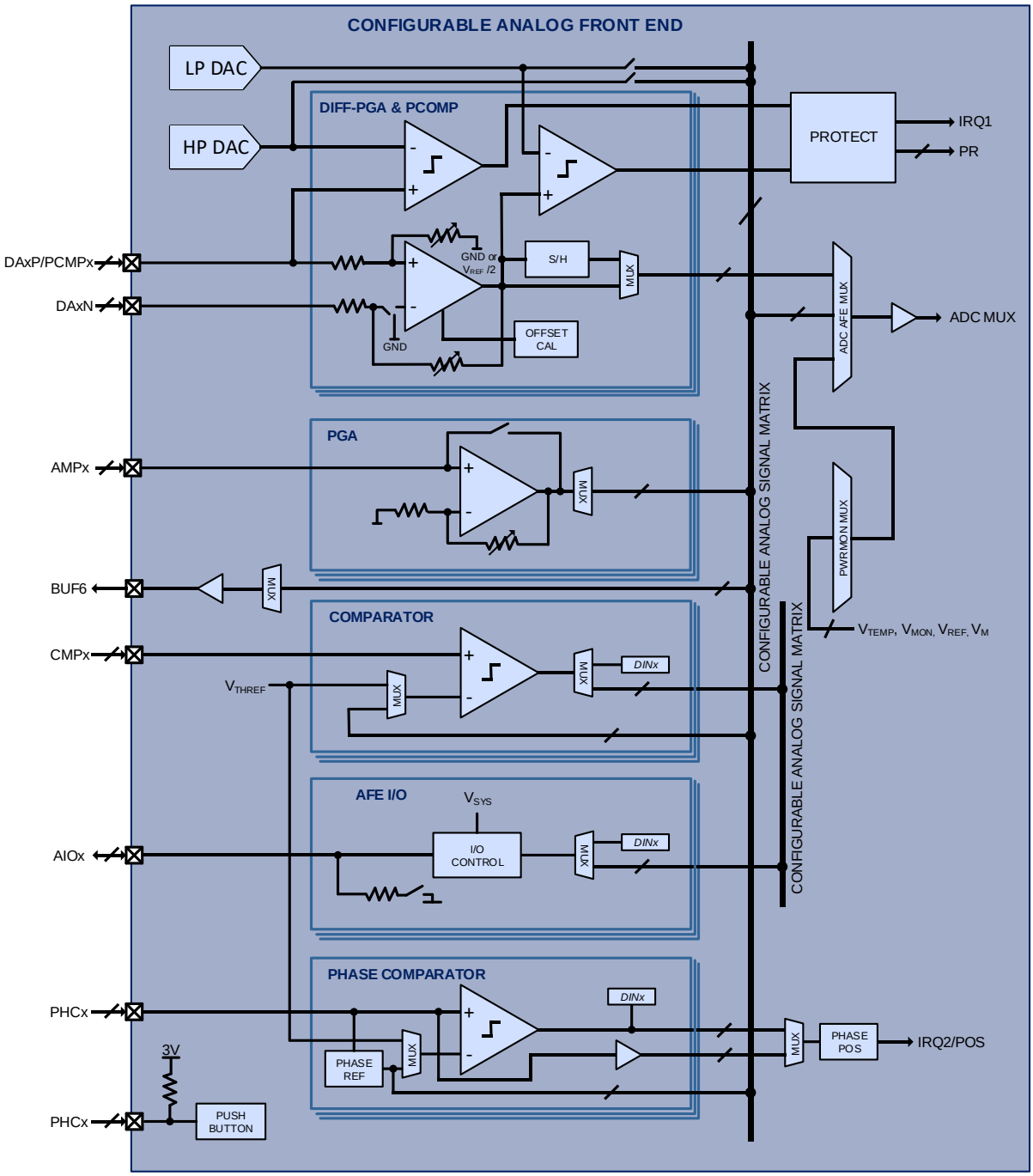
The PAC5527 includes a Configurable Analog Front End accessible through 8 analog and I/O pins. These pins can be configured to form flexible interconnected circuitry made up of 3 differential programmable gain amplifiers, 4 single-ended programmable gain amplifiers, 4 general purpose comparators, 3 phase comparators, 10 protection comparators, and one buffer output. These pins can also be programmed as analog feed-through pins, or as analog front end I/O pins that can function as digital inputs or digital open-drain outputs. The PAC proprietary configurable analog signal matrix (CASM) and configurable digital signal matrix (CDSM) allow real time asynchronous analog and digital signals to be routed in flexible circuit connections for different applications. A push button function is provided for optional push button on, hibernate, and off power management function.

9.2 Features

- 10 Analog Front-End IO pins
- 3 Differential Programmable Gain Amplifiers (Differential or Single-ended mode)
- 7 Single-ended Programmable Gain Amplifiers
- Programmable Over-Current Protection and Current Limit
- 10 Comparators
- 2 10-bit DACs
- Buffered output on AIO2 or AIO7
- V_{REF} Buffered output
- DAC output to pin
- Hibernate Mode and Hibernate Wake-up using timer or push-button

9.3 System Block Diagram

Figure 9-1 CAFE System Block Diagram



9.4 Enabling the CAFE

Before the CAFE sub-system can sampling signals, it must be enabled. To enable this sub-system, set **SOC.MISC.SMEN** to 1b.

9.5 Entering Hibernate Mode

Hibernate mode on the PAC5527 allows a very low I_Q mode when not in operation to minimize energy consumption of the battery.

To enter hibernate mode, the set **SOC.MISC.HIB** to 1b. This bit will be automatically cleared when the power-up sequence is initiated, or in hibernate mode after the wake-up timer delay or after push-button wake-up.

To wake-up from hibernate mode the user may either use the Hibernate Wake-up Timer or the Push-button function. Before entering hibernate mode, one of these two methods must be configured or the PAC5527 will not be able to exit hibernate mode.

9.6 Hibernate wake-up using Wake-Up Timer

To wake up from hibernate mode using the wake-up timer, set **SOC.PWRCTL.WUTIMER** to the desired value from the table below.

Table 9-1 Hibernate Wake-Up Timer Options

REGISTER VALUE	WAKE-UP TIME
000b	Infinite (never wakes up)
001b	8ms
010b	16ms
011b	32ms
100b	64ms
101b	1s
110b	2s
111b	4s

9.7 Hibernate wake-up using Push-Button

When the PAC5527 is in hibernate mode, the AIO6 push-button may be used to wake up the device. To enable the push-button wake-up using AIO6, the device must be in AIO6 special mode with the push-button enabled. To configure and enable the push-button mode, set **SOC.CFGAIO6.MODE6** = 11b and **SOC.MISC.PBEN** = 0b.

When in push-button mode, the polarity of the push-button detection may be configured to be active-low or active-high. To configure the push-button polarity for active-low set **SOC.CFGAIO6.PB_POL** to 0b and to configure the push-button polarity for active-high set **SOC.CFGAIO6.PB_POL** to 1b.

When configured for active-low, AIO6 is pulled up using a 50k weak pull-up. When configured for active-high, AIO6 is pulled down to ground using a 300k pull-down. These pull-up and pull-down resistors are active as soon as the push-button is enabled after **SOC.MISC.PBEN** is set to 1b.

There is a de-bouncing time used for the push-button detection. Before entering hibernate mode, set the de-bouncing time by setting **SOC.MISC.TPBD** to 0b for 32ms or 1b for 1ms. After the de-bouncing time has expired and the push-button is detected, the real-time status of the push-button will be available in **SOC.STATUS.PBSTAT**. The latched status of the push-button will be available in **SOC.STATUS.PBSTAT_LATCHED**, which is also used to generate the IRQ1 interrupt to the MCU. To de-assert this interrupt, set **SOC.STATUS.PBSTAT_LATCHED** to 1b.

If the PAC5527 is in hibernate and AIO6 transitions high for the de-bouncing time period, the **SOC.MISC.HIB** is cleared and the device powers up.

9.8 DAC output

The output of the HPDAC and LPDAC may be connected to the analog bus through register configuration.

To connect HPDAC to AB2, set **SOC.HPDACAB2** to 1b. To connect LPDAC to AB3, set **SOC.LPDACAB3** to 1b.

9.9 VREF Output

The user may configure the CAFE to output the V_{REF} onto the ABUS AB5 channel by setting **SOC.CFGIO1.VREFBP** to 1b. When set, this will output the configured VREF from **SOC.MISC.VREFSET** (2.5V or 3.0V) to be output on AB5.

9.10 Hard Reset

A hard reset of the PAC5527 may be performed by pulling the AIO6 input low for more than 8 seconds when the AIO6 push-button mode is enabled.

When this is detected, the reset signal to the MCU will be asserted and **SOC.STATUS.HWRSTAT** will be set to 1b to indicate this condition.

9.11 General-Purpose Register

The PAC5527 contains an 8-bit general-purpose register in the analog sub-system that is available for user applications. This register may be used to synchronize information between the MCU and analog sub-system for the application.

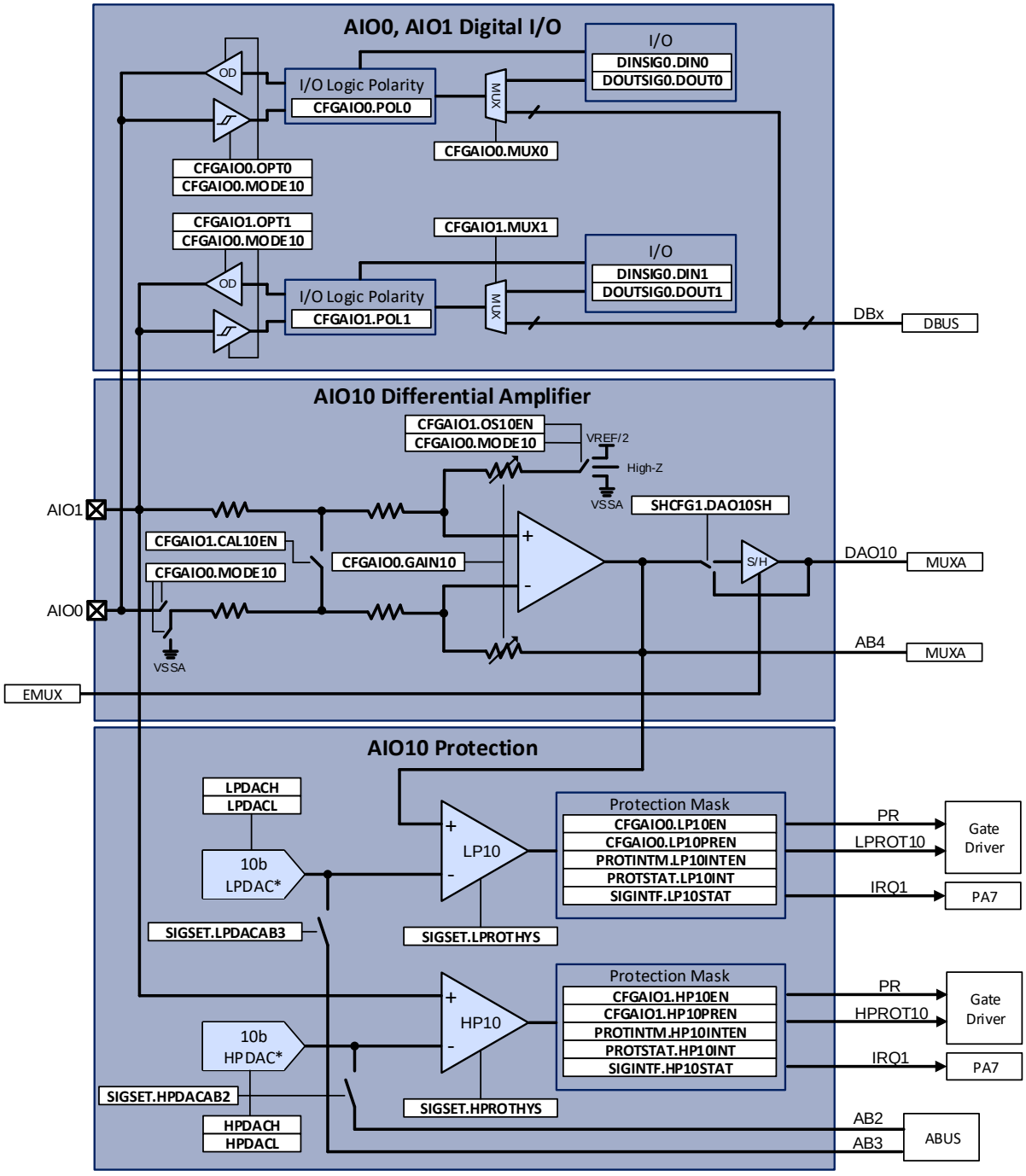
The user may read or write this register at **SOC.GP0**.

9.12 AIO10

AIO10 may be configured as a pair of digital I/O or as a differential amplifier with protection.

9.12.1 System Block Diagram

Figure 9-2 AIO10 Block Diagram



* Common DAC for AIO10, AIO32 and AIO54

9.12.2 AIO1, AIO0 Digital I/O Mode

To configure AIO0 and AIO1 as digital I/O, set **SOC.CFGAIO0.MODE10** = 00b.

9.12.2.1 AIO0 Digital I/O

Set **SOC.CFGAIO0.OPT0** = 00b to use AIO0 as a digital input. The input state can be read at **SOC.DINSIG0.DIN0**.

Set **SOC.CFGAIO0.OPT0** = 10b to use AIO0 as open-drain output. Set **SOC.CFGAIO0.MUX0** = 00b to mux the output state from **SOC.DOUTSIG0.DOUT0**. Use **SOC.CFGAIO0.MUX0** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

To configure the input or output polarity of AIO0, use **SOC.CFGAIO0.POL0** to set logic polarity of the signal between AIO0 input/output and MUX0.

9.12.2.2 AIO1 Digital I/O

Set **SOC.CFGAIO1.OPT1** = 00b to use AIO1 as a digital input. The input state can be read at **SOC.DINSIG0.DIN1**.

Set **SOC.CFGAIO1.OPT1** = 10b to use AIO1 as open-drain output. Set **SOC.CFGAIO1.MUX1** = 00b to mux the output state from **SOC.DOUTSIG0.DOUT1**. Use **SOC.CFGAIO1.MUX1** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

To configure the input or output polarity of AIO1, use **SOC.CFGAIO1.POL1** to set logic polarity of the signal between AIO1 input/output and MUX1.

9.12.3 AIO1, AIO0 Differential Amplifier Mode

The differential amplifier may be configured as a differential amplifier or as an infinite-impedance single-ended amplifier. To configure as a differential amplifier, set **SOC.CFGAGIO0.MODE10** = 01b. To configure as a single-ended amplifier, set **SOC.CFGAIO0.MODE10** = 10b.

In differential mode, AIO0 is connected to the negative terminal of the amplifier and AIO1 is connected to the positive terminal of the amplifier. The reference for the amplifier is programmable. **SOC.CFGAIO1.OS10EN** may be used to set the amplifier reference either VSSA or VREF/2. Use **SOC.CFGAIO1.CAL10EN** to short the inputs of the differential amplifier to allow reading of the amplifier offset.

In single-ended mode, AIO1 is connected to the positive terminal of the amplifier and AIO0 is not used. The negative terminal of the amplifier is internally shorted to VSSA and the amplifier is put into a high-impedance state.

In both differential and single-ended mode, the amplifier gain may be set between 1X and 16X by using **SOC.CFGAIO0.GAIN10**.

9.12.4 AIO1, AIO0 ADC Sampling

When the ADC is in automatic mode and the DTSE is active, the EMUX is used to communicate data to the CAFE to select the ADC AFE MUX channel as well as activate and deactivate the sample and hold

engines for the differential amplifier output. To enable the EMUX set **SOC.SHCFG1.EMUXEN** to 1b. The EMUX state machine may be reset at any time by setting **SOC.SHCFG1.EMUXEN** to 0b.

In either ADC automatic or manual mode, the ADC buffer must be enabled by setting **SOC.SHCFG1.ADCBUFEN** to 1b before sampling using the ADC.

Each differential amplifier has a dedicated sample and hold engine that may be enabled and disabled manually or by the DTSE using the EMUX. To synchronize the output of the sample and hold circuit for DAO10 to the ADC AFE MUX set **SOC.SHCFG1.DAO10SH** to 1b. To bypass the sample and hold circuit for DAO10 to the ADC AFE MUX set **SOC.SHCFG1.DAO10SH** to 0b. The raw output of the differential amplifier is always available on AB4.

When the ADC in is manual mode (DTSE not active), the sample and hold circuit may be activated by writing **SOC.SHCFG2.HLD0** to a 1b (hold) and de-activated by writing **SOC.SHCFG2.HLD0** to a 0b (release). The ADC AFE MUX channel may be selected by writing **SOC.SHCFG2.MUXA** to the desired channel.

When the ADC is in automatic mode (DTSE active), the sample and hold state as well as the ADC AFE MUX channel may be commanded using data from the EMUX, which is sent by the ADC DTSE. The data is 8b and the format of the bits are the same as shown in **SOC.SHCFG2**.

9.12.5 AIO1, AIO0 Protection

In differential amplifier mode (**SOC.CFGAIO0.MODE10** = 01b), a high side comparator protector HP10 and a low side comparator protector LP10 are also active that can be configured to disable high-side or low-side gate drivers in the Application-Specific Power Driver (ASPD).

9.12.5.1 HP10 Comparator

The HP10 comparator takes the AIO1 voltage and compares it against the HP-DAC voltage. The 10-bit HP-DAC value is programmable using **SOC.HPDACH** and **SOC.HPDACL**. **SOC.CFGAIO1.HP10EN** may be used to enable the HP10 comparator with different blanking times. Set **SOC.SIGSET.HPROTHYS** to 1b to enable HP10 comparator hysteresis.

The output of HP10 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO1.HP10PREN**.

The output of HP10 can also trigger the IRQ1 interrupt by setting **SOC.PROTINTEN.HP10INTEN** to 1b. The real-time status can be observed using **SOC.SIGINTF.HP10STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.HP10INT**.

9.12.5.2 LP10 Comparator

The LP10 comparator takes the output of the differential amplifier and compares it against the LP-DAC voltage. The 10-bit LP-DAC value is programmable using **SOC.LPDACH** and **SOC.LPDACL**. **SOC.CFGAIO0.LP10EN** may be used to enable LP10 comparator with different blanking times. Set **SOC.SIGSET.LPROTHYS** to 1b to enable LP10 comparator hysteresis.

The output of LP10 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO1.LP10PREN**.

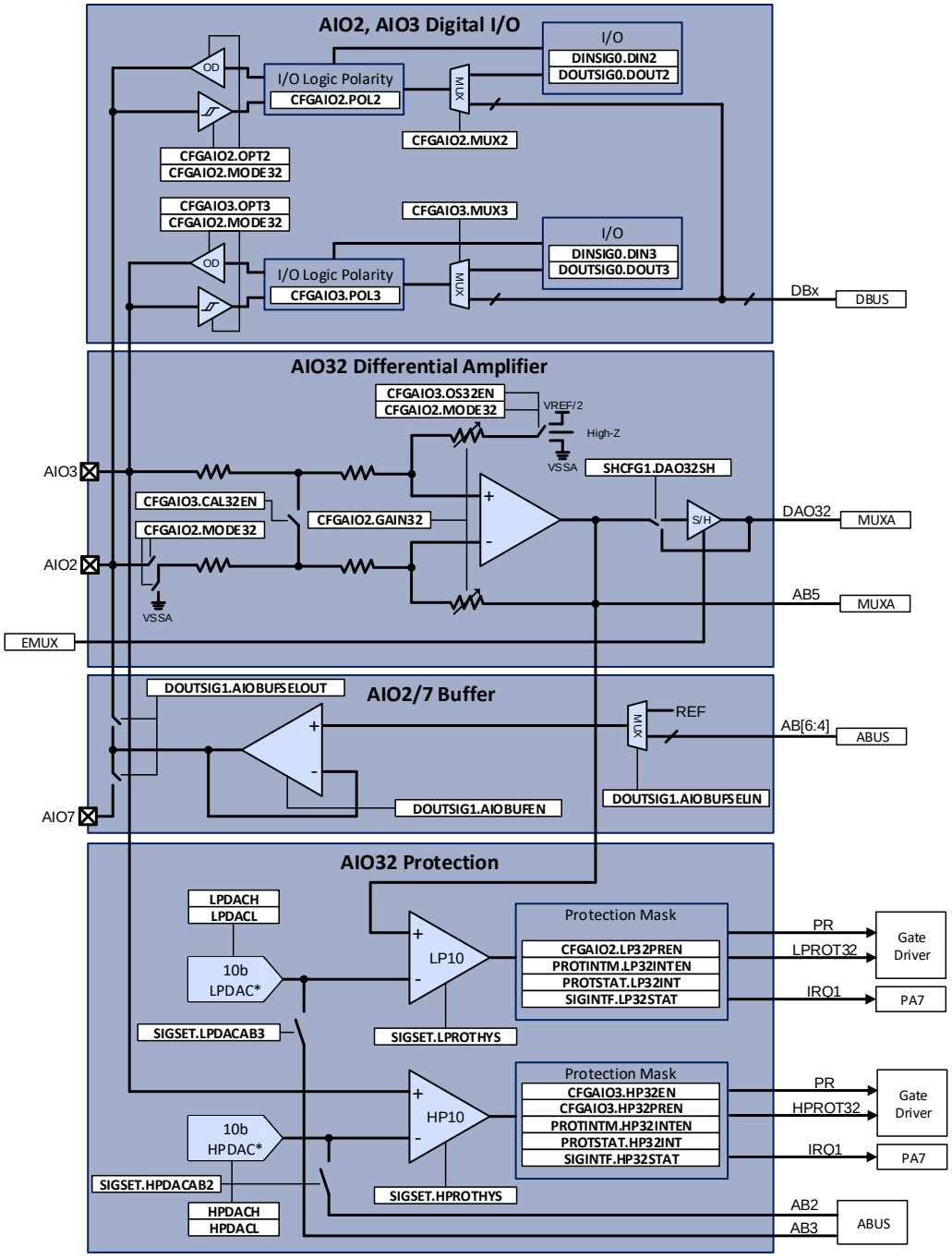
The output of LP10 can also trigger the IRQ1 interrupt by setting **SOC.PROTINTEN.LP10INTEN** to 1b. The real-time status can be observed using **SOC.SIGINTF.LP10STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.LP10INT**.

9.13 AIO32

AIO32 may be configured as a pair of digital I/O or as a differential amplifier with protection.

9.13.1 System Block Diagram

Figure 9-3 AIO32 Block Diagram



* Common DAC for AIO10, AIO32 and AIO54

9.13.2 AIO3, AIO2 Digital I/O Mode

To configure AIO3 and AIO2 as digital I/O, set **SOC.CFGAIO2.MODE32** = 00b.

9.13.2.1 AIO2 Digital I/O

Set **SOC.CFGAIO2.OPT2** = 00b to use AIO2 as a digital input. The input state can be read at **SOC.DINSIG0.DIN2**.

Set **SOC.CFGAIO2.OPT2** = 10b to use AIO2 as open-drain output. Set **SOC.CFGAIO2.MUX2** = 000b to mux the output state from **SOC.DOUTSIG0.DOUT2**. Use **SOC.CFGAIO2.MUX2** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

To configure the input or output polarity of AIO2, use **SOC.CFGAIO2.POL2** to set logic polarity of the signal between AIO2 input/output and MUX2.

9.13.2.2 AIO3 Digital I/O

Set **SOC.CFGAIO3.OPT3** = 00b to use AIO3 as a digital input. The input state can be read at **SOC.DINSIG0.DIN3**.

Set **SOC.CFGAIO3.OPT3** = 10b to use AIO3 as open drain output. Set **SOC.CFGAIO3.MUX3** = 00b to MUX the output state from **SOC.DOUTSIG0.DOUT3**. Use **SOC.CFGAIO3.MUX3** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

To configure the input or output polarity of AIO3, use **SOC.CFGAIO3.POL3** to set logic polarity of the signal between AIO3 input/output and MUX3.

9.13.3 AIO3, AIO2 Differential Amplifier Mode

The differential amplifier may be configured as a differential amplifier or as an infinite-impedance single-ended amplifier. To configure as a differential amplifier, set **SOC.CFGAGIO2.MODE32** = 01b. To configure as a single-ended amplifier, set **SOC.CFGAIO2.MODE32** = 10b.

In differential mode, AIO2 is connected to the negative terminal of the amplifier and AIO3 is connected to the positive terminal of the amplifier. The reference for the amplifier is programmable. **SOC.CFGAIO3.OS32EN** may be used to set the amplifier reference either VSSA or VREF/2. Use **SOC.CFGAIO3.CAL32EN** to short the inputs of the differential amplifier to allow reading of the amplifier offset.

In single-ended mode, AIO3 is connected to the positive terminal of the amplifier and AIO2 is not used. The negative terminal of the amplifier is internally shorted to VSSA and the amplifier is put into a high-impedance state.

In both differential and single-ended mode, the amplifier gain may be set between 1X and 16X by using **SOC.CFGAIO2.GAIN32**.

9.13.4 AIO3, AIO2 ADC Sampling

When the ADC is in automatic mode and the DTSE is active, the EMUX is used to communicate data to the CAFE to select the ADC AFE MUX channel as well as activate and deactivate the sample and hold

engines for the differential amplifier output. To enable the EMUX set **SOC.SHCFG1.EMUXEN** to 1b. The EMUX state machine may be reset at any time by setting **SOC.SHCFG1.EMUXEN** to 0b.

In either ADC automatic or manual mode, the ADC buffer must be enabled by setting **SOC.SHCFG1.ADCBUFEN** to 1b before sampling using the ADC.

Each differential amplifier has a dedicated sample and hold engine that may be enabled and disabled manually or by the DTSE using the EMUX. To synchronize the output of the sample and hold circuit for DAO32 to the ADC AFE MUX set **SOC.SHCFG1.DAO32SH** to 1b. To bypass the sample and hold circuit for DAO32 to the ADC AFE MUX set **SOC.SHCFG1.DAO32SH** to 0b. The raw output of the differential amplifier is always available on AB5.

When the ADC in is manual mode (DTSE not active), the sample and hold circuit may be activated by writing **SOC.SHCFG2.HLD1** to a 1b (hold) and de-activated by writing **SOC.SHCFG2.HLD1** to a 0b (release). The ADC AFE MUX channel may be selected by writing **SOC.SHCFG2.MUXA** to the desired channel.

When the ADC is in automatic mode (DTSE active), the sample and hold state as well as the ADC AFE MUX channel may be commanded using data from the EMUX, which is sent by the ADC DTSE. The data is 8b and the format of the bits are the same as shown in **SOC.SHCFG2**.

9.13.5 AIO3, AIO2 Protection

In differential amplifier mode (**SOC.CFGAIO2.MODE32** = 01b), a high side comparator protector HP32 and a low side comparator protector LP32 are also active that can be configured to disable high-side or low-side gate drivers in the Application-Specific Power Driver (ASPD).

9.13.5.1 HP32 Comparator

The HP32 comparator takes the AIO3 voltage and compares it against the HP-DAC voltage. The 10-bit HP-DAC value is programmable using **SOC.HPDACH** and **SOC.HPDACL**. **SOC.CFGAIO3.HP32EN** may be used to enable the HP32 comparator with different blanking times. Set **SOC.SIGSET.HPROTHYS** to 1b to enable HP32 comparator hysteresis.

The output of HP32 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO3.HP32PREN**.

The output of HP32 can also trigger the IRQ1 interrupt by setting **SOC.PROTINTEN.HP32INTEN** to 1b. The real-time status can be observed using **SOC.SIGINTF.HP32STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.HP32INT**.

9.13.5.2 LP32 Comparator

The LP32 comparator takes the output of the differential amplifier and compares it against the LP-DAC voltage. The 10-bit LP-DAC value is programmable using **SOC.LPDACH** and **SOC.LPDACL**. **SOC.CFGAIO2.LP32EN** may be used to enable LP32 comparator with different blanking times. Set **SOC.SIGSET.LPROTHYS** to 1b to enable LP32 comparator hysteresis.

The output of LP32 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO3.LP32PREN**.

The output of LP32 can also trigger the IRQ1 interrupt by setting **SOC.PROTINTEN.LP32INTEN** to 1b. The real-time status can be observed using **SOC.SIGINTF.LP32STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.LP32INT**.

9.13.6 AIO2/AIO7 Buffer

There is an output buffer that may be used for either AIO2 or AIO7 in the PAC5527 CAFE. To enable this buffer, set **SOC.DOUTSIG1.AIOBUFEN** = 1b.

The input signal for this buffer may be selected by using **SOC.DOUTSIG1.AIOBUFSELIN** with the values below.

Table 9-2 AIO2/AIO7 Buffer Input Select

SOC.DOUTSIG1.AIOBUFSELIN	SIGNAL
00b	ADC VREF (2.5V or 3.0V as selected by **SOC.MISC.VREFSET**).
01b	AB4
10b	AB5
11b	AB6

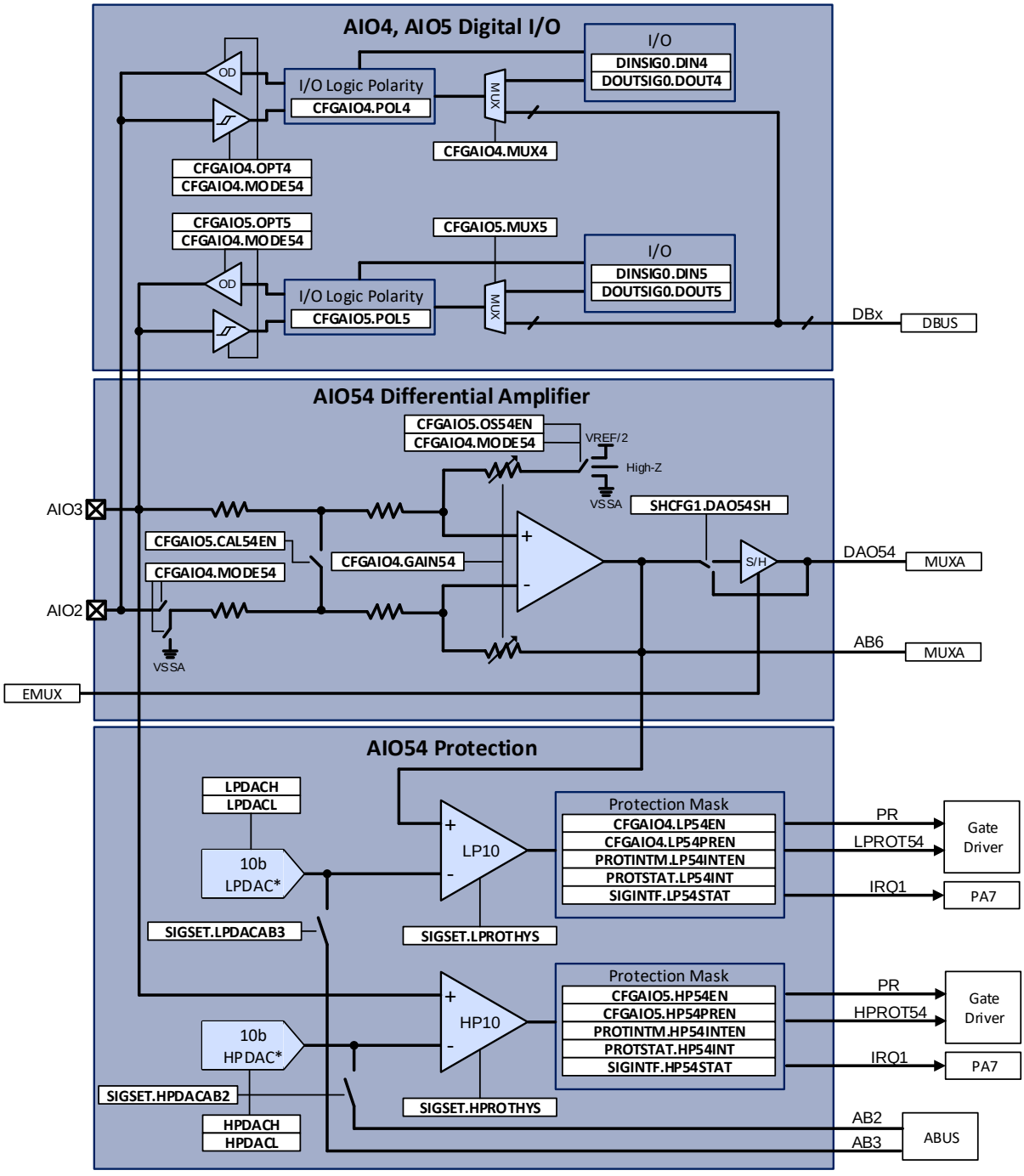
The output of this buffer may be configured to be AIO2 or AIO7. To configure the output of the buffer to be AIO2, set **SOC.DOUTSIG1.AIOBUFSELOUT** to be 0b. To configure the output of the buffer to be AIO7, set **SOC.DOUTSIG1.AIOBUFSELOUT** to be 1b.

9.14 AIO54

AIO54 may be configured as a pair of digital I/O or as a differential amplifier with protection.

9.14.1 System Block Diagram

Figure 9-4 AIO54 Block Diagram



* Common DAC for AIO10, AIO32 and AIO54

9.14.2 AIO5, AIO4 Digital I/O Mode

To configure AIO4 and AIO5 as digital I/O, set **SOC.CFGAIO4.MODE54** = 00b.

9.14.2.1 AIO4 Digital I/O

Set **SOC.CFGAIO4.OPT4** = 00b to use AIO4 as a digital input. The input state can be read at **SOC.DINSIG0.DIN4**.

Set **SOC.CFGAIO4.OPT4** = 10b to use AIO4 as open-drain output. Set **SOC.CFGAIO4.MUX4** = 00b to mux the output state from **SOC.DOUTSIG0.DOUT4**. Use **SOC.CFGAIO4.MUX4** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

To configure the input or output polarity of AIO4, use **SOC.CFGAIO4.POL4** to set logic polarity of the signal between AIO4 input/output and MUX4.

9.14.2.2 AIO5 Digital I/O

Set **SOC.CFGAIO5.OPT5** = 00b to use AIO5 as a digital input. The input state can be read at **SOC.DINSIG0.DIN5**.

Set **SOC.CFGAIO5.OPT5** = 10b to use AIO5 as open-drain output. Set **SOC.CFGAIO5.MUX5** = 00b to MUX the output state from **SOC.DOUTSIG0.DOUT5**. Use **SOC.CFGAIO5.MUX5** to MUX the output signal from the internal digital bus DBUS DB1 to DB7.

To configure the input or output polarity of AIO5, use **SOC.CFGAIO5.POL5** to set logic polarity of the signal between AIO5 input/output and MUX5.

9.14.3 AIO4, AIO5 Differential Amplifier Mode

The differential amplifier may be configured as a differential amplifier or as an infinite-impedance single-ended amplifier. To configure as a differential amplifier, set **SOC.CFGAGIO4.MODE54** = 01b. To configure as a single-ended amplifier, set **SOC.CFGAIO4.MODE54** = 10b.

In differential mode, AIO4 is connected to the negative terminal of the amplifier and AIO5 is connected to the positive terminal of the amplifier. The reference for the amplifier is programmable. **SOC.CFGAIO5.OS54EN** may be used to set the amplifier reference either VSSA or VREF/2. Use **SOC.CFGAIO5.CAL54EN** to short the inputs of the differential amplifier to allow reading of the amplifier offset.

In single-ended mode, AIO5 is connected to the positive terminal of the amplifier and AIO4 is not used. The negative terminal of the amplifier is internally shorted to VSSA and the amplifier is put into a high-impedance state.

In both differential and single-ended mode, the amplifier gain may be set between 1X and 16X by using **SOC.CFGAIO4.GAIN54**.

9.14.4 AIO5, AIO4 ADC Sampling

When the ADC is in automatic mode and the DTSE is active, the EMUX is used to communicate data to the CAFE to select the ADC AFE MUX channel as well as activate and deactivate the sample and hold

engines for the differential amplifier output. To enable the EMUX set **SOC.SHCFG1.EMUXEN** to 1b. The EMUX state machine may be reset at any time by setting **SOC.SHCFG1.EMUXEN** to 0b.

In either ADC automatic or manual mode, the ADC buffer must be enabled by setting **SOC.SHCFG1.ADCBUFEN** to 1b before sampling using the ADC.

Each differential amplifier has a dedicated sample and hold engine that may be enabled and disabled manually or by the DTSE using the EMUX. To synchronize the output of the sample and hold circuit for DAO54 to the ADC AFE MUX set **SOC.SHCFG1.DAO54SH** to 1b. To bypass the sample and hold circuit for DAO54 to the ADC AFE MUX set **SOC.SHCFG1.DAO54SH** to 0b. The raw output of the differential amplifier is always available on AB6.

When the ADC in is manual mode (DTSE not active), the sample and hold circuit may be activated by writing **SOC.SHCFG2.HLD2** to a 1b (hold) and de-activated by writing **SOC.SHCFG2.HLD2** to a 0b (release). The ADC AFE MUX channel may be selected by writing **SOC.SHCFG2.MUXA** to the desired channel.

When the ADC is in automatic mode (DTSE active), the sample and hold state as well as the ADC AFE MUX channel may be commanded using data from the EMUX, which is sent by the ADC DTSE. The data is 8b and the format of the bits are the same as shown in **SOC.SHCFG2**.

9.14.5 AIO5, AIO4 Protection

In differential amplifier mode (**SOC.CFGAIO4.MODE54** = 01b), a high side comparator protector HP54 and a low side comparator protector LP54 are also active that can be configured to disable high-side or low-side gate drivers in the Application-Specific Power Driver (ASPD).

9.14.5.1 HP54 Comparator

The HP54 comparator takes the AIO5 voltage and compares it against the HP-DAC voltage. The 10-bit HP-DAC value is programmable using **SOC.HPDACH** and **SOC.HPDACL**. **SOC.CFGAIO5.HP54EN** may be used to enable the HP54 comparator with different blanking times. Set **SOC.SIGSET.HPROTHYS** to 1b to enable HP54 comparator hysteresis.

The output of HP54 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO5.HP54PREN**.

The output of HP54 can also trigger the IRQ1 interrupt by setting **SOC.PROTINTEN.HP54INTEN** to 1b. The real-time status can be observed using **SOC.PROTSTAT.HP54STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.HP54INT**.

9.14.5.2 LP10 Comparator

The LP54 comparator takes the output of the differential amplifier and compares it against the LP-DAC voltage. The 10-bit LP-DAC value is programmable using **SOC.LPDACH** and **SOC.LPDACL**. **SOC.CFGAIO5.LP54EN** may be used to enable LP54 comparator with different blanking times. Set **SOC.SIGSET.LPROTHYS** to 1b to enable LP54 comparator hysteresis.

The output of LP54 comparator can be configured to trigger protection signal PR using **SOC.CFGAIO5.LP54PREN**.

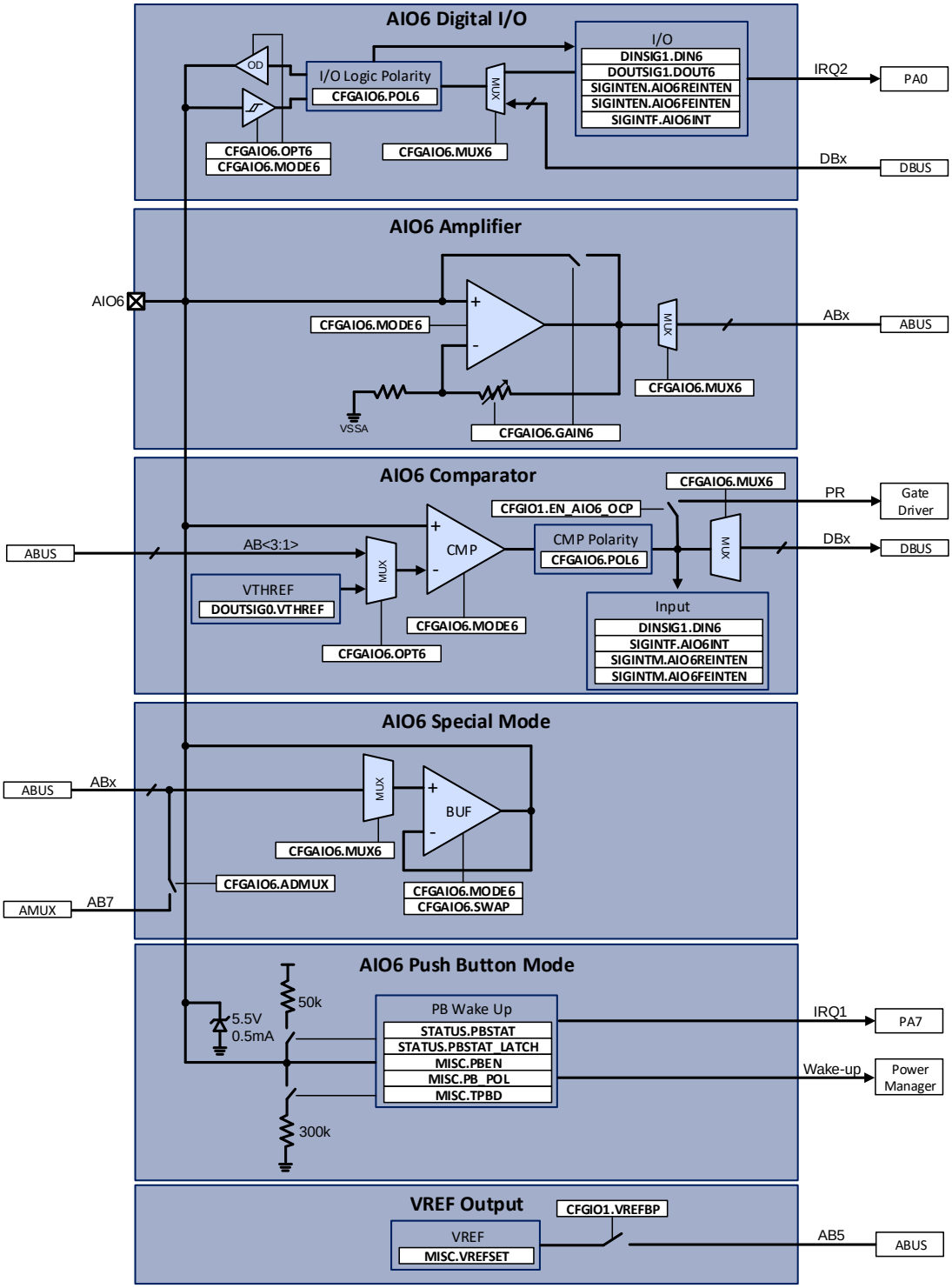
The output of LP54 can also trigger the IRQ1 interrupt by setting **SOC.PROTINTEN.LP54INTEN** to 1b. The real-time status can be observed using **SOC.PROTSTAT.LP54STAT** and the latched interrupt status can be observed using **SOC.PROTSTAT.LP54INT**.

9.15 AIO6

AIO6 may be configured as a digital input, single-ended programmable gain amplifier, comparator, output from analog ABUS or as a push-button input to wake up the device from total hibernate mode.

9.15.1 System Block Diagram

Figure 9-5 AIO6 System Block Diagram



9.15.2 AIO6 Digital I/O Mode

In AIO6 digital I/O mode the push-button function must be disabled. To configure AIO6 for digital I/O mode, set **SOC.MISC.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 00b.

Set **SOC.CFGAIO6.OPT6** = 10b to use AIO6 as an open-drain output. Set **SOC.CFGAIO6.MUX6** = 000b to mux the output state from **SOC.DOUTSIG1.DOUT6**. Use **SOC.CFGAIO6.MUX6** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

Set **SOC.CFGAIO6.OPT6** = 00b to use AIO6 as a digital input. The state can be read from **SOC.DINSIG1.DIN6**.

To configure the input or output polarity of AIO6, use **SOC.CFGAIO6.POL6** to set logic polarity of the signal between AIO6 input/output and MUX6.

To enable interrupts for low to high transitions on AIO6, set **SOC.SIGINTEN.AIO6REINTEN** to 1b. To enable interrupts for high to low transitions on AIO6, set **SOC. SIGINTEN.AIO6FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO6INT** and cleared by writing **SOC.SIGINTF.AIO6INTF** to 1b.

9.15.3 AIO6 Amplifier Mode

In AIO6 amplifier mode the push-button function must be disabled. To configure AIO6 for amplifier mode set **SOC.MISC.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 01b.

Use **SOC.CFGAIO6.GAIN6** to set the amplifier gain from 1x to 48x or to bypass mode. Use **SOC.CFGAIO6.MUX6** to switch the output of the amplifier to analog channel AB1 to AB7 on the analog bus ABUS.

9.15.4 AIO6 Comparator Mode

In AIO6 comparator mode the push-button function must be disabled. Set **SOC.MISC.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 10b to use AIO6 in comparator mode.

The comparator reference may be selected from AB<3:1> or from a programmable comparator threshold voltage (VTHREF). Set **SOC.CFGAIO6.OPT6** to select the comparator reference. To select the VTHREF comparator threshold use **SOC.DOUTSIG0.VTHREF** to select a value from the following:

- 00b: 0.1V
- 01b: 0.2V
- 10b: 0.5V
- 11b: 1.25V

The output polarity of the comparator may be selected by using **SOC.CFGAIO6.POL6** (0b: active-high; 1b: active-low).

The output of the comparator may be sent to the digital bus DB1 to DB7 or to **SOC.DINSIG1.DIN6** by using **SOC.CFGAIO6.MUX6**.

In this mode, the digital input state and input interrupts are also available. To enable interrupts for low to high transitions on AIO6, set **SOC.SIGINTEN.AIO6REINTEN** to 1b. To enable interrupts for high to low transitions on AIO6, set **SOC.SIGINTEN.AIO6FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO6INT** and cleared by writing **SOC.SIGINTF.AIO6INTF** to 1b.

In this mode, AIO6 may also be used to detect an over-current event, and to notify the ASPD to disable the gate drivers, much like the differential amplifier mode. To signal the ASPD upon the comparator output state, set **SOC.CFGIO1.EN_AIO6_OCP** to 1b. This will send the PR signal to the ASPD.

9.15.5 AIO6 Special Mode

In special mode the AIO6 can output a buffered signal from the internal ABUS, AB1 to AB7. Set **SOC.MISC.PBEN** = 0b and **SOC.CFGAIO6.MODE6** = 11b to use AIO6 in special mode.

The input to the AIO6 special mode buffer may also be sent to the AFE MUX on AB7. To send the ABUS signal to the AFE MUX for ADC sampling, set **CFGAIO6.ADMUX** to 1b.

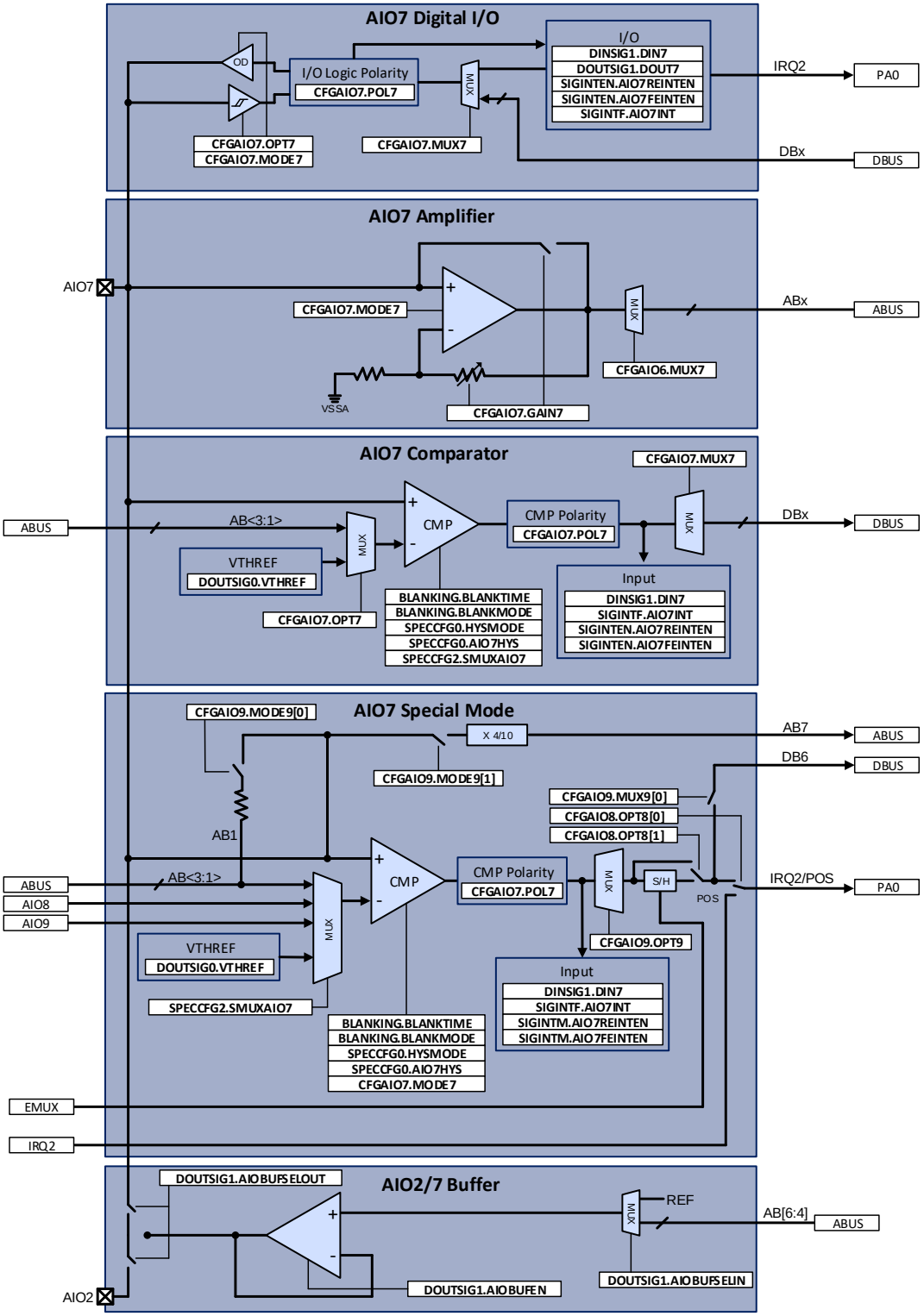
To configure the ABUS input to the AIO6 special mode buffer (AB1 – AB7), use **SOC.CFGAIO6.MUX6**. The **SOC.CFGAIO6.SWAP** to 1b to swap the random offset of the buffer for calibration.

9.16 AIO7

AIO7 may be configured as a digital input/output, single-ended programmable gain amplifier, comparator or a BEMF zero-cross comparator.

9.16.1 System Block Diagram

Figure 9-6 AIO7 System Block Diagram



9.16.2 AIO7 Digital I/O Mode

To configure AIO7 for digital I/O mode, set **SOC.CFGAIO7.MODE7** = 00b.

Set **SOC.CFGAIO7.OPT7** = 10b to use AIO7 as an open-drain output. Set **SOC.CFGAIO7.MUX7** = 000b to mux the output state from **SOC.DOUTSIG1.DOUT7**. Use **SOC.CFGAIO7.MUX7** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

Set **SOC.CFGAIO7.OPT7** = 00b to use AIO7 as a digital input. The state can be read from **SOC.DINSIG1.DIN7**.

To configure the input or output polarity of AIO7, use **SOC.CFGAIO7.POL7** to set logic polarity of the signal between AIO7 input/output and MUX7.

To enable interrupts for low to high transitions on AIO7, set **SOC.SIGINTEN.AIO7REINTEN** to 1b. To enable interrupts for high to low transitions on AIO7, set **SOC. SIGINTEN.AIO7FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO7INT** and cleared by writing **SOC.SIGINTF.AIO7INTF** to 1b.

9.16.3 AIO7 Amplifier Mode

To configure AIO7 for amplifier mode set **SOC.CFGAIO7.MODE7** = 01b. In amplifier mode, the AIO7 gain amplifier is enabled.

Use **SOC.CFGAIO7.GAIN7** to set the amplifier gain from 1x to 48x or to bypass mode. Use **SOC.CFGAIO7.MUX7** to switch the output of the amplifier to analog channel AB1 to AB7 on the analog bus ABUS.

9.16.4 AIO7 Comparator Mode

Set **SOC.CFGAIO7.MODE7** = 10b to use AIO7 in comparator mode. In comparator mode, the AIO7 general-purpose comparator is enabled.

9.16.4.1 Comparator Reference

The comparator reference may be selected from AB<3:1> or from a programmable comparator threshold voltage (VTHREF). Set **SOC.CFGAIO7.OPT7** to select the comparator reference. To select the VTHREF comparator threshold use **SOC.DOUTSIG0.VTHREF** to select a value from the following:

- 00b: 0.1V
- 01b: 0.2V
- 10b: 0.5V
- 11b: 1.25V

9.16.4.2 Comparator Configuration

The AIO7 comparator has programmable blanking time and hysteresis modes.

The blanking time for the comparator may be configured to use leading edge, trailing edge, leading/trailing edge or no blanking by using **SOC.BLANKING.BLANKMODE**. If **SOC.BLANKING.BLANKMODE** is not 00b (disabled), then the blanking time may be configured to be between 100ns and 6000ns by setting the value in **SOC.BLANKING.BLANKTIME**.

The comparator hysteresis may be configured independently for rising and falling input (asymmetric and bi-directional). To set the comparator hysteresis scale for AIO7, set **SOC.SPECCFG0.HYSMODE** and to set the hysteresis level set **SOC.SPECCFG0.AIO7HYS**.

The output polarity of the comparator may be selected by using **SOC.CFGAIO7.POL7** (0b: active-high; 1b: active-low).

The output of the comparator may be sent to the digital bus DB1 to DB7 or to **SOC.DINSIG1.DIN7** by using **SOC.CFGAIO7.MUX7**.

9.16.4.3 I/O and Interrupts

In this mode, the digital input state and input interrupts are also available. To enable interrupts for low to high transitions on AIO7, set **SOC.SIGINTEN.AIO7REINTEN** to 1b. To enable interrupts for high to low transitions on AIO7, set **SOC.SIGINTEN.AIO7FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO7INT** and cleared by writing **SOC.SIGINTF.AIO7INTF** to 1b.

9.16.5 AIO7 Special Mode

AIO7 Special Mode is typically used for BEMF applications that need to measure the zero-cross threshold of the phase voltage for motor commutation. In special mode, the CAFE can be configured to internally generate a virtual center-tap voltage as a comparator reference for the phase voltages.

Set **SOC.CFGAIO7.MODE7** = 11b to use AIO<9:7> in special mode. In special mode the AIO7 special mode comparator is enabled.

9.16.5.1 Comparator Reference

In special mode, the comparator reference may be selected from AB<3:1>, AIO8, AIO9 or from a programmable comparator threshold voltage (VTHREF). AB1 is used as the virtual center-tap for BEMF zero-cross applications.

Set **SOC.SPECCFG2.SMUXAIO7** to select the comparator reference. To select the VTHREF comparator threshold use **SOC.DOUTSIG0.VTHREF** to select a value from the following:

- 00b: 0.1V
- 01b: 0.2V
- 10b: 0.5V
- 11b: 1.25V

9.16.5.2 Comparator Configuration

The AIO7 comparator has programmable blanking time and hysteresis modes.

The blanking time for the comparator may be configured to use leading edge, trailing edge, leading/trailing edge or no blanking by using **SOC.BLANKING.BLANKMODE**. If **SOC.BLANKING.BLANKMODE** is not 00b (disabled), then the blanking time may be configured to be between 100ns and 6000ns by setting the value in **SOC.BLANKING.BLANKTIME**.

The comparator hysteresis may be configured independently for rising and falling input (asymmetric and bi-directional). To set the comparator hysteresis scale for AIO7, set **SOC.SPECCFG0.HYSMODE** and to set the hysteresis level set **SOC.SPECCFG0.AIO7HYS**.

The output polarity of the comparator may be selected by using **SOC.CFGAIO7.POL7** (0b: active-high; 1b: active-low).

9.16.5.3 I/O and Interrupts

In this mode, the digital input state and input interrupts are also available. To enable interrupts for low to high transitions on AIO7, set **SOC.SIGINTEN.AIO7REINTEN** to 1b. To enable interrupts for high to low transitions on AIO7, set **SOC.SIGINTEN.AIO7FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO7INT** and cleared by writing **SOC.SIGINTF.AIO7INTF** to 1b.

9.16.5.4 Star-Point Connection

Set **SOC.CFGAIO9.MODE9[0]** to 1b in order to connect the motor phase voltages on AIO<9:7> to AB1 with a 100kΩ resistor to create a star-point referent to the comparator.

The AB1 reference may also be configured to come from AIO6 when in amplifier mode. When **SOC.CFGAIO9.MODE9[0]** = 0b, the AB1 reference can be configured to come from the output of the AIO6 amplifier when **SOC.CFGAIO6.MODE6** = 01b (amplifier mode) and **SOC.CFGAIO6.GAIN6** = 000b (direct mode) and **SOC.CFGAIO6.MUX6** = 001b (output to AB1).

To MUX the AIO7 voltage on AB7 with 40% attenuation, set **SOC.CFGAIO9.MODE9[1]** =1b, so the ADC can read out AIO7 voltage from the AFE MUX.

The BEMF position output (POS) can be selected between AIO<9:7> through the MUX at the output of the comparator polarity selector. To select the output of the AIO7 comparator for POS, set **SOC.CFGAIO9.OPT9** to 01b.

The selected POS output can also be connected to the digital MUX. To route the POS output to DB6 on the digital bus, set **SOC.CFGAIO9.MUX9[0]** to 1b.

There is an optional sample and hold circuit available for the POS selected POS signal. To bypass the S/H circuit, set **SOC.CFGAIO8.OPT8[1]** to 0b. To configure the CAFE to use the S/H circuit for the POS signal, set **SOC.CFGAIO8.OPT8[1]** to 1b. In order to start and stop the S/H circuit, the ADC EMUX must be used as described above in the EMUX section.

The IRQ2/POS signal to the MCU can be configured to be the POS signal above, or as the IRQ2 interrupt signal. To configure IRQ2/POS to be the POS position as described above, set **SOC.CFGAIO8.OPT8[0]** to 0b. To configure IRQ/POS to be the IRQ2 signal, set **SOC.CFGAIO8.OPT8[0]** to be 1b.

9.16.6 AIO2/AIO7 Buffer

There is an output buffer that may be used for either AIO2 or AIO7 in the PAC5527 CAFE. To enable this buffer, set **SOC.DOUTSIG1.AIOBUFEN** = 1b.

The input signal for this buffer may be selected by using **SOC.DOUTSIG1.AIOBUFSELIN** with the values below.

Table 9-3 AIO2/AIO7 Buffer Input Select

SOC.DOUTSIG1.AIOBUFSELIN	SIGNAL
00b	ADC VREF (2.5V or 3.0V as selected by **SOC.MISC.VREFSET**).
01b	AB4
10b	AB5
11b	AB6

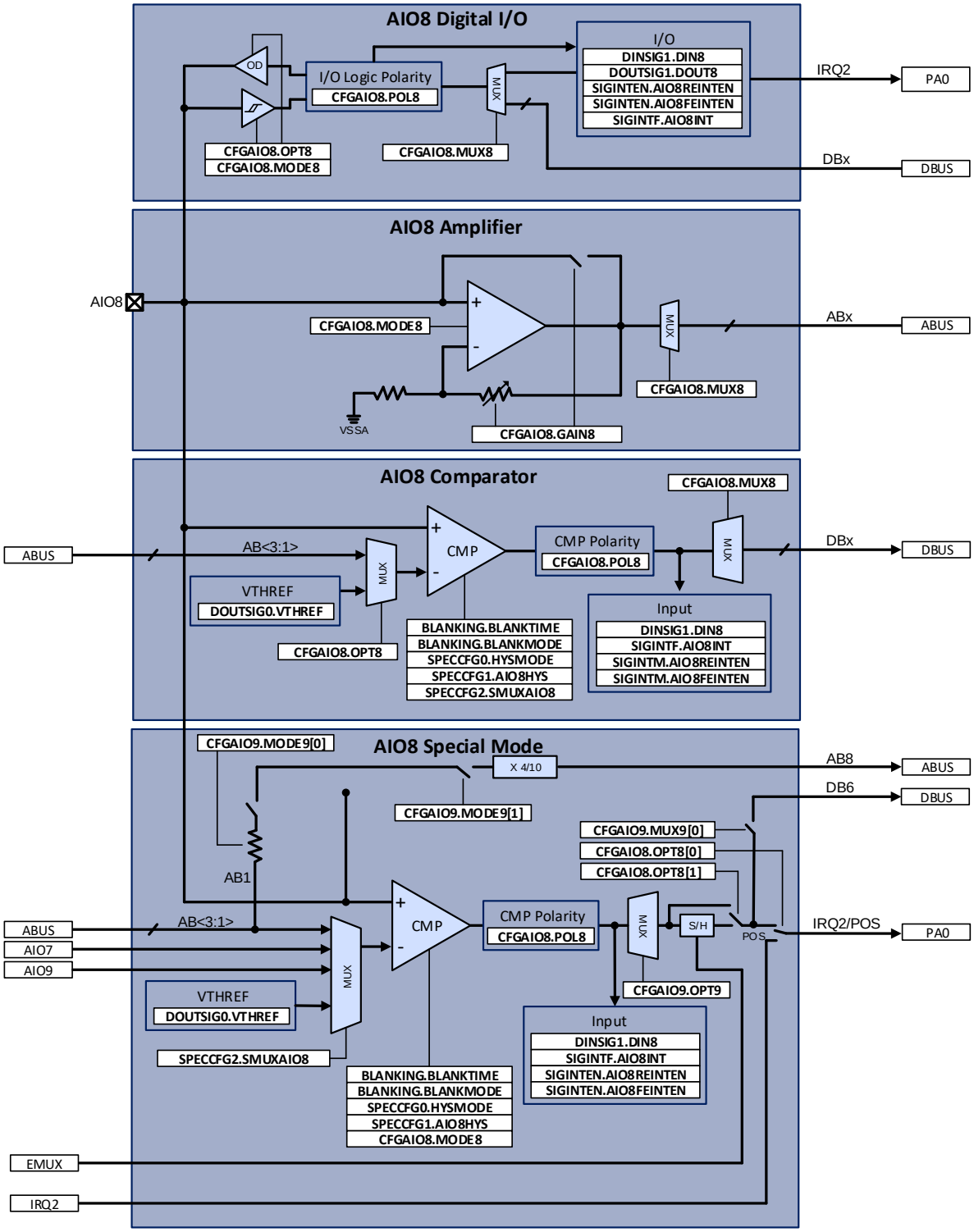
The output of this buffer may be configured to be AIO2 or AIO7. To configure the output of the buffer to be AIO2, set **SOC.DOUTSIG1.AIOBUFSELOUT** to be 0b. To configure the output of the buffer to be AIO7, set **SOC.DOUTSIG1.AIOBUFSELOUT** to be 1b.

9.17 AIO8

AIO8 may be configured as a digital input, single-ended programmable gain amplifier, comparator or a BEMF zero-cross comparator.

9.17.1 System Block Diagram

Figure 9-7 AIO8 System Block Diagram



9.17.2 AIO8 Digital I/O Mode

To configure AIO8 for digital I/O mode, set **SOC.CFGAIO8.MODE8** = 00b.

Set **SOC.CFGAIO8.OPT8** = 10b to use AIO8 as an open-drain output. Set **SOC.CFGAIO8.MUX8** = 000b to mux the output state from **SOC.DOUTSIG1.DOUT8**. Use **SOC.CFGAIO8.MUX8** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

Set **SOC.CFGAIO8.OPT8** = 00b to use AIO8 as a digital input. The state can be read from **SOC.DINSIG1.DIN8**.

To configure the input or output polarity of AIO8, use **SOC.CFGAIO8.POL8** to set logic polarity of the signal between AIO8 input/output and MUX8.

To enable interrupts for low to high transitions on AIO8, set **SOC.SIGINTEN.AIO8REINTEN** to 1b. To enable interrupts for high to low transitions on AIO8, set **SOC. SIGINTEN.AIO8FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO8INT** and cleared by writing **SOC.SIGINTF.AIO8INTF** to 1b.

9.17.3 AIO8 Amplifier Mode

To configure AIO8 for amplifier mode set **SOC.CFGAIO8.MODE8** = 01b. In amplifier mode, the AIO8 gain amplifier is enabled.

Use **SOC.CFGAIO8.GAIN8** to set the amplifier gain from 1x to 48x or to bypass mode. Use **SOC.CFGAIO8.MUX8** to switch the output of the amplifier to analog channel AB1 to AB7 on the analog bus ABUS.

9.17.4 AIO8 Comparator Mode

Set **SOC.CFGAIO8.MODE8** = 10b to use AIO8 in comparator mode. In comparator mode, the AIO8 general-purpose comparator is enabled.

9.17.4.1 Comparator Reference

The comparator reference may be selected from AB<3:1> or from a programmable comparator threshold voltage (VTHREF). Set **SOC.CFGAIO8.OPT8** to select the comparator reference. To select the VTHREF comparator threshold use **SOC.DOUTSIG0.VTHREF** to select a value from the following:

- 00b: 0.1V
- 01b: 0.2V
- 10b: 0.5V
- 11b: 1.25V

9.17.4.2 Comparator Configuration

The AIO8 comparator has programmable blanking time and hysteresis modes.

The blanking time for the comparator may be configured to use leading edge, trailing edge, leading/trailing edge or no blanking by using **SOC.BLANKING.BLANKMODE**. If **SOC.BLANKING.BLANKMODE** is not 00b (disabled), then the blanking time may be configured to be between 100ns and 6000ns by setting the value in **SOC.BLANKING.BLANKTIME**.

The comparator hysteresis may be configured independently for rising and falling input (asymmetric and bi-directional). To set the comparator hysteresis scale for AIO8, set **SOC.SPECCFG0.HYSMODE** and to set the hysteresis level set **SOC.SPECCFG1.AIO8HYS**.

The output polarity of the comparator may be selected by using **SOC.CFGAIO8.POL8** (0b: active-high; 1b: active-low).

The output of the comparator may be sent to the digital bus DB1 to DB7 or to **SOC.DINSIG1.DIN8** by using **SOC.CFGAIO8.MUX8**.

9.17.4.3 I/O and Interrupts

In this mode, the digital input state and input interrupts are also available. To enable interrupts for low to high transitions on AIO8, set **SOC.SIGINTEN.AIO8REINTEN** to 1b. To enable interrupts for high to low transitions on AIO8, set **SOC.SIGINTEN.AIO8FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO8INT** and cleared by writing **SOC.SIGINTF.AIO8INTF** to 1b.

9.17.5 AIO8 Special Mode

AIO8 Special Mode is typically used for BEMF applications that need to measure the zero-cross threshold of the phase voltage for motor commutation. In special mode, the CAFE can be configured to internally generate a virtual center-tap voltage as a comparator reference for the phase voltages.

Set **SOC.CFGAIO7.MODE7** = 11b to use AIO<9:7> in special mode. In special mode the AIO8 special mode comparator is enabled.

9.17.5.1 Comparator Reference

In special mode, the comparator reference may be selected from AB<3:1>, AIO7, AIO9 or from a programmable comparator threshold voltage (VTHREF). AB1 is used as the virtual center-tap for BEMF zero-cross applications.

Set **SOC.SPECCFG2.SMUXAIO8** to select the comparator reference. To select the VTHREF comparator threshold use **SOC.DOUTSIG0.VTHREF** to select a value from the following:

- 00b: 0.1V
- 01b: 0.2V
- 10b: 0.5V
- 11b: 1.25V

9.17.5.2 Comparator Configuration

The AIO8 comparator has programmable blanking time and hysteresis modes.

The blanking time for the comparator may be configured to use leading edge, trailing edge, leading/trailing edge or no blanking by using **SOC.BLANKING.BLANKMODE**. If **SOC.BLANKING.BLANKMODE** is not 00b (disabled), then the blanking time may be configured to be between 100ns and 6000ns by setting the value in **SOC.BLANKING.BLANKTIME**.

The comparator hysteresis may be configured independently for rising and falling input (asymmetric and bi-directional). To set the comparator hysteresis scale for AIO8, set **SOC.SPECCFG0.HYSMODE** and to set the hysteresis level set **SOC.SPECCFG1.AIO8HYS**.

The output polarity of the comparator may be selected by using **SOC.CFGAIO8.POL8** (0b: active-high; 1b: active-low).

9.17.5.3 I/O and Interrupts

In this mode, the digital input state and input interrupts are also available. To enable interrupts for low to high transitions on AIO8, set **SOC.SIGINTEN.AIO8REINTEN** to 1b. To enable interrupts for high to low transitions on AIO8, set **SOC.SIGINTEN.AIO8FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO8INT** and cleared by writing **SOC.SIGINTF.AIO8INTF** to 1b.

9.17.5.4 Star-Point Connection

Set **SOC.CFGAIO9.MODE9[0]** to 1b in order to connect the motor phase voltages on AIO<9:7> to AB1 with a 100kΩ resistor to create a star-point referent to the comparator.

The AB1 reference may also be configured to come from AIO6 when in amplifier mode. When **SOC.CFGAIO9.MODE9[0]** = 0b, the AB1 reference can be configured to come from the output of the AIO6 amplifier when **SOC.CFGAIO6.MODE6** = 01b (amplifier mode) and **SOC.CFGAIO6.GAIN6** = 000b (direct mode) and **SOC.CFGAIO6.MUX6** = 001b (output to AB1).

To MUX the AIO8 voltage on AB8 with 40% attenuation, set **SOC.CFGAIO9.MODE9[1]** =1b, so the ADC can read out AIO8 voltage from the AFE MUX.

The BEMF position (POS) can be selected between AIO<9:7> through the MUX at the output of the comparator polarity selector. To select the output of the AIO8 comparator for POS, set **SOC.CFGAIO9.OPT9** to 01b.

The selected POS output can also be connected to the digital MUX. To route the POS output to DB6 on the digital bus, set **SOC.CFGAIO9.MUX9[0]** to 1b.

There is an optional sample and hold circuit available for the POS selected POS signal. To bypass the S/H circuit, set **SOC.CFGAIO8.OPT8[1]** to 0b. To configure the CAFE to use the S/H circuit for the POS signal, set **SOC.CFGAIO8.OPT8[1]** to 1b. In order to start and stop the S/H circuit, the ADC EMUX must be used as described above in the EMUX section.

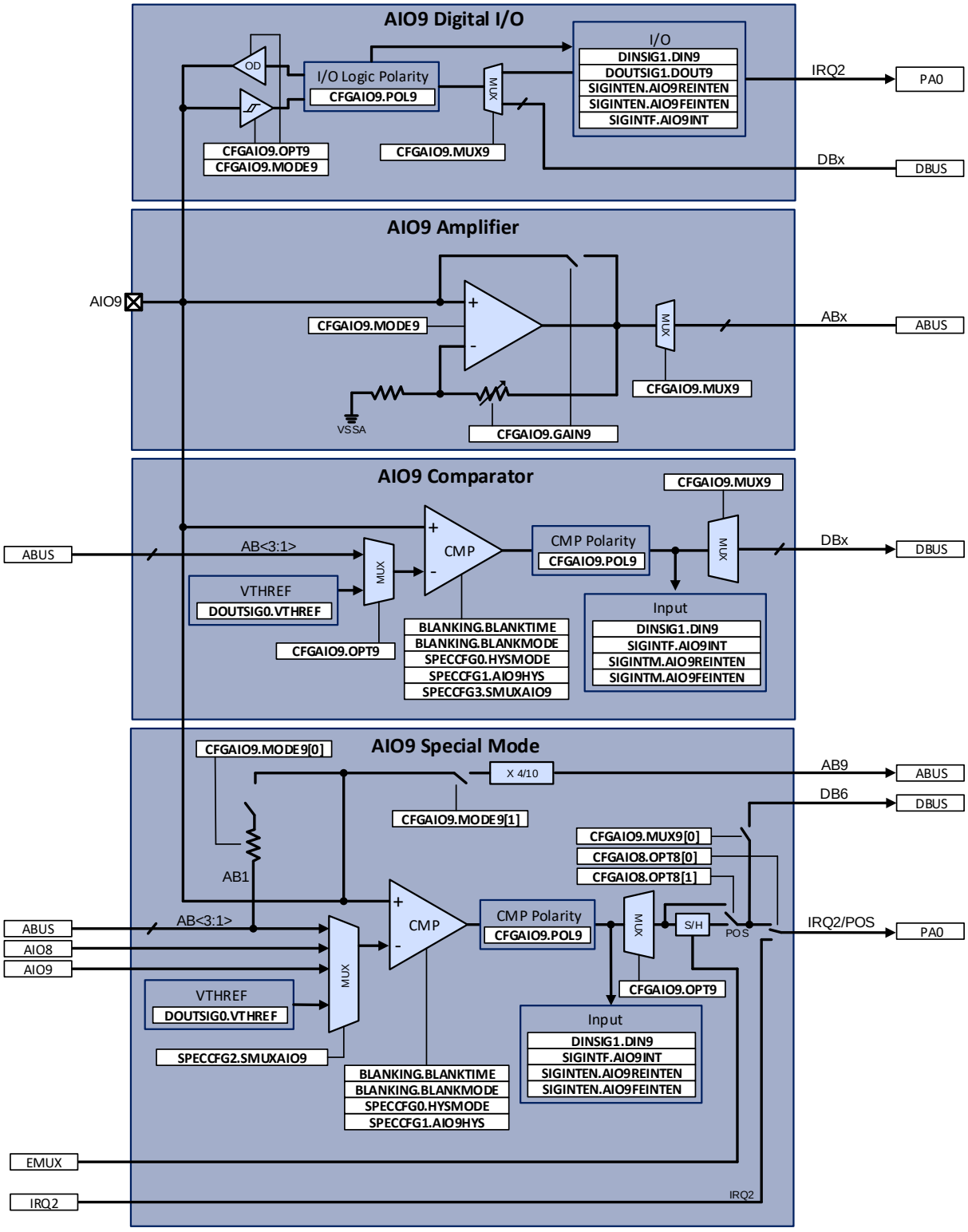
The IRQ2/POS signal to the MCU can be configured to be the POS signal above, or as the IRQ2 interrupt signal. To configure IRQ2/POS to be the POS position as described above, set **SOC.CFGAIO8.OPT8[0]** to 0b. To configure IRQ/POS to be the IRQ2 signal, set **SOC.CFGAIO8.OPT8[0]** to be 1b.

9.18 AIO9

AIO9 may be configured as a digital input, single-ended programmable gain amplifier, comparator or a BEMF zero-cross comparator.

9.18.1 System Block Diagram

Figure 9-8 AIO9 System Block Diagram



9.18.2 AIO9 Digital I/O Mode

To configure AIO9 for digital I/O mode, set **SOC.CFGAIO9.MODE9** = 00b.

Set **SOC.CFGAIO9.OPT9** = 10b to use AIO9 as an open-drain output. Set **SOC.CFGAIO9.MUX9** = 000b to mux the output state from **SOC.DOUTSIG1.DOUT9**. Use **SOC.CFGAIO9.MUX9** to mux the output signal from the internal digital bus DBUS DB1 to DB7.

Set **SOC.CFGAIO9.OPT9** = 00b to use AIO9 as a digital input. The state can be read from **SOC.DINSIG1.DIN9**.

To configure the input or output polarity of AIO9, use **SOC.CFGAIO9.POL9** to set logic polarity of the signal between AIO9 input/output and MUX9.

To enable interrupts for low to high transitions on AIO9, set **SOC.SIGINTEN.AIO9REINTEN** to 1b. To enable interrupts for high to low transitions on AIO9, set **SOC. SIGINTEN.AIO9FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO9INT** and cleared by writing **SOC.SIGINTF.AIO9INTF** to 1b.

9.18.3 AIO9 Amplifier Mode

To configure AIO9 for amplifier mode set **SOC.CFGAIO9.MODE9** = 01b. In amplifier mode, the AIO9 gain amplifier is enabled.

Use **SOC.CFGAIO9.GAIN9** to set the amplifier gain from 1x to 48x or to bypass mode. Use **SOC.CFGAIO9.MUX9** to switch the output of the amplifier to analog channel AB1 to AB7 on the analog bus ABUS.

9.18.4 AIO9 Comparator Mode

Set **SOC.CFGAIO9.MODE9** = 10b to use AIO9 in comparator mode. In comparator mode, the AIO9 general-purpose comparator is enabled.

9.18.4.1 Comparator Reference

The comparator reference may be selected from AB<3:1> or from a programmable comparator threshold voltage (VTHREF). Set **SOC.CFGAIO9.OPT9** to select the comparator reference. To select the VTHREF comparator threshold use **SOC.DOUTSIG0.VTHREF** to select a value from the following:

- 00b: 0.1V
- 01b: 0.2V
- 10b: 0.5V
- 11b: 1.25V

9.18.4.2 Comparator Configuration

The AIO9 comparator has programmable blanking time and hysteresis modes.

The blanking time for the comparator may be configured to use leading edge, trailing edge, leading/trailing edge or no blanking by using **SOC.BLANKING.BLANKMODE**. If **SOC.BLANKING.BLANKMODE** is not 00b (disabled), then the blanking time may be configured to be between 100ns and 6000ns by setting the value in **SOC.BLANKING.BLANKTIME**.

The comparator hysteresis may be configured independently for rising and falling input (asymmetric and bi-directional). To set the comparator hysteresis scale for AIO9, set **SOC.SPECCFG0.HYSMODE** and to set the hysteresis level set **SOC.SPECCFG1.AIO9HYS**.

The output polarity of the comparator may be selected by using **SOC.CFGAIO9.POL9** (0b: active-high; 1b: active-low).

The output of the comparator may be sent to the digital bus DB1 to DB7 or to **SOC.DINSIG1.DIN9** by using **SOC.CFGAIO9.MUX9**.

9.18.4.3 I/O and Interrupts

In this mode, the digital input state and input interrupts are also available. To enable interrupts for low to high transitions on AIO9, set **SOC.SIGINTEN.AIO9REINTEN** to 1b. To enable interrupts for high to low transitions on AIO9, set **SOC.SIGINTEN.AIO9FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO9INT** and cleared by writing **SOC.SIGINTF.AIO9INTF** to 1b.

9.18.5 AIO9 Special Mode

AIO9 Special Mode is typically used for BEMF applications that need to measure the zero-cross threshold of the phase voltage for motor commutation. In special mode, the CAFE can be configured to internally generate a virtual center-tap voltage as a comparator reference for the phase voltages.

Set **SOC.CFGAIO7.MODE7** = 11b to use AIO<9:7> in special mode. In special mode the AIO9 special mode comparator is enabled.

9.18.5.1 Comparator Reference

In special mode, the comparator reference may be selected from AB<3:1>, AIO8, AIO9 or from a programmable comparator threshold voltage (VTHREF). AB1 is used as the virtual center-tap for BEMF zero-cross applications.

Set **SOC.SPECCFG3.SMUXAIO9** to select the comparator reference. To select the VTHREF comparator threshold use **SOC.DOUTSIG0.VTHREF** to select a value from the following:

- 00b: 0.1V
- 01b: 0.2V
- 10b: 0.5V
- 11b: 1.25V

9.18.5.2 Comparator Configuration

The AIO9 comparator has programmable blanking time and hysteresis modes.

The blanking time for the comparator may be configured to use leading edge, trailing edge, leading/trailing edge or no blanking by using **SOC.BLANKING.BLANKMODE**. If **SOC.BLANKING.BLANKMODE** is not 00b (disabled), then the blanking time may be configured to be between 100ns and 6000ns by setting the value in **SOC.BLANKING.BLANKTIME**.

The comparator hysteresis may be configured independently for rising and falling input (asymmetric and bi-directional). To set the comparator hysteresis scale for AIO9, set **SOC.SPECCFG0.HYSMODE** and to set the hysteresis level set **SOC.SPECCFG1.AIO9HYS**.

The output polarity of the comparator may be selected by using **SOC.CFGAIO9.POL9** (0b: active-high; 1b: active-low).

9.18.5.3 I/O and Interrupts

In this mode, the digital input state and input interrupts are also available. To enable interrupts for low to high transitions on AIO9, set **SOC.SIGINTEN.AIO9REINTEN** to 1b. To enable interrupts for high to low transitions on AIO9, set **SOC.SIGINTEN.AIO9FEINTEN** to 1b. When the edge is detected, an interrupt will be asserted on IRQ2 to the MCU. The interrupt status can be monitored by reading **SOC.SIGINTF.AIO9INT** and cleared by writing **SOC.SIGINTF.AIO9INTF** to 1b.

9.18.5.4 Star-Point Connection

Set **SOC.CFGAIO9.MODE9[0]** to 1b in order to connect the motor phase voltages on AIO<9:7> to AB1 with a 100kΩ resistor to create a star-point referent to the comparator.

The AB1 reference may also be configured to come from AIO6 when in amplifier mode. When **SOC.CFGAIO9.MODE9[0]** = 0b, the AB1 reference can be configured to come from the output of the AIO6 amplifier when **SOC.CFGAIO6.MODE6** = 01b (amplifier mode) and **SOC.CFGAIO6.GAIN6** = 000b (direct mode) and **SOC.CFGAIO6.MUX6** = 001b (output to AB1).

To MUX the AIO9 voltage on AB9 with 40% attenuation, set **SOC.CFGAIO9.MODE9[1]** =1b, so the ADC can read out AIO9 voltage from the AFE MUX.

The BEMF position (POS) can be selected between AIO<9:7> through the MUX at the output of the comparator polarity selector. To select the output of the AIO9 comparator for POS, set **SOC.CFGAIO9.OPT9** to 01b.

The selected POS output can also be connected to the digital MUX. To route the POS output to DB6 on the digital bus, set **SOC.CFGAIO9.MUX9[0]** to 1b.

There is an optional sample and hold circuit available for the POS selected POS signal. To bypass the S/H circuit, set **SOC.CFGAIO8.OPT8[1]** to 0b. To configure the CAFE to use the S/H circuit for the POS signal, set **SOC.CFGAIO8.OPT8[1]** to 1b. In order to start and stop the S/H circuit, the ADC EMUX must be used as described above in the EMUX section.

The IRQ2/POS signal to the MCU can be configured to be the POS signal above, or as the IRQ2 interrupt signal. To configure IRQ2/POS to be the POS position as described above, set **SOC.CFGAIO8.OPT8[0]** to 0b. To configure IRQ/POS to be the IRQ2 signal, set **SOC.CFGAIO8.OPT8[0]** to be 1b.

9.19 Register Summary

Table 9-4 CAFE Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
0x06	**SOC.CFGAIO0**	AIO0 Configuration	0x00
0x07	**SOC.CFGAIO1**	AIO1 Configuration	0x00
0x08	**SOC.CFGAIO2**	AIO2 Configuration	0x00
0x09	**SOC.CFGAIO3**	AIO3 Configuration	0x00
0x0A	**SOC.CFGAIO4**	AIO4 Configuration	0x00
0x0B	**SOC.CFGAIO5**	AIO5 Configuration	0x00
0x0C	**SOC.CFGAIO6**	AIO6 Configuration	0x00
0x0D	**SOC.CFGAIO7**	AIO7 Configuration	0x00
0x0E	**SOC.CFGAIO8**	AIO8 Configuration	0x00
0x0F	**SOC.CFGAIO9**	AIO9 Configuration	0x00
0x10	**SOC.SIGSET**	Signal manager Configuration	0x00
0x11	**SOC.HPDACH**	High Protection Threshold	0x00
0x12	**SOC.HPDACL**	High Protection Threshold	0x00
0x13	**SOC.LPDACH**	Low Protection Threshold	0x00
0x14	**SOC.LPDACL**	Low Protection Threshold	0x00
0x15	**SOC.SHCFG1**	Sample and Hold Configuration 1	0x00
0x16	**SOC.SHCFG2**	Sample and Hold Configuration 2	0x00
0x17	**SOC.PROTINTEN**	Driver Protection Interrupt Enable	0x00
0x18	**SOC.PROTSTAT**	Driver Protection Interrupt Status	0x00
0x19	**SOC.DOUTSIG0**	AIO Data Output 0	0x00
0x1A	**SOC.DOUTSIG1**	AIO Data Output 1	0x00
0x1B	**SOC.DINSIG0**	AIO Data Input 0	0x00
0x1C	**SOC.DINSIG1**	AIO Data Input 1	0x00
0x1D	**SOC.CFGIO1**	AIO10-AIO13 Configuration 0	0x00
0x1F	**SOC.SIGINTEN**	AIO Interrupt Enable	0x00

0x20	**SOC.SIGINTF**	AIO Interrupt Flag Status	0x00
0x21	**SOC.BLANKING**	BEMF Comparator Blanking Configuration	0x00
0x22	**SOC.SPECCFG0**	AIO7 Hysteresis Configuration	0x00
0x23	**SOC.SPECCFG1**	AIO8/AIO9 Hysteresis Configuration	0x00
0x24	**SOC.SPECCFG2**	AIO7/AIO8 Comparator Input MUX Configuration	0x00
0x25	**SOC.SPECCFG3**	AIO9 Comparator Input MUX Configuration	0x00
0x26	**SOC.GP0**	General-purpose register space	0x00

9.20 Register Detail

9.20.1 SOC.CFGAIO0

Register 9-1 SOC.CFGAIO0 (AIO0 Configuration, 06h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE10**	RW	00b	00b	01b
5:4	**OPT0**	RW	00b	**OPT0**: AIO0 Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN10:** Differential amplifier gain setting: 000b: 1x 010b: 1x 011b: 2x 001b: 4x 100b: 8x 101b: 16x 110b: 16x 111b: 16x
3	**POL0**	RW	0b	**POL0**: AIO0 Polarity If **CFGAIO0.OPT0** = 00b, AIO0 input polarity setting. If **CFGAIO0.OPT0** = 10b, AIO0 output polarity setting: 0b: active high 1b: active low	
2	**MUX0**	RW	0b	**MUX0**: AIO0 Digital MUX setting: 000b: DATAIO0 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 0b
1:0		RW	00b		**LP10EN:** LP10 Comparator option: 00b: Disabled 01b: Enabled with 1µs blanking time 10b: Enabled with 2µs blanking time 11b: Enabled with 4µs blanking time

9.20.2 SOC.CFGAIO1

Register 9-2 SOC.CFGAIO1 (AIO1 Configuration, 07h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	R	00b	Reserved	Reserved
5:4	**OPT1**	RW	0b	**OPT1**: AIO1 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**HP10PREN:** HPROT10 PR Protection enable: 0b: HP10 output to PR disabled 1b: HP10 output to PR enabled
		RW	0b		**LP10PREN:** LPROT10 PR Protection enable: 0b: LP10 output to PR disabled 1b: LP10 output to PR enabled
3	**POL1**	RW	0b	If **CFGAIO1.OPT1** = 00b, AIO1 input polarity setting. If **CFGAIO1.OPT1** = 10b, AIO1 output polarity setting: 0b: active high 1b: active low	**OS10EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX1**	RW	0b	**MUX1**: AIO1 Digital MUX: 000b: DATAIO1 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL10EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP10EN:** HP10 Comparator setting: 00b: Disabled 01b: Enabled with 1µs blanking time 10b: Enabled with 2µs blanking time 11b: Enabled with 4µs blanking time

9.20.3 SOC.CFGAIO2

Register 9-3 SOC.CFGAIO2 (AIO2 Configuration, 08h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE32**	RW	00b	00b	01b
5:4	**OPT2**	RW	0b	**OPT2**: AIO2 Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN32:** Differential amplifier gain setting: 000b: 1x 010b: 1x 011b: 2x 001b: 4x 100b: 8x 101b: 16x 110b: 16x 111b: 16x
3	**POL2**	RW	0b	If **CFGAIO2.OPT2** = 00b, AIO2 input polarity setting. If **CFGAIO2.OPT2** = 10b, AIO2 output polarity setting: 0b: active high 1b: active low	
2	**MUX2**	RW	0b	**MUX2**: AIO0 Digital MUX setting: 000b: DATAIO2 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 0b
1:0		RW	0b		**LP32EN:** LP32 Comparator setting: 00b: Disabled 01b: Enabled with 1µs blanking time 10b: Enabled with 2µs blanking time 11b: Enabled with 4µs blanking time

9.20.4 SOC.CFGAIO3

Register 9-4 SOC.CFGAIO3 (AIO3 Configuration, 09h)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	RW	0b	Reserved	Reserved
5	**OPT3**	RW	0b	**OPT3**: AIO3 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**HP32PREN:** HPROT32 PR Protection enable: 0b: HP32 output to PR disabled 1b: HP32 output to PR enabled
4		RW	0b		**LP32PREN:** LPROT32 PR Protection enable: 0b: LP32 output to PR disabled 1b: LP32 output to PR enabled
3	**POL3**	RW	0b	If **CFGAIO3.OPT3** = 00b, AIO3 input polarity setting If **CFGAIO3.OPT3** = 10b, AIO3 output polarity setting: 0b: active high 1b: active low	**OS32EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX3**	RW	0b	**MUX3**: AIO3 Digital MUX: 000b: DATAIO3 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL32EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP32EN:** HP32 Comparator setting: 00b: Disabled 01b: Enabled with 1µs blanking time 10b: Enabled with 2µs blanking time 11b: Enabled with 4µs blanking time

9.20.5 SOC.CFGAIO4

Register 9-5 SOC.CFGAIO4 (AIO4 Configuration, 0Ah)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**MODE54**	RW	00b	00b	01b
5:4	**OPT4**	RW	0b	**OPT4**: AIO4 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN54:** Differential amplifier gain setting: 000b: 1x 010b: 1x 011b: 2x 001b: 4x 100b: 8x 101b: 16x 110b: 16x 111b: 16x
3	**POL4**	RW	0b	If **CFGAIO4.OPT4** = 00b, AIO4 input polarity setting. If **CFGAIO4.OPT4** = 10b, AIO4 output polarity setting: 0b: active high 1b: active low	
2	**MUX4**	RW	0b	**MUX4**: AIO4 Digital MUX: 000b: DATAIO4 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 0b
		RW	00b		**LP54EN:** LP54 Comparator setting: 00b: Disabled 01b: Enabled with 1µs blanking time 10b: Enabled with 2µs blanking time 11b: Enabled with 4µs blanking time

9.20.6 SOC.CFGAIO5

Register 9-6 SOC.CFGAIO5 (AIO5 Configuration, 0Bh)

BIT	NAME	ACCESS	RESET	IO MODE	DIFFAMP MODE
7:6	**RFU**	RW	0b	Reserved	Reserved
5	**OPT5**	RW	0b	**OPT5**: AIO5 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**HP54PREN:** HPROT54 PR Protection enable: 0b: HP54 output to PR disabled 1b: HP54 output to PR enabled
4		RW	0b		**LP54PREN:** LPROT54 PR Protection enable: 0b: LP54 output to PR disabled 1b: LP54 output to PR enabled
3	**POL5**	RW	0b	If **CFGAIO5.OPT5** = 00b, AIO5 input polarity setting. If **CFGAIO5.OPT5** = 10b, AIO5 output polarity setting: 0b: active high 1b: active low	**OS54EN:** Differential Amplifier Offset: 0b: Offset disabled 1b: Offset enabled, input signal shifted by $V_{REF}/2$
2	**MUX5**	RW	0b	**MUX5**: AIO5 Digital MUX: 000b: DATAIO5 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**CAL54EN:** Differential Amplifier Offset Calibration: 0b: disabled 1b: enabled
1:0		RW	00b		**HP54EN:** HP54 Comparator setting: 00b: Disabled 01b: Enabled with 1µs blanking time 10b: Enabled with 2µs blanking time 11b: Enabled with 4µs blanking time

9.20.7 SOC.CFGAIO6

Register 9-7 SOC.CFGAIO6 (AIO6 Configuration, 0Ch)

BIT	IO MODE	AMPLIFIER MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE6:** 00b	**MODE6:** 01b	**MODE6:** 10b	**MODE6:** 11b
5	**OPT6:** AIO6 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN6:** AIO6 Amplifier gain setting: 000b: Gain amplifier bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT6:** AIO6 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**ADMUX:** 1b: Switch ADCIN to AB7
4				**SWAP:** Buffer Swap: 0b: Do not swap buffer offset 1b: Swap buffer offset
3	**POL6:** AIO6 Polarity Setting: 00b: active-high 01b: active-low		**POL6:** AIO6 Comparator output polarity setting: 0b: active-high 1b: active-low	Reserved, write as 0b
2:0	**MUX6:** AIO6 Digital MUX Setting: 000b: DATAIO6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX6:** Analog MUX Setting: 000b: AB6 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX6:** AIO6 Digital MUX Setting: 000b: DATAIO6 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX6:** Analog MUX Setting: 000b: AB6 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7

9.20.8 SOC.CFGAIO7

Register 9-8 SOC.CFGAIO7 (AIO7 Configuration, 0Dh)

BIT	IO MODE	AMPLIFIER MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE7:** 00b	**MODE7:** 01b	**MODE7:** 10b	**MODE7:** 11b
5	**OPT7:** AIO7 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN7:** AIO7 Amplifier gain setting: 000b: Bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT7:** AIO7 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	Reserved, write as 0b
4				Reserved, write as 0b
3	**POL7**: AIO7 Polarity Setting: 00b: active-high 01b: active-low		**POL7:** AIO7 Comparator polarity setting: 0b: active-high 1b: active-low	**POL7:** AIO7 Comparator polarity setting: 0b: active-high 1b: active-low
2:0	**MUX7:** AIO7 Digital MUX: 000b: DATAIO7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX7:** AIO7 Analog MUX Setting: 000b: AB7 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX7:** AIO7 Digital MUX: 000b: DATAIO7 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 000b

9.20.9 SOC.CFGAIO8

Register 9-9 SOC.CFGAIO8 (AIO8 Configuration, 0Eh)

BIT	IO MODE	AMPLIFIER MODE	COMPARATOR MODE	SPECIAL MODE
7:6	**MODE8:** 00b	**MODE8:** 01b	**MODE8:** 10b	Reserved, write as 00b.
5	**OPT8:** AIO8 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN8** Amplifier gain setting: 000b: Bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT8:** AIO8 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**OPT8[1]:** S/H bypass for POS: 0b: Bypass S/H for POS signal 1b: Do not bypass S/H for POS signal
4				**OPT8[0]:** IRQ2/POS output: 0b: Select IRQ2/POS output POS (BEMF) 1b: Select IRQ2/POS output IRQ2 (INT)
3	**POL8:** AIO8 Polarity Setting: 00b: active-high 01b: active-low		**POL8:** AIO8 Comparator polarity setting: 0b: active-high 1b: active-low	**POL8:** AIO8 Comparator polarity setting: 0b: active-high 1b: active-low
2:0	**MUX8:** AIO8 Digital MUX: 000b: DATAIO8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX8:** AIO8 Analog MUX: 000b: AB8 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX8:** AIO8 Digital MUX: 000b: DATAIO8 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write as 000b.

9.20.10 SOC.CFGAIO9

Register 9-10 SOC.CFGAIO9 (AIO9 Configuration, 0Fh)

BIT	IO MODE	AMPLIFIER MODE	COMPARATOR MODE	SPECIAL MODE
7	**MODE9:** 00b	**MODE9:** 01b	**MODE9:** 10b	**MODE9[1]:** Switch (4/10) * AIO7/8/9 to AB7/8/9.
6				**MODE9[0]:** Switch AIO7/8/9 to CT resistors to generate CT at AB1.
5	**OPT9:** AIO9 IO Option: 00b: Input 01b: Hi-Z 10b: Open-drain output 11b: Hi-Z	**GAIN9:** AIO9 Amplifier gain setting: 000b: Bypass, direct mode 001b: 1x 010b: 2x 011b: 4x 100b: 8x 101b: 16x 110b: 32x 111b: 48x	**OPT9:** AIO9 Comparator Reference select: 00b: VTHREF 01b: AB1 10b: AB2 11b: AB3	**OPT9:** AIO789 comparator output to POS: 00b: not connected 01b: MUX AIO7 comparator output to POS 10b: MUX AIO8 comparator output to POS 11b: MUX AIO9 comparator output to POS
4				
3	**POL9:** AIO9 Polarity Setting: 00b: active-high 01b: active-low		**POL9:** AIO9 Comparator polarity setting: 0b: active-high 1b: active-low	**POL9:** AIO9 Comparator polarity setting: 0b: active-high 1b: active-low
2:1	**MUX9:** AIO9 Digital MUX: 000b: DATAIO9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	**MUX9**: AIO9 Analog MUX Setting: 000b: AB9 001b: AB1 010b: AB2 011b: AB3 100b: AB4 101b: AB5 110b: AB6 111b: AB7	**MUX9:** AIO9 Digital MUX: 000b: DATAIO9 001b: DB1 010b: DB2 011b: DB3 100b: DB4 101b: DB5 110b: DB6 111b: DB7	Reserved, write to 00b.
0				**MUX9[0]**: Switch POS after MUX to DB6.

9.20.11 SOC.SIGSET

Register 9-11 SOC.SIGSET (Signal Manager Configuration, 10h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**RFU**	R	0b	Reserved, write to 000b
3	**HPROTHYS**	R/W	0b	HPx Hysteresis: 0b: Comparator Hysteresis disabled 1b: Comparator Hysteresis enabled
2	**LPROTHYS**	R/W	0b	LPx Hysteresis: 0b: Comparator Hysteresis disabled 1b: Comparator Hysteresis enabled
1	**LPDACAB3**	R/W	0b	Connect LPDAC output to AB3: 0b: LPDAC output not connected to AB3 1b: LPDAC output connected to AB3
0	**HPDACAB2**	R/W	0b	Connect HPDAC output to AB2: 0b: HPDAC output not connected to AB2 1b: HPDAC output connected to AB2

9.20.12 SOC.HPDACH

Register 9-12 SOC.HPDACH (HPDAC High Setting, 11h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**HPDAC[9:2]**	R/W	0	HPDAC MSB setting bits 9:2

9.20.13 SOC.HPDACL

Register 9-13 SOC.HPDACL (HPDAC Low Setting, 12h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**RFU**	R	0	Reserved, write to 0
1:0	**HPDAC[1:0]**	R/W	0	HPDAC MSB setting bits 1:0

9.20.14 SOC.LPDACH

Register 9-14 SOC.LPDACH (LPDAC High Setting, 13h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**LPDAC[9:2]**	R/W	0	LPDAC MSB setting bits 9:2

9.20.15 SOC.LPDACL

Register 9-15 SOC.LPDAC1 (LPDAC Low Setting, 14h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**Reserved**	R	0b	Reserved, write to 0.
1:0	**LPDAC[1:0]**	R/W	0b	LPDAC Setting bits 1:0

9.20.16 SOC.SHCFG1

Register 9-16 SOC.SHCFG1 (Sample and Hold Configuration, 15h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	000b	Reserved, write to 0
4	**EMUXEN**	R/W	0b	EMUX Enable. Note that writing 0b to this field will reset the EMUX state machine: 0b: disabled 1b: enabled
3	**ADCBUFEN**	R/W	0b	ADCBUF Circuit Enable: 0b: disabled 1b: enabled
2	**DAO54SH**	R/W	0b	DAO54 Sample and Hold output sync to AFE ADC MUX: 0b: Bypass S/H 1b: enable S/H
1	**DAO32SH**	R/W	0b	DAO32 Sample and Hold output sync to AFE ADC MUX: 0b: Bypass S/H 1b: enable S/H
0	**DAO10SH**	R/W	0b	DAO10 Sample and Hold output sync to AFE ADC MUX: 0b: Bypass S/H 1b: enable S/H

9.20.17 SOC.SHCFG2

Register 9-17 SOC.SHCFG2 (Sample and Hold Configuration 2, 16h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**COMP_SH**	R/W	0b	Comparator Toggle: 0b: Sample POS value 1b: Hold POS value
6	**HLD2**	R/W	0b	DAO54 Sample and Hold Output: 0b: Sample 1b: Hold
5	**HLD1**	R/W	0b	DAO32 Sample and Hold Output: 0b: Sample 1b: Hold
4	**HLD0**	R/W	0b	DAO10 Sample and Hold Output: 0b: Sample 1b: Hold
3:0	**MUXA**	R/W	0b	ADC Mux Channel Selector when **SHCFG1.EMUX_E**N is 0b: 0000b: DAO10 0001b: DAO32 0010b: DAO54 0011b: AB1 0100b: AB2 0101b: AB3 0110b: AB4 0111b: AB5 1000b: AB6 1001b: AB7 1010b: AB8 1011b: AB9 1100b: AB10 (VPTAT) 1101b: AB11 (PWRMON) 1110b: AB12 (VP / 10) 1111b: AB13 (VM / 20)

9.20.18 SOC.PROTINTEN

Register 9-18 SOC.PROTINTEN (Protection Interrupt Enable, 17h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6	**HP54INTEN**	R/W	0b	HPROT54 Interrupt enable: 0b: disabled 1b: enabled
5	**HP32INTEN**	R/W	0b	HPROT32 Interrupt enable: 0b: disabled 1b: enabled
4	**HP10INTEN**	R/W	0b	HPROT10 Interrupt enable: 0b: disabled 1b: enabled
3	**RFU**	R	0b	Reserved, write to 0.
2	**LP54INTEN**	R/W	0b	LPROT54 Interrupt enable: 0b: disabled 1b: enabled
1	**LP32INTEN**	R/W	0b	LPROT32 Interrupt enable: 0b: disabled 1b: enabled
0	**LP10INTEN**	R/W	0b	LPROT10 Interrupt enable: 0b: disabled 1b: enabled

9.20.19 SOC.PROTSTAT

Register 9-19 SOC.PROTSTAT (Protection Interrupt Status, 18h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HP54STAT**	R	0b	HPROT54 Real-time status: 0b: Comparator output low 1b: Comparator output high
6	**HP54INT**	R/W	0b	HPROT54 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
5	**HP32INT**	R/W	0b	HPROT32 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
4	**HP10INT**	R/W	0b	HPROT10 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
3	**LP54STAT**	R	0b	LPROT54 Real-time status: 0b: Comparator output low 1b: Comparator output high
2	**LP54INT**	R/W	0b	LPROT54 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
1	**LP32INT**	R/W	0b	LPROT32 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear
0	**LP10INT**	R/W	0b	LPROT10 Interrupt: 0b: No interrupt 1b: Interrupt, write 1 to clear

9.20.20 SOC.DOUTSIG0

Register 9-20 SOC.DOUTSIG0 (Digital Output 0, 19h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**VTHREF**	R/W	00b	Threshold voltage for comparators in AIO<9:6>: 00b: 0.1V 01b: 0.2V 10b: 0.5V 11b: 1.25V
5	**DOUT5**	R/W	0b	Data output to AIO5.
4	**DOUT4**	R/W	0b	Data output to AIO4.
3	**DOUT3**	R/W	0b	Data output to AIO3.
2	**DOUT2**	R/W	0b	Data output to AIO2.
1	**DOUT1**	R/W	0b	Data output to AIO1.
0	**DOUT0**	R/W	0b	Data output to AIO0.

9.20.21 SOC.DOUTSIG1

Register 9-21 SOC.DOUTSIG1 (Digital Output 1,1Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**AIOBUFSELOUT**	R/W	0b	AIO2/AIO7 buffer output select. 0b: Enable output buffer to AIO2 1b: Enable output buffer to AIO7
6:5	**AIOBUFSELIN**	R/W	0b	AIO2/AIO7 buffer input select. 00b: ADC VREF 01b: AB4 10b: AB5 11b: AB6
4	**AIOBUFEN**	R/W	0b	Enable AIO2/AIO7 buffer. 0b: Not enabled 1b: Enabled
3	**DOUT9**	R/W	0b	Data output to AIO9.
2	**DOUT8**	R/W	0b	Data output to AIO8.
1	**DOUT7**	R/W	0b	Data output to AIO7.
0	**DOUT6**	R/W	0b	Data output to AIO6.

9.20.22 SOC.DINSIG0

Register 9-22 SOC.DINSIG0 (Digital Input 0, 1Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**RFU**	R	00b	Reserved, write to 0.
5	**DIN5**	R	0b	Data input from AIO5.
4	**DIN4**	R	0b	Data input from AIO4.
3	**DIN3**	R	0b	Data input from AIO3.
2	**DIN2**	R	0b	Data input from AIO2.
1	**DIN1**	R	0b	Data input from AIO1.
0	**DIN0**	R	0b	Data input from AIO0.

9.20.23 SOC.DINSIG1

Register 9-23 SOC.DINSIG1 (Digital Input 1, 1Ch)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	000b	Reserved, write to 0.
4	**DRV_FLT**	R	0b	Driver Fault. 0b: No fault detected 1b: Fault detected
3	**DIN9**	R	0b	Data input from AIO9.
2	**DIN8**	R	0b	Data input from AIO8.
1	**DIN7**	R	0b	Data input from AIO7.
0	**DIN6**	R	0b	Data input from AIO6.

9.20.24 SOC.CFGIO1

Register 9-24 SOC.CFGIO1 (AIO10-AIO13 Configuration 1, 1Dh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	000b	Reserved, write as 0.
4	**EN_AIO6_OCP**	RW	0b	Enable AIO6 comparator output to disable gate driver on OC event.
3	**VREFBP**	RW	0b	Switch VREF signal to AB5 so that it can be buffered out on AIO6.
2:0	**RFU**	R	000b	Reserved, write as 0.

9.20.25 SOC.SIGINTEN

Register 9-25 SOC.SIGINTEN (AIO Interrupt Enable, 1Fh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**AIO9REINTEN**	R/W	0b	AIO9 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
6	**AIO8REINTEN**	R/W	0b	AIO8 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
5	**AIO7REINTEN**	R/W	0b	AIO7 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
4	**AIO6REINTEN**	R/W	0b	AIO6 digital input rising edge interrupt enable. 0b: disabled 1b: enabled
3	**AIO9FEINTEN**	R/W	0b	AIO9 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
2	**AIO8FEINTEN**	R/W	0b	AIO8 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
1	**AIO7FEINTEN**	R/W	0b	AIO7 digital input falling edge interrupt enable. 0b: disabled 1b: enabled
0	**AIO6FEINTEN**	R/W	0b	AIO6 digital input falling edge interrupt enable. 0b: disabled 1b: enabled

9.20.26 SOC.SIGINTF

Register 9-26 SOC.SIGINTF (AIO Interrupt Flag, 20h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HP32STAT**	R	0b	HPROT32 Real-time status: 0b: Comparator output low 1b: Comparator output high
6	**LP32STAT**	R	0b	LPROT32 Real-time status: 0b: Comparator output low 1b: Comparator output high
5	**HP10STAT**	R	0b	HPROT10 Real-time status: 0b: Comparator output low 1b: Comparator output high
4	**LP10STAT**	R	0b	LPROT10 Real-time status: 0b: Comparator output low 1b: Comparator output high
3	**AIO9INT**	RW	0b	AIO9 Interrupt: 0b: No Interrupt 1b: Interrupt, IRQ2 asserted. Write 1b to clear.
2	**AIO8INT**	RW	0b	AIO8 Interrupt: 0b: No Interrupt 1b: Interrupt, IRQ2 asserted. Write 1b to clear.
1	**AIO7INT**	RW	0b	AIO7 Interrupt: 0b: No Interrupt 1b: Interrupt, IRQ2 asserted. Write 1b to clear.
0	**AIO6INT**	RW	0b	AIO6 Interrupt: 0b: No Interrupt 1b: Interrupt, IRQ2 asserted. Write 1b to clear.

9.20.27 SOC.BLANKING

Register 9-27 SOC.BLANKING (Comparator Blanking Configuration, 21h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**BLANKTIME**	R/W	0000b	Blanking time for BEMF Comparator: 0000b: 100ns 0001b: 250ns 0010b: 500ns 0011b: 750ns 0100b: 1000ns 0101b: 1250ns 0110b: 1500ns 0111b: 2000ns 1000b: 2500ns 1001b: 3000ns 1010b: 3500ns 1011b: 4000ns 1100b: 4500ns 1101b: 5000ns 1110b: 5500ns 1111b: 6000ns
3:2	**RFU**	R	00b	Reserved, write as 0.
1:0	**BLANKMODE**	R/W	00b	BEMF Comparator Blanking Mode: 00b: Disabled 01b: Leading edge blanking 10b: Trailing edge blanking 11b: Leading and trailing edge blanking

9.20.29 SOC.SPECCFG0

Register 9-28 SOC.SPECCFG0 (AIO7 Comparator Hysteresis Configuration, 22h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**HYSMODE**	RW	0x0	AIO<9:7> Special Mode Comparator Hysteresis Mode: 0b: Hysteresis = 0/5/10/20 mV 1b: Hysteresis = 0/20/40/80 mV
6:4	**RFU**	R	0x0	Reserved
3:0	**AIO7HYS**	R/W	0x0	AIO7 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 0000b: Rising = 0mV, Falling = 0mV 0001b: Rising = 0mV, Falling = 5mV 0010b: Rising = 0mV, Falling = 10mV 0011b: Rising = 0mV, Falling = 20mV 0100b: Rising = 5mV, Falling = 0mV 0101b: Rising = 5mV, Falling = 5mV 0110b: Rising = 5mV, Falling = 10mV 0111b: Rising = 5mV, Falling = 20mV 1000b: Rising = 10mV, Falling = 0mV 1001b: Rising = 10mV, Falling = 5mV 1010b: Rising = 10mV, Falling = 10mV 1011b: Rising = 10mV, Falling = 20mV 1100b: Rising = 20mV, Falling = 0mV 1101b: Rising = 20mV, Falling = 5mV 1110b: Rising = 20mV, Falling = 10mV 1111b: Rising = 20mV, Falling = 20mV AIO7 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 0000b: Rising = 0mV, Falling = 0mV 0001b: Rising = 0mV, Falling = 20mV 0010b: Rising = 0mV, Falling = 40mV 0011b: Rising = 0mV, Falling = 80mV 0100b: Rising = 20mV, Falling = 0mV 0101b: Rising = 20mV, Falling = 20mV 0110b: Rising = 20mV, Falling = 40mV 0111b: Rising = 20mV, Falling = 80mV 1000b: Rising = 40mV, Falling = 0mV 1001b: Rising = 40mV, Falling = 20mV 1010b: Rising = 40mV, Falling = 40mV 1011b: Rising = 40mV, Falling = 80mV 1100b: Rising = 80mV, Falling = 0mV 1101b: Rising = 80mV, Falling = 20mV 1110b: Rising = 80mV, Falling = 40mV 1111b: Rising = 80mV, Falling = 80mV

9.20.30 SOC.SPECCFG1

Register 9-29 SOC.SPECCFG1 (AIO8/9 Comparator Hysteresis Configuration, 23h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	**AIO8HYS**	R/W	0x0	AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 0000b: Rising = 0mV, Falling = 0mV 0001b: Rising = 0mV, Falling = 5mV 0010b: Rising = 0mV, Falling = 10mV 0011b: Rising = 0mV, Falling = 20mV 0100b: Rising = 5mV, Falling = 0mV 0101b: Rising = 5mV, Falling = 5mV 0110b: Rising = 5mV, Falling = 10mV 0111b: Rising = 5mV, Falling = 20mV 1000b: Rising = 10mV, Falling = 0mV 1001b: Rising = 10mV, Falling = 5mV 1010b: Rising = 10mV, Falling = 10mV 1011b: Rising = 10mV, Falling = 20mV 1100b: Rising = 20mV, Falling = 0mV 1101b: Rising = 20mV, Falling = 5mV 1110b: Rising = 20mV, Falling = 10mV 1111b: Rising = 20mV, Falling = 20mV AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 0000b: Rising = 0mV, Falling = 0mV 0001b: Rising = 0mV, Falling = 20mV 0010b: Rising = 0mV, Falling = 40mV 0011b: Rising = 0mV, Falling = 80mV 0100b: Rising = 20mV, Falling = 0mV 0101b: Rising = 20mV, Falling = 20mV 0110b: Rising = 20mV, Falling = 40mV 0111b: Rising = 20mV, Falling = 80mV 1000b: Rising = 40mV, Falling = 0mV 1001b: Rising = 40mV, Falling = 20mV 1010b: Rising = 40mV, Falling = 40mV 1011b: Rising = 40mV, Falling = 80mV 1100b: Rising = 80mV, Falling = 0mV 1101b: Rising = 80mV, Falling = 20mV 1110b: Rising = 80mV, Falling = 40mV 1111b: Rising = 80mV, Falling = 80mV
3:0	**AIO9HYS**	R/W	0x0	AIO9 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 0: 0000b: Rising = 0mV, Falling = 0mV 0001b: Rising = 0mV, Falling = 5mV 0010b: Rising = 0mV, Falling = 10mV 0011b: Rising = 0mV, Falling = 20mV 0100b: Rising = 5mV, Falling = 0mV 0101b: Rising = 5mV, Falling = 5mV 0110b: Rising = 5mV, Falling = 10mV 0111b: Rising = 5mV, Falling = 20mV 1000b: Rising = 10mV, Falling = 0mV 1001b: Rising = 10mV, Falling = 5mV 1010b: Rising = 10mV, Falling = 10mV 1011b: Rising = 10mV, Falling = 20mV 1100b: Rising = 20mV, Falling = 0mV 1101b: Rising = 20mV, Falling = 5mV 1110b: Rising = 20mV, Falling = 10mV

				1111b: Rising = 20mV, Falling = 20mV AIO8 Special Mode Comparator Rising/Falling Hysteresis for **SOC.SPECCFG0.HYSMODE** = 1: 0000b: Rising = 0mV, Falling = 0mV 0001b: Rising = 0mV, Falling = 20mV 0010b: Rising = 0mV, Falling = 40mV 0011b: Rising = 0mV, Falling = 80mV 0100b: Rising = 20mV, Falling = 0mV 0101b: Rising = 20mV, Falling = 20mV 0110b: Rising = 20mV, Falling = 40mV 0111b: Rising = 20mV, Falling = 80mV 1000b: Rising = 40mV, Falling = 0mV 1001b: Rising = 40mV, Falling = 20mV 1010b: Rising = 40mV, Falling = 40mV 1011b: Rising = 40mV, Falling = 80mV 1100b: Rising = 80mV, Falling = 0mV 1101b: Rising = 80mV, Falling = 20mV 1110b: Rising = 80mV, Falling = 40mV 1111b: Rising = 80mV, Falling = 80mV

9.20.31 SOC.SPECCFG2

Register 9-30 SOC.SPECCFG2 (AIO7/8 Comparator MUX Input Configuration, 24h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6:4	**SMUXAIO7**	R/W	000b	Special Mode Comparator Input MUX Selection for AIO7: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO8 (phase to phase compare) 101b: AIO9 (phase to phase compare) 110b: RFU 111b: RFU
3	**RFU**	R	0b	Reserved, write to 0.
2:0	**SMUXAIO8**	R/W	000b	Special Mode Comparator Input MUX Selection for AIO8: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (phase to phase compare) 101b: AIO9 (phase to phase compare) 110b: RFU 111b: RFU

9.20.32 SOC.SPECCFG3

Register 9-31 SOC.SPECCFG3 (AIO9 Comparator MUX Input Configuration, 25h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write to 0.
6:4	**SMUXAIO9**	R/W	000b	Special Mode Comparator Input MUX Selection for AIO7: 000b: VTHREF 001b: AB1 (virtual center-tap) 010b: AB2 011b: AB3 100b: AIO7 (phase to phase compare) 101b: AIO8 (phase to phase compare) 110b: RFU 111b: RFU
3:0	**RFU**	R	000b	Reserved, write to 0.

9.20.33 SOC.GP0

Register 9-32 SOC.GP0 (General-Purpose Register Space, 26h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**VAL**	R/W	0b	General-purpose, read-write register.

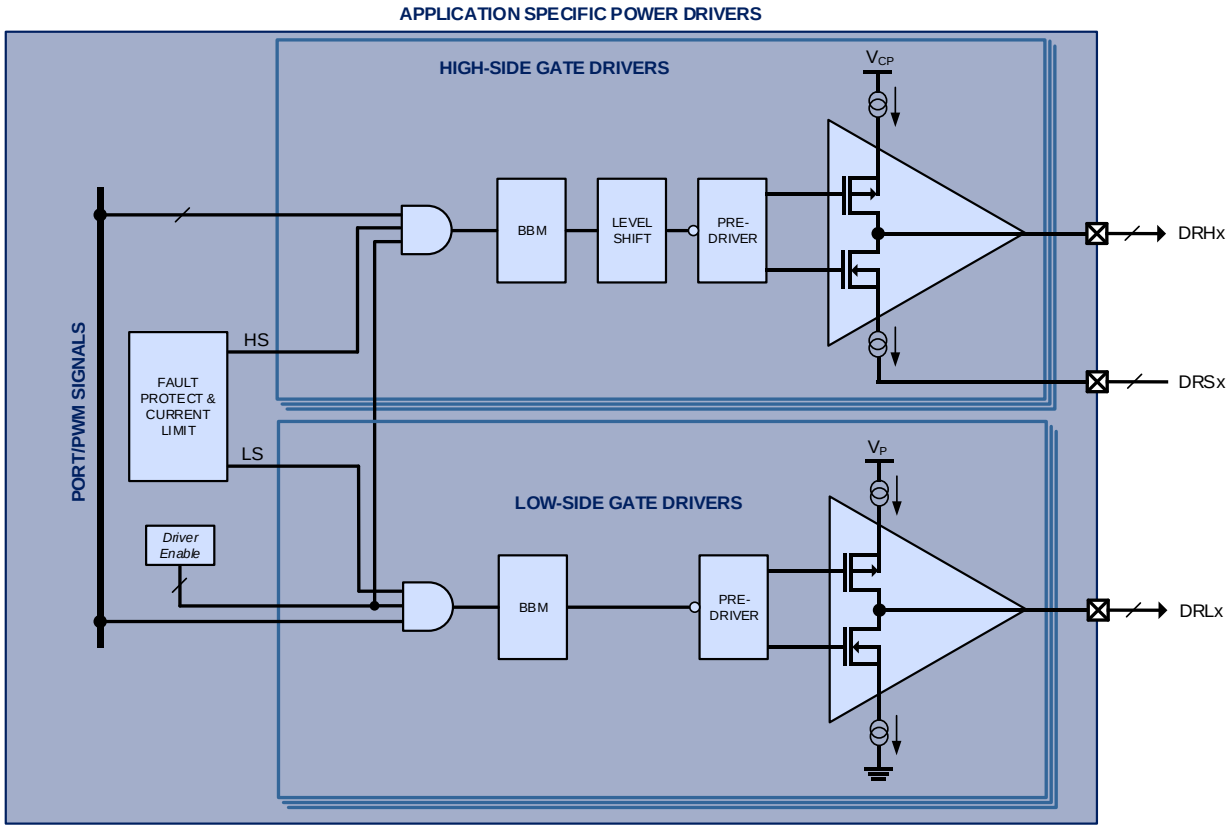
10 APPLICATION SPECIFIC POWER DRIVER

10.1 Features

- 3 high-side gate drivers with programmable gate driving up to 1A
- 3 low-side gate drivers with programmable gate driving up to 1A
- 100% duty cycle
- Cycle-by-cycle current limit
- Configurable fault protection
- Short-circuit detection

10.2 System Block Diagram

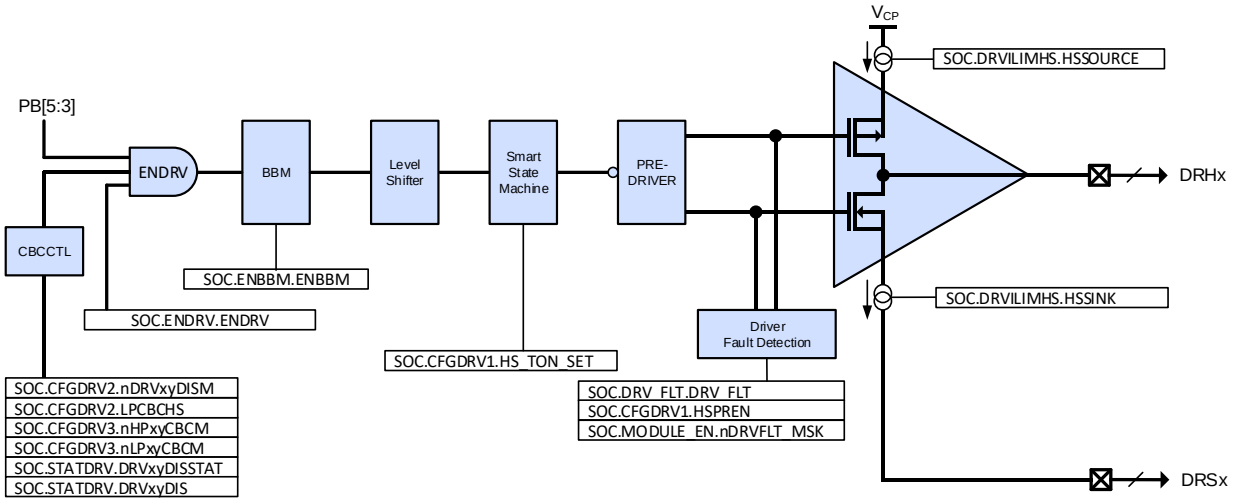
Figure 10-1 ASPD System Block Diagram



10.3 Functional Description

The Application Specific Power Drivers™ (**Error! Reference source not found.**) module handles power driving for power and motor control applications. The ASPD contains three programmable-current low-side gate drivers (DRLx), three programmable-current high-side gate drivers (DRHx). Each gate driver can drive an external MOSFET switch in response to high-speed control signals from the micro-controller ports, and a pair of high-side and low-side gate drivers can form a half-bridge driver.

Figure 10-2 High-Side Gate Driver Block Diagram



10.4 High-Side Gate Drivers

The ASPD contains 3 push-pull high-side gate drivers, with programmable sink and source current.

The DRH<2:0> outputs of the ASPD are used to drive the gate of an external high-side power MOSFET. The supply for the high-side gate drivers is V_{CP}, which is the sum of V_M + V_P. The charge pump regulates VCP based on the motor voltage (V_P) and the configured output of the MVBB (V_P).

The input to the gate drivers are from PWM timer output signals from the MCU. The MCU can configure these gate driver inputs from the PWM timer peripheral and can configure the dead-time between complementary high-side/low-side pairs.

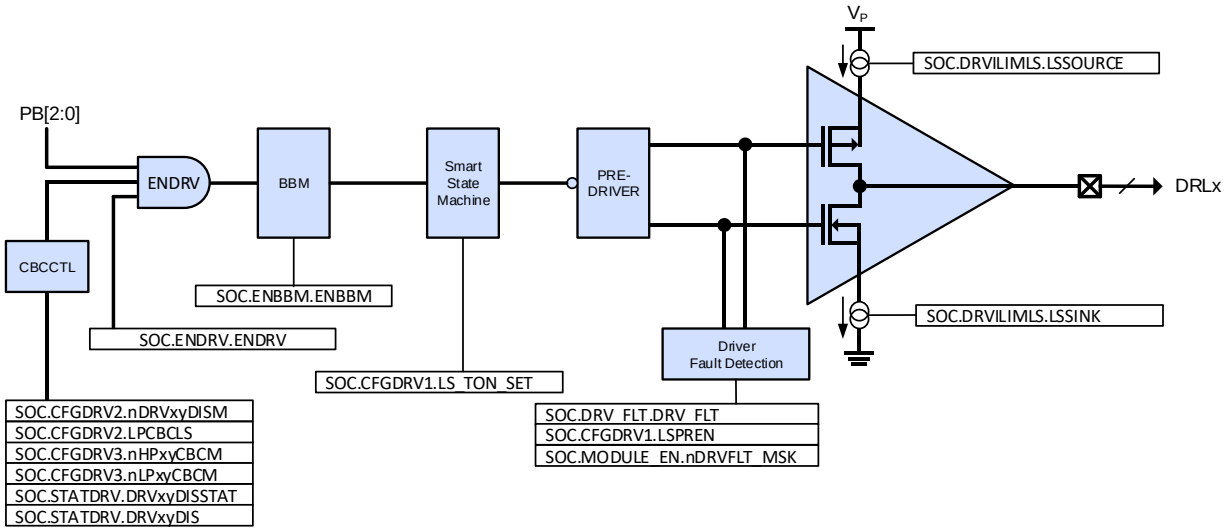
The input to the 3 high-side gate drivers are shown below:

- DRH0: PB4 (PWMA4)
- DRH1: PB5 (PWMA5)
- DRH2: PB6 (PWMA6)

10.5 Low-Side Gate Drivers

The ASPD contains 3 push-pull low-side gate drivers, with programmable sink and source current.

Figure 10-3 Low-Side Gate Driver Block Diagram



The DRL<2:0> outputs of the ASPD are used to drive the gate of an external low-side power MOSFET. The supply for the low-side gate drivers is VP, which is the output of the MVBB. VP may be configured to 10V or 12V.

The input to the gate drivers are from PWM timer output signals from the MCU. The MCU can configure these gate driver inputs from the PWM timer peripheral and can configure the dead-time between complementary high-side/low-side pairs.

The input to the 3 high-side gate drivers are shown below:

- DRL0: PB0 (PWMA4)
- DRL1: PB1 (PWMA5)
- DRL2: PB2 (PWMA6)

10.6 Enabling the ASPD

To enable the ASPD, set **SOC.ENDRV.ENDRV** to 1b.

10.7 Gate Driver Safe State

After the device is powered, both the low-side gate drivers are pulled-down and the high-side gate drivers are pulled-down using weak pull-downs. The low-side gate drivers are pulled-down to ground and the high-side gate drivers are pulled-down to the source node to put them into a safe state while the driver manager is disabled.

Once the driver manager is enabled, the gate drivers will be driven high or low according to the PWM inputs configured by the MCU.

10.8 Driver Protection

During operation the ASPD may disable the gate drivers when events such as over-current occur.

The ASPD has a protection input signal (PR) that notifies the ASPD of a protection event. If the ASPD has unmasked the high-side PR protection (**SOC.CFGDRV1.nHSPRM** = 1b) then the high-side gate drivers will be disabled. If the ASPD has unmasked the low-side PR protection (**SOC.CFGDRV1.nLSPRM** = 1b), then the low-side gate drivers will be disabled.

Once the gate drivers have been disabled, the MCU must reset the ASPD by setting **SOC.ENDRV.ENDRV** to 0b, then back to 1b in order to re-enable the ASPD.

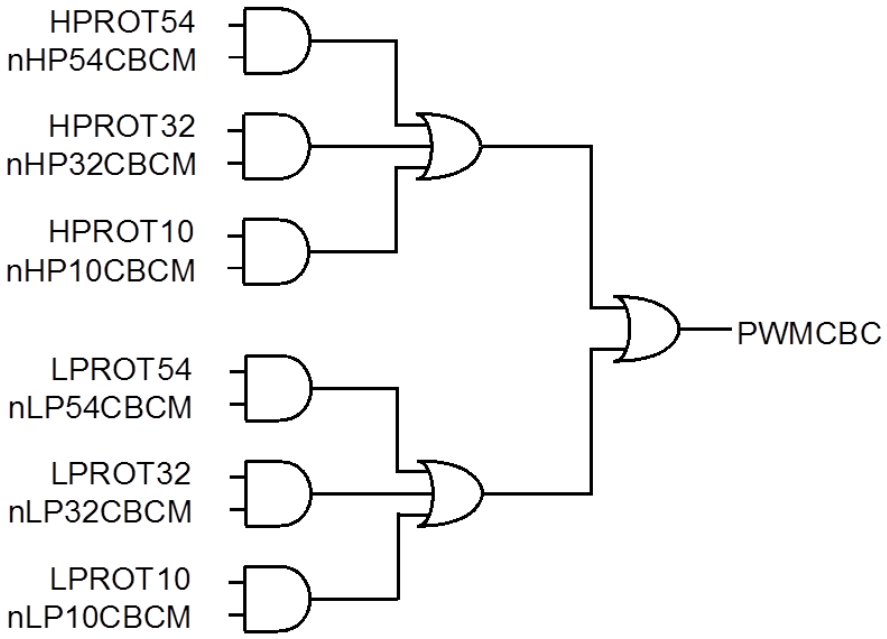
10.9 Cycle by Cycle Current Limit

To provide hardware assist for current limit, the ASPD may be configured to temporarily disable the gate drivers, when the current is over a configured threshold. This method is duty cycle truncation and is most useful in edge-aligned PWM topologies, for 120-degree commutation.

During these events, the ASPD may turn off all the high-side, low-side or high-side and low-side gate drivers based on the state of the Signal Manager HPCOMP/LPCOMP comparators. This can allow applications to have cycle by cycle current limit, without intervention of the MCU.

The diagram below shows how the protection comparators can be used to generate an event signal PWMCBC, which can be used to control this operation.

Figure 10-4 Cycle by Cycle Current Limit



The mask signal (**CFGDRV2.nDRVxyDISM**) is used to select which half-bridge to enable cycle-by-cycle current limit on, while **CFGDRV2.LPCBCHS** and **CFGDRV2.LPCBCLS** are used to select the high-side or low-side gate driver for the half-bridge to disable.

The real-time status of which half-bridge is in cycle-by-cycle current limit operation is available in **STATDRV.DRVxyDISSTAT**. The latched status is available in **STATDRV.DRVxyDIS**.

During operation, if the PWMCBC signal is high, then the output to the configured gate drivers is temporarily disabled, until the PWMCBC becomes available again. The following shows which drivers are disabled during this condition:

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV52DISM** = 1b, disable DRH5
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV52DISM** = 1b, disable DRL2

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV41DISM** = 1b, disable DRH4
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV41DISM** = 1b, disable DRL1

PWMCBC = high:

- If **CFGDRV2.LPCBCHS** = 1b and **CFGDRV2.nDRV30DISM** = 1b, disable DRH3
- If **CFGDRV2.LPCBCLS** = 1b and **CFGDRV2.nDRV30DISM** = 1b, disable DRL0

10.10 Gate Driver Short Protection

The driver manager can detect short-circuit conditions in the low-side MOSFET when enabled. To enable this feature, set **SOC.ENDRV.DRVFLTEN** (driver fault enable) to 1b.

When the low-side gate is turned off, if the DRLx voltage does not fall below the $V_{SC;DRL}$ threshold within the $t_{SC;DRL}$ time, then a fault is declared. When the low-side gate is turned on, if the DRLx voltage does not rise above the $V_{SC;DRL}$ threshold within the $t_{SC;DRL}$ time, then a fault is declared.

When the fault is declared, the driver manager will be disabled and the **SOC.DRV_FLT.DRV_FLT** bit will be set to 1b and an interrupt on IRQ1 will be asserted. To clear this condition, set **SOC.ENDRV.DRVFLTEN** to 0b then set this field to a 1b.

10.11 VP UVLO Configuration

If **SOC.CFGDRV4.VPUVLOQUAL** is set to 0b, then the VP UVLO threshold is set to $V_{UVLOR;VP}$ when VP is rising, and $V_{UVLOF;VP}$ when VP is falling.

If the **SOC.CFGDRV4.VPUVLOQUAL** is set to 1b, then the VP UVLO threshold is set as above qualified by the VP power OK threshold. For example, when VP is rising the VP UVLO threshold is set when VP crosses $V_{UVLOR;VP}$ and $k_{POKR;VP}$. When VP is falling, the VP UVLO threshold is set when VP crosses $V_{UVLOF;VP}$ and $k_{POKF;VP}$.

10.12 Break-before-make Configuration

The PAC5527 contains support for “break-before-make” gate driver safety. When **SOC.CFGDRV4.ENBBM** is set to 1b, then the gate driver will force a 100ns dead-time in between the half-bridge complementary gate drivers (DRH0/DRL0, DRH1/DRL1, DRH2/DRL2).

Note that this safety check is in addition to the programmable dead-time that the MCU inserts between the high-side and low-side gate driver inputs.

10.13 Gate Driver Programmable Current

The PAC5527 high-side and low-side gate drivers support programmable current output. This allows the gate driver to internally control the slew rate to the MOSFET gate, which eliminates the need for external series components to control the slew rate.

For both the high-side and low-side gate drivers, the user may configure the source and sink current of the gate drivers, which will be used during the miller plateau of V_{GS} to control the slew rate. The user may configure the duration of the controlled current and the current output of the gate drivers during this time.

The user may configure the controlled current between 250mA and 1A in 8 steps for both the high-side and low-side gate drivers, for sink and source current independently.

Below are the waveforms for the high-side and low-side gate drivers that are generated with the programmable current configuration.

Figure 10-5 High-side Gate Driver Waveforms

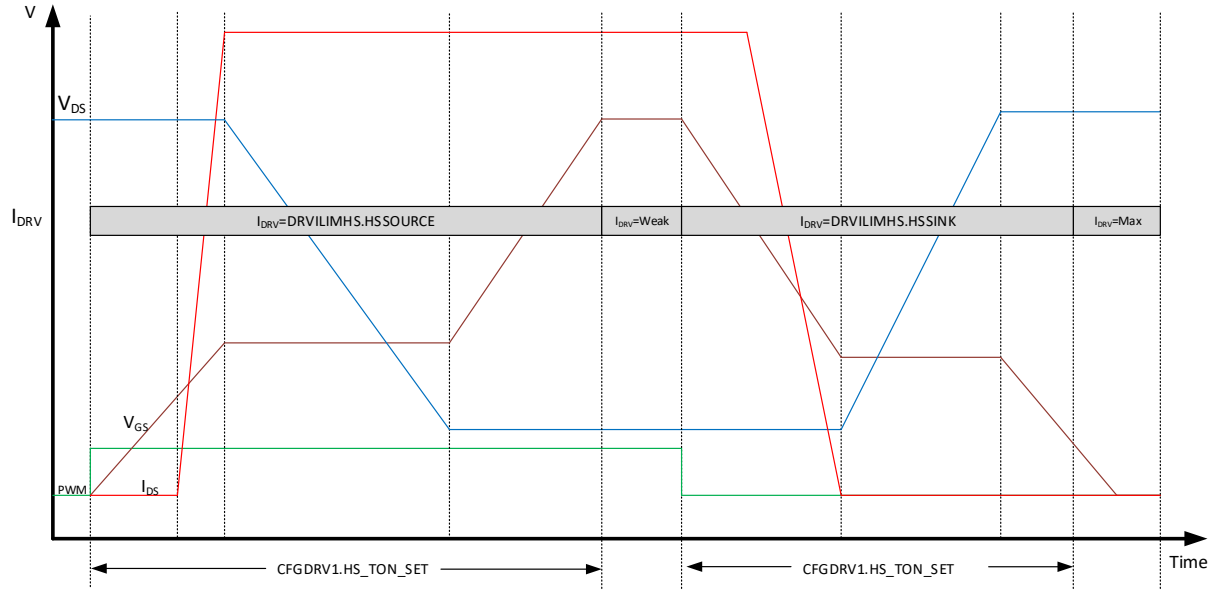
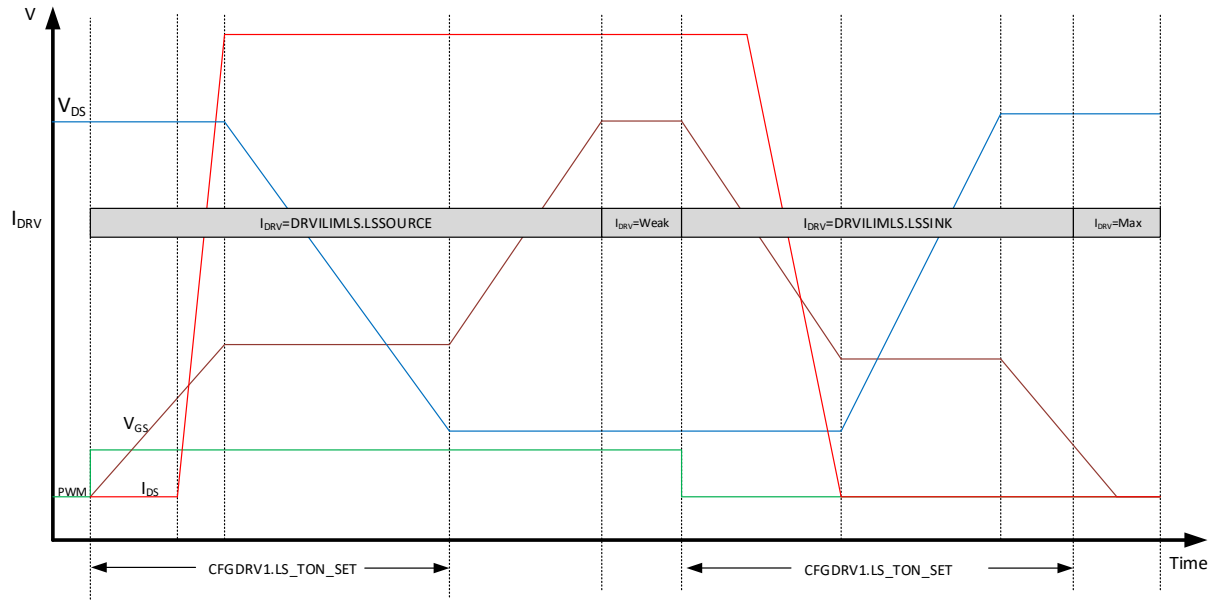


Figure 10-6 Low-side Gate Driver Waveforms



The gate driver input is a PWM signal from the MCU's PWM Timer. The user can configure the amount of time to apply the controlled current gate driver by setting the **CFGDRV1.HS_TON_SET** for the high-side gate driver, or the **CFGDRV1.LS_TON_SET** for the low-side gate driver. This is the amount of time from the input PWM edge transition during which the current is controlled.

The duration of the controlled current may be set according to the following table.

Table 10-1 ASPD Controlled-Current Time Configuration

Register	Value	Time Duration
CFGDRV1.HS_TON_SET CFGDRV1.LS_TON_SET	000b	4.7µs
	001b	2.5µs
	010b	1.8µs
	011b	1.3µs
	100b	1.1µs
	101b	0.9µs
	110b	0.75µs
	111b	0.55µs

The current that is applied during this time is configurable by the user as follows:

- High-side gate driver source current: **DRVILIMHS.HSSOURCE**
- High-side gate driver sink current: **DRVILIMHS.HSSINK**
- Low-side gate driver source current: **DRVILIMLS.LSSOURCE**
- Low-side gate driver sink current: **DRVILIMLS.LSSINK**

The source and sink current that is applied during this time is shown in the following table.

Table 10-2 ASPD Controlled-Current Time Configuration

Register	Value	Time Duration
DRVILIMHS.HSSOURCE DRVILIMHS.HSSINK DRVILIMLS.LSSOURCE DRVILIMLS.LSSINK	000b	250mA
	001b	350mA
	010b	450mA
	011b	550mA
	100b	650mA
	101b	750mA
	110b	850mA
	111b	1000mA

10.14 Register Summary

Table 10-3 ASPD Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
27h	**SOC.CFGDRV1**	Driver Configuration 1	00h
28h	**SOC.CFGDRV2**	Driver Configuration 2	00h
29h	**SOC.CFGDRV3**	Driver Configuration 3	00h
2Ah	**SOC.STATDRV**	Driver Status	00h
79h	**SOC.DRVILIMS**	Low-side Driver Current Limit Configuration	00h
7Ah	**SOC.DRVILIMH**	High-side Driver Current Limit Configuration	00h
7Bh	**SOC.CFGDRV4**	Driver Configuration 4	0x00
7Ch	**SOC.DRV_FLT**	Driver Fault Status	00h
7Dh	**SOC.ENDRV**	Driver Manager Enable	00h
7Eh	**SOC.WDTPASS**	SOC Watchdog Timer Password	00h

10.15 Register Detail

10.15.1 SOC.CFGDRV1

Register 10-1 SOC.CFGDRV1 (Driver Configuration 1, 27h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**HS_TON_SET**	R/W	0x0	High-side driver turn-on set: 000b: 4.7µs 001b: 2.5µs 010b: 1.8µs 011b: 1.3µs 100b: 1.1µs 101b: 0.9µs 110b: 0.75µs 111b: 0.55µs
4:2	**LS_TON_SET**	R/W	0x0	Low-side driver turn-on set: 000b: 4.7µs 001b: 2.5µs 010b: 1.8µs 011b: 1.3µs 100b: 1.1µs 101b: 0.9µs 110b: 0.75µs 111b: 0.55µs
1	**HSPREN**	R/W	0b	High side PR protection enable: 0b: PR disabled 1b: PR enabled
0	**LSPREN**	R/W	0b	Low side PR protection enable: 0b: PR disabled 1b: PR enabled

10.15.2 SOC.CFGDRV2

Register 10-2 SOC.CFGDRV2 (Driver Configuration 2, 28h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	**RFU**	R	0x0	Reserved
4	**nDRV52DISM**	R/W	0b	Mask signal for DRH5/DRL2 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
3	**nDRV41DISM**	R/W	0b	Mask signal for DRH4/DRL1 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
2	**nDRV30DISM**	R/W	0b	Mask signal for DRH3/DRL0 high-side, low-side or both driver disable. Used for PWM pulse cycle-by-cycle current limit: 0b: not masked 1b: masked
1	**LPCBCLS**	R/W	0b	Control signal for low-side gate drivers disable. Used for PWM pulse cycle-by-cycle current limit: 0b: Do not disable 1b: Disable when commanded
0	**LPCBCHS**	R/W	0b	Control signal for high-side gate drivers disable. Used for PWM pulse cycle-by-cycle current limit: 0b: Do not disable 1b: Disable when commanded

10.15.3 SOC.CFGDRV3

Register 10-3 SOC.CFGDRV3 (Driver Configuration 3, 29h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**nHP54CBCM**	R/W	0b	Mask signal for HPROT54 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
6	**nLP54CBCM**	R/W	0b	Mask signal for LPROT54 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
5	**nHP32CBCM**	R/W	0b	Mask signal for HPROT32 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
4	**nLP54CBCM**	R/W	0b	Mask signal for LPROT32 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
3	**nHP10CBCM**	R/W	0b	Mask signal for HPROT10 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
2	**nLP10CBCM**	R/W	0b	Mask signal for LPROT10 for PWM pulse cycle-by-cycle current limit: 0b: masked 1b: not masked
1:0	**RFU**	R	00b	Reserved, write as 0.

10.15.4 SOC.STATDRV

Register 10-4 SOC.STATDRV (Driver Status, 2Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	**RFU**	R	00b	Reserved, write as 0.
5	**DRV52DISSTAT**	R	0b	Real-time status of DRV52DIS signal: 0b: Driver disable inactive 1b: Driver disable active
4	**DRV41DISSTAT**	R	0b	Real-time status of DRV41DIS signal: 0b: Driver disable inactive 1b: Driver disable active
3	**DRV30DISSTAT**	R	0b	Real-time status of DRV30DIS signal: 0b: Driver disable inactive 1b: Driver disable active
2	**DRV52DIS**	R	0b	Latched status of DRV54DIS signal. To clear, write this bit to a 1b: 0b: No driver disable event 1b: Driver disable event occurred
1	**DRV32DIS**	R	0b	Latched status of DRV32DIS signal. To clear, write this bit to a 1b: 0b: No driver disable event 1b: Driver disable event occurred
0	**DRV10DIS**	R	0b	Latched status of DRV10DIS signal. To clear, write this bit to a 1b: 0b: No driver disable event 1b: Driver disable event occurred

10.15.5 SOC.DRVILIMLS

Register 10-5 SOC.DRVILIMLS (Low-side Driver Current Limit Configuration, 79h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write as 0b.
6:4	**LSSINK**	R/W	000b	Low-side gate driver programmable sink current: 000b: 250mA 001b: 350mA 010b: 450mA 011b: 550mA 100b: 650mA 101b: 750mA 110b: 850mA 111b: 1000mA
3	**RFU**	R	0b	Reserved, write as 0b.
2:0	**LSSOURCE**	R/W	000b	Low-side gate driver programmable source current: 000b: 250mA 001b: 350mA 010b: 450mA 011b: 550mA 100b: 650mA 101b: 750mA 110b: 850mA 111b: 1000mA

10.15.6 SOC.DRVILIMHS

Register 10-6 SOC.DRVILIMHS (High-side Driver Current Limit Configuration, 7Ah)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	**RFU**	R	0b	Reserved, write as 0b.
6:4	**HSSINK**	R/W	000b	High-side gate driver programmable sink current: 000b: 250mA 001b: 350mA 010b: 450mA 011b: 550mA 100b: 650mA 101b: 750mA 110b: 850mA 111b: 1000mA
3	**RFU**	R	0b	Reserved, write as 0b
2:0	**HSSOURCE**	R/W	000b	High-side gate driver programmable source current: 000b: 250mA 001b: 350mA 010b: 450mA 011b: 550mA 100b: 650mA 101b: 750mA 110b: 850mA 111b: 1000mA

10.15.7 SOC.CFGDRV4

Register 10-7 SOC.CFGDRV4 (Driver Configuration 4, 7Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	**RFU**	R	0x0	Reserved
1	**VPUVLOQUAL**	R/W	0b	VP UVLO Power-OK qualify: 0b: VP UVLO determined by just VP threshold 1b: VP UVLO determined by VP threshold and VP power-OK threshold
0	**ENBBM**	R/W	0b	Enable Break-before-make: 0b: Do not enable break-before-make protection 1b: Enable break-before-make protection

10.15.8 SOC.DRV_FLT

Register 10-8 SOC.DRV_FLT (Driver Fault Flat, 7Ch)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	**RFU**	R	0b	Reserved
2	**CPFLT**	R/W	0b	Charge pump fault flag: 0b: No fault event 1b: Charge Pump Fault, write 1b to clear. **SOC.ENDRV.ENDRV** will be reset to 0b during this event.
1	**CPFLTSTAT**	R	0b	Charge pump fault real-time status: This is the real-time status of the charge pump fault. When the charge pump is disabled, this value will be 0b.
0	**DRV_FLT**	R	0b	Driver fault flag: 0b: no flag 1b: flag

10.15.9 SOC.ENDRV

Register 10-9 SOC.ENDRV (Driver Manager Enable, 7Dh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	**RFU**	R	000 0000b	Reserved, write as 0.
0	**ENDRV**	RW	0b	Driver Manager Enable: 0b: Disable 1b: Enable

10.15.10 SOC.WDTPASS

Register 10-10 SOC.WDTPASS (WDT Password, 7Eh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	**WDTPASS**	RW	0000 0000b	To reset the SOC Watchdog Timer, write this field to ACh.

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