ACT88325 Register Definition

Abstract

This application note identifies and explains the ACT88325 and ACT88326 internal registers that help make these ICs flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. The default register settings in this application note are only valid for the ACT88325VA101. Refer to each datasheet for each specific IC's functional differences from the settings in this document.

Introduction

The ACT8832x is an ActivePMU power management unit from Active-Semi. It is designed to power a wide range of processors, FPGA's, peripherals, microcontroller and solid-state drive applications. The ACT8832x core includes 3 DC/DC step down converters using integrated power FETs and 2 low-dropout regulators (LDOs). Each regulator can be configured for a wide range of output voltages through the I2C interface.

Today's processors require more complexity in their startup and sequencing requirements. This is also true for entering and exiting sleep and low power modes. The ACT8832x is specifically designed to meet today's processors' stringent power system requirements. These processors include, but are not limited to

Although the ACT8832x is programmed at the factory with a default configuration, these settings can be changed through the I2C interface to provide customized configurations optimized for a specific processor and/or end application. IC configurability includes many options such as output voltage, startup sequencing, startup timing, slew rates, GPIO configuration, fault responses, and more. Active-Semi identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT88325's CMI 101. Refer to the datasheet for the specific changes to other CMI versions.

Register Types

The ACT8832x ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

Factory Non-Volatile – Factory bits. These bits are used by the factory to set IC functionality. The customer can read these bits, but cannot write to them. The default values can be modified at the factory to optimize IC functionality for specific applications.

The ACT8832x contains seven major register spaces.

Master Reg	0x00h to 0x1Fh
Buck1 Reg	0x30h to 0x3Fh
Buck2 Reg	0x40h to 0x4Fh
Buck3 Reg	0x50h to 0x5Fh
LDO12 Reg	0xA0h thru 0xAFh
Load Switch Reg	0xE5h thru 0xEFh

Register Map Overview

The following table show an overview of the ACT8832x register map. Note that not all register addresses are sequential.

	Master Registers							
Address (HEX)	7	6	5	4	3	2	1	0
00	RFU	WD TIMER ALERT	TWARN	VSYSSTAT	PC STAT	SR STAT	PBASTAT	PBDSTAT
01	RFU	WD ALERT MSK	TMSK	VSYSMSK	PC STAT MASK	SR STAT MASK	PBAMSK	PBDMSK
02	FACTORY MODE	RFU	RFU	VSYSDAT	RFU	RFU	RFU	PBDAT
03	TRST_DLY[1:0]		PB WAIT TIME SET [1:0]		VSYSMON			
04	EN _SKIP_LPM	EN BUCK1 BYP MODE	ALL BUCKS FASTER SS	DIS DPSLP PWROFF DELAY	IOB2 DELAY EN	IOB1 DEL EN	DIS OV UV SHUTDOWN	ANA MODE EN
05	RFU							
06	RFU							
07	RFU							
08	RFU							
09	RFU		DIS OTS	SLEEP MODE	DPSLP MODE	RFU		
0E	RFU			VIN_OV_SEL	BUCK1_VREFMUX	RFU		
12	INTADR							
13	PB COUNTER							
14	RFU	RFU	RFU	OK_START	RFU	WAKETRG	WDPCEN	WDSREN
15	RFU	RFU	POWER OFF	MR	SLEEP	SLEEP EN	DPSLP	DPSLP EN
16	LED1 DBL BLINK	LED_DELAY1<2:0>			ILED1<3:0>			
17	LED2 DBL BLINK	LED_DELAY2<2:0>			ILED2<3:0>			
18	LED_BREATHE1_EN	PWMFREQ1			PWMDUTY1			
19	LED_BREATHE2_EN	PWMFREQ2			PWMDUTY2			
1B	RFU						GPIO2 STAT	GPIO1 STAT
1C	RFU						GPIO2 INTR	GPIO1 INTR
1D	RFU						GPIO2 MASK	GPIO1 MASK
	Buck1							
30	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
31	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
32	VSET0							
33	VSET1							
34	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	RFU
35	MODE	RST	DBQL				DBOK	
36	DBON				ON DELAY		DBSTBY	
37	PHASE_DELAY	PHASE	DISLPM	OFF DELAY				
	Buck2							
40	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
41	RFU							
42	VSET0							
43	VSET1							
44	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	RFU
45	MODE	RST	DBQL				DBOK	
46	DBON				ON DELAY		DBSTBY	
47	PHASE_DELAY	PHASE	DISLPM	OFF DELAY				
	Buck3							
50	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
51	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
52	VSET0							
53	VSET1							
54	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_SET	RFU
55	MODE	RST	DBQL				DBOK	
56	DBON				ON DELAY		DBSTBY	
57	PHASE_DELAY	PHASE	DISLPM	OFF DELAY				
	LDO1/2							
A0	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
A1	LDO 1 VSET							
A2	ON LDO1	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
A3	OFF DELAY					DBOK		
A4	DBON				MODE	RST	ON DELAY	
A5	RFU							
A6	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2	ILIM_FLTMSK_LDO2	RFU
A7	LDO 2 VSET							
A8	ON LDO2	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
A9	OFF DELAY					DBOK		
AA	DBON				MODE	RST	ON DELAY	
AC	RFU	VREF CTRL	RFU					
AD	QLTCH LDO2	QLTCH LDO1	ILIM2<1:0>		ILIM1<1:0>		LDO2 ILIM SHUTDOWN DIS	LDO1 ILIM SHUTDOWN DIS
	Load Switch							
E5	RFU	RFU	LOAD SW1 PGOOD/UV	LOAD SW1 ILIM FLT	RFU	RFU	LOAD SW1 PGOOD FLT MASK	LOAD SW1 ILIM FLT MASK
E6	BUCK1_BYP_ISS		GATE1 SLEW		RFU	RFU	QLTCH1	RFU
E7	ON_LSW	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
E8	OFF DELAY					DBOK		
E9	DBON				MODE	RST	ON DELAY	
EA	RFU							
EB	RFU			LDO1_ADJ_ILIM	LDO2_ADJ_ILIM	EN_DVS_I2C	SEL_DVS_IN	I2C_DVS_ON
EC	EXT_EN_DWN_AT_SLEEP_EN	EXT_EN_DWN_AT_DPSLP_EN	LDO1_LSW_MODE	RFU	ILIM_BUCK3[0]	ILIM_BUCK1[0]	ILIM_BUCK2[0]	REF_SEL_BUCK2

MASTER REGISTERS

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	TWARN	VSYSSTAT	PC STAT	SR STAT	PBASTAT	PBDSTAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
TWARN	0 – Junction temperature < TWARN Threshold 1 - Junction temperature > TWARN Threshold	Thermal Warning Status Bit
VSYSSTAT	0 – VSYS > VSYS Monitor Threshold 1 - VSYS < VSYS Monitor Threshold	VSYS UV Status
PC STAT	0 – Power Cycle has not triggered 1 – Power Cycle was triggered	Power Cycle Status. Note that this is only valid for the ACT88326 CMIs.
SR STAT	0 – Soft Reset was not triggered 1 – Soft Reset was triggered	Soft reset Status. Note that this is only valid for the ACT88326 CMIs.
PBASTAT	0 – Push Button was not asserted 1 – Push Button was asserted	Push Button Assert Status. Note that this is only valid for the ACT88326 CMIs.
PBDSTAT	0 – Push button was de-asserted 1 – Push button was asserted	Push Button de-assert status. Note that this is only valid for the ACT88326 CMIs.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	WD ALERT MSK	TMSK	VSYSMSK	PC STAT MSK	SR STAT MSK	PBAMSK	PBDMSK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Do not change this register value. Changing the register value can affect IC functionality.
WD ALERT MSK	0 – Clear Mask 1 – Mask enabled	Watch Dog Timer Expiration interrupt mask bit
TMSK	0 – Clear Mask 1 – Mask enabled	Thermal Warning Status Bit interrupt mask bit
VSYMSK	0 – Clear Mask 1 – Mask enabled	VSYS UV interrupt mask bit
PC STAT MSK	0 – Clear Mask 1 – Mask enabled	Power Cycle interrupt mask bit. Note that this is only valid for the ACT88326 CMIs.
SR STAT MSK	0 – Clear Mask 1 – Mask enabled	Soft reset interrupt mask bit. Note that this is only valid for the ACT88326 CMIs.
PBAMSK	0 – Clear Mask 1 – Mask enabled	Push Button Assert interrupt mask bit. Note that this is only valid for the ACT88326 CMIs.
PBDMSK	0 – Clear Mask 1 – Mask enabled	Push Button de-assert interrupt mask bit. Note that this is only valid for the ACT88326 CMIs.

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	FACTORY MODE	RFU [1:0]		VSYSDAT	RFU	RFU	RFU	PBDAT
Default	0	00		0	0	0	0	0
Access	RO	R/W		RO	R/W	R/W	R/W	R/W

Name	Description	Notes
FACTORY MODE	0 – In normal mode 1 – In Factory Mode	Status indicator to show that the IC is operating normally. Factory mode is not user accessible.
RFU	Reserved for Future Use	
VSYSDAT	0 – VIN is higher than VSYSMON 1 – VIN is lower than VSYSMON	Real time status of the input voltage being above or below the VSYSMON threshold
RFU	Reserved for Future Use	
PBDAT	0 – Push Button is being asserted 1 – Push Button is de-assert	Real time status of the push button pin

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	TRST_DLY [1:0]		PB WAIT TIME SET [1:0]		VSYSMON [3:0]			
Default	00		00		0000			
Access	R/W		R/W		R/W			

Name	Description	Notes
TRST_DLY [1:0]	nRESET Delay Timer - On – See spec EC tables for settings.	See electrical characteristics tables in data sheet for available settings.
PB WAIT TIME SET [1:0]	Push Button Wait time for power on	See electrical characteristics tables in data sheet for available settings. Note that this is only valid for the ACT88326 CMIs.
VSYSMON [3:0]	Configuration for VSYS Monitor (VSYSMON) interrupt threshold. Checks the falling edge of VSYS voltage and issues an interrupt when VSYS < VSYSMON threshold.	See electrical characteristics tables in data sheet for available settings.

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x48h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_SKIP_ LPM	ENB1BYP MODE	BUCKS FAST SS	DIS DPSLP PWROFF DELAY	IOB2 DELAY EN	IOB1 DELAY EN	DIS OVUV SHDN	ANA MODE EN
Default	0	1	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
EN_SKIP_LPM	0 – Disable Skip Mode in Buck1 1 – Enable Skip Mode in Buck1	
ENB1BYP MODE	0 – Disable Buck 1 Bypass Mode 1 – Enable Buck 1 Bypass Mode	
BUCKS FAST SS	0 – Slow soft start ramp for BUCKs 1 – All Bucks have a faster soft start ramp	
DIS DPSLP PWROFF DELAY	0 – Enable power off delay when entering DPSLP state 1 – Disable power off delay when entering DPSLP state	
IOB2 DELAY EN	0 – Disable 2.5ms Delay for IOB2 (GPIO2) 1 – Enable 2.5ms Delay for IOB2 (GPIO2)	
IOB1 DELAY EN	0 – Disable 2.5ms Delay for IOB1 (GPIO1) 1 – Enable 2.5ms Delay for IOB1 (GPIO1)	
DIS OVUV SHDN	0 – Enable hiccup mode or OVUVFLT state in PWREN Mode 1 – Disable hiccup mode or OVUVFLT state in PWREN Mode	
ANA MODE EN	0 – Disable GPIO3 and GPIO4 when configured as an analog GPIO (LED Drivers) 1 – Enable GPIO4 and GPIO4 when configured as an analog GPIO (LED Drivers)	NOTE: ANA MODE EN is not used if the GPIO3 and GPIO4 are not configured to Analog Mode. GPIO3 and GPIO4 would be configured as digital I/O in this case.

RFU - RFU

Address = 0x05h – 0x08h	Default = N/A	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	N/A							
Access	R/W							

Name	Description	Notes
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0x0Bh	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	DIS_OTS	SLEEP_MODE	DPSLP_MODE	RFU		
Default	0	0	0	0	1	011		
Access	RO	RO	RO	RO	RO	RO		

Name	Description	Notes
RFU		
RFU		
DIS_OTS	0 – Normal overtemperature shutdown operation 1 – Disable overtemperature shutdown	
SLEEP_MODE	0 – Disable SLEEP Mode 1 – Enable SLEEP Mode	
DPSLP_MODE	0 – Disable DPSLP Mode 1 – Enable DPSLP Mode	
RFU		

MSTR0E - Master Configuration Register

Address = 0x0Eh	Default = 0x90h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU			VIN_OV_SEL	BK1_REFMUX	RFU		
Default	100			1	0	00		
Access	R/W			RO	RO	RO		

Name	Description	Notes
RFU		
VIN_OV_SEL	0 – VIN_OV = 5.7V 1 – VIN_OV = 3.8V	
BK1_REFMUX	0 – Buck1 reference voltage = 0.8V 1 – Buck1 reference voltage = 0.6V	
RFU		

MSTR12 - Master Configuration Register

Address = 0x12h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INTADR [7:0]							
Default	00000000							
Access	RO							

Name	Description			Notes
INTADR [7:0]	Value	I2C Register	Register Function	The value contained in this register identifies the I2C register that generated the interrupt.
	0x01h	0x00h	System Level Functions	
	0x02h	0x1Ch	System Level Functions	
	0x30h	0x30h	Buck1	
	0x40h	0x40h	Buck2	
	0x50h	0x50h	Buck3	
	0xA1h	0xA0h	LDO1	
	0xA2h	0xA6h	LDO2	
	0xE1h	0xE5h	Load Switch	

MSTR13 - Master Configuration Register (For ACT88326 only)

Address = 0x0Ah	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PB COUNTER [7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
PB COUNTER [7:0]	Displays the time that PB is asserted	The counter time = PB COUNTER * 64ms

MSTR14 - Master Configuration Register

Address = 0x14h	Default = 0x10h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [2:0]			OK_START	RFU	WAKETRG	WDPCEN	WDSREN
Default	000			1	0	0	0	0
Access	R/W			R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU [2:0]	Reserved for future use	Do not change these bits
OK_START	0 – Prevents wakeup from DPSLP or SLEEP mode by the nPB pins. 1 – Allows wakeup from DPSLP or SLEEP mode by the nPB pins.	
RFU	Reserved for future use	Do not change this bit
WAKETRG	0 – Not used 1 – Not used	Changing this bit does not affect IC operation
WDPCEN	0 – IC does not power cycle if the watchdog timer times out 1 – IC power cycles if the watchdog timer times out	Note that this is a higher priority than WDSREN
WDSREN	0 – Disables a soft reset if the watchdog timer times out 1 – Enables a soft reset if the watchdog timer times out	

MSTR15 – Master Configuration Register

Address = 0x15h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	SHIP MODE	RFU	POWER OFF	MR	SLEEP	SLEEP EN	DPSLP	DPSLP EN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
SHIP MODE	0 – Not used 1 – Not used	Changing this bit does not affect IC operation
RFU	Reserved for future use	Do not change this bit
POWER OFF	0 – IC is operating normally 1 – IC Defaults to POWER OFF = 1 and all regulators are off when POWER OFF = 1 upon power up.	Clear Power Off to 0 using I2C to start a power on sequence. It is similar to a push button assertion to start power up sequence. Note that this bit is only valid for the ACT88326.
MR	0 – No Manual Reset 1 – Initiate a Manual Reset or Power Cycle by setting this bit by I^2C	Power cycle by I2C using this bit. Note that this bit is only valid for the ACT88326.
SLEEP	0 – PMIC operates in power on state 1 – PMIC enters into SLEEP state	Initial SLEEP state using I2C by setting this bit to 1 and exit SLEEP state
SLEEP EN	0 – SLEEP Mode is disabled 1 – SLEEP Mode is enabled	NOTE: This bit is not used in Push Button Configuration but is used in PWREN Configuration.
DPSLP	0 – PMIC operates in power on state 1 – PMIC Enters into DPSLP Mode	
DPSLP EN	0 – DPSLP Mode is disabled 1 – DPSLP Mode is enabled	NOTE: This bit is not used in Push Button Configuration but is used in PWREN Configuration.

MSTR16 – Master Configuration Register (Only available when GPIO3 is configured as an LED driver)

Address = 0x16h	Default = 0x08h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED1 DBL BLINK	LED_DELAY1[2:0]			ILED1[3:0]			
Default	0	000			1000			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED1 DBL BLINK	0 – LED blinks once per cycle 1 – LED blinks twice per cycle	
LED_DELAY1[2:0]	Control bits to set the delay as a percentage of LED time period from start of the LED Clock edge (equivalent to phase delay) for GPIO3 / GPIOD1	
ILED1[5:0]	Control bits to set peak current level in LED driver mode for GPIO3	

MSTR17 – Master Configuration Register (Only available when GPIO4 is configured as an LED driver)

Address = 0x17h	Default = 0x08h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED2 DBL BLINK	LED_DELAY2 [2:0]			ILED2 [3:0]			
Default	0	000			1000			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED2 DBL BLINK	0 – LED blinks once per cycle 1 – LED blinks twice per cycle	
LED_DELAY2 [2:0]	Control bits to set the delay as a percentage of LED time period from start of the LED Clock edge (equivalent to phase delay) for GPIO3 / 4	
ILED2 [5:0]	Control bits to set peak current level in LED driver mode for GPIO3 / 4	

MSTR18 – Master Configuration Register (Only available when GPIO3 is configured as an LED driver)

Address = 0x18h	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED_BREATHE1_EN	PWMFREQ1[2:0]			PWMDUTY1[3:0]			
Default	0	000			0010			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED1 BREATHE1 EN	0 – Disable Breathe Mode 1 – Enable Breathe Mode	Current steps through from minimum to maximum current setting code in stair step manner.
PWMFREQ1 [2:0]	PWM Frequency setting for LED1	
PWMDUTY1 [3:0]	PWM Duty cycle setting for LED1	

MSTR19 – Master Configuration Register (Only available when GPIO4 is configured as an LED driver)

Address = 0x19h	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED_BREATHE2_EN	PWMFREQ2 [2:0]			PWMDUTY2 [3:0]			
Default	0	000			0010			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED1 BREATHE2 EN	0 – Disable Breathe Mode 1 – Enable Breathe Mode	Current steps through from minimum to maximum current setting code in stair step manner.
PWMFREQ2 [2:0]	PWM Frequency setting for LED2	
PWMDUTY2 [3:0]	PWM Duty cycle setting for LED2	

MSTR1B – Master Configuration Register

Address = 0x1Bh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [5:0]						GPIO2 STAT	GPIO1 STAT
Default	000000						0	0
Access	R/W						RO	RO

Name	Description	Notes
RFU [0:5]	Reserved for future use	Do not change these bits
GPIO2 STAT	0 – GPIO2 input is logic low 1 – GPIO2 input is logic high	Shows the GPIO input status when the GPIO is configured as an input.
GPIO1 STAT	0 – GPIO1 input is logic low 1 – GPIO1 input is logic high	Shows the GPIO input status when the GPIO is configured as an input.

MSTR1C – Master Configuration Register

Address = 0x1Ch	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [5:0]						GPIO2 INTR	GPIO1 INTR
Default	000000						0	0
Access	R/W						RO	RO

Name	Description	Notes
RFU [0:5]	Reserved for future use	Do not change these bits
GPIO2 INTR	0 – GPIO2 status has not changed 1 – GPIO2 status has changed	A GPIO input value change sets this bit and generates an interrupt if the mask bit is 0
GPIO1 INTR	0 – GPIO1 status has not changed 1 – GPIO1 status has changed	A GPIO input value change sets this bit and generates an interrupt if the mask bit is 0

MSTR1D – Master Configuration Register

Address = 0x1Dh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [5:0]						GPIO2 MASK	GPIO1 MASK
Default	000000						1	1
Access	R/W						R/W	R/W

Name	Description	Notes
RFU [0:5]	Reserved for future use	Do not change these bits
GPIO2 MASK	0 – GPIO2 Interrupt is not masked 1 – GPIO2 Interrupt is masked	GPIO status change triggers an interrupt if the GPIO input value changes if unmasked.
GPIO1 MASK	0 – GPIO2 Interrupt is not masked 1 – GPIO2 Interrupt is masked	GPIO status change triggers an interrupt if the GPIO input value changes if unmasked.

BUCK REGULATORS REGISTERS

Buck1 Registers

B1_REG00 – Buck1 Configuration Register

Address = 0x30h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	0 – Buck1 voltage is below the power good threshold 1 – Buck1 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck1 voltage is above the overvoltage threshold 1 – Buck1 voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – Buck1 is below the ILIM threshold 1 – Buck1 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	0 – Buck1 is below the ILIM warning threshold 1 – Buck1 is above the ILIM warning threshold	Provides real-time current limit warning status
UV_FLTMSK	0 – Unmasks the Buck1 POK signal 1 – Masks the Buck1 POK signal	When 1, the Buck1 POK signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is disabled or drops out of regulation. B1_POK still provides real-time power good status.
OV_FLTMSK	0 – Unmasks the Buck1 OV register 1 – Masks the Buck1 OV register	When 1, the Buck1 OV signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. B1_OV still provides real-time OV status.
ILIM_FLTMSK	0 – Unmasks the Buck1 ILIM register 1 – Masks the Buck1 ILIM register	When 1, the ILIM fault bit is masked from the master fault register. ILIM still provides real-time current limit status.
ILIM_WARN_FLTMSK	0 – Unmasks the Buck1 ILIM_WARN register 1 – Masks the Buck1 ILIM_WARN register	When 1, the ILIM_WARN fault bit is masked from the master fault register. ILIM_WARN still provides real-time current limit warning status.

B1_REG01 – Buck1 Configuration Register

Address = 0x31h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
RFU [7:0]	Reserved for future use	Do not change these bits

B1_VSET00 – Buck1 Voltage Set0 Register

Address = 0x32h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0 [7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
B1_VSET0[7:0]	Buck1 output voltage setting in ACTIVE mode.	Controls the Buck1 output voltage. B1_VSET0 is used in ACTIVE mode. When the Buck1 reference voltage is set to 0.8V, the output voltage is equal to VSET * 0.0125 + 0.8V. When the Buck1 reference voltage is set to 0.6V, the output voltage is equal to VSET*0.009375 + 0.6V. Note that the Buck1 reference voltage setting is not user controllable. The CMI 101 Buck1 is configured in Bypass mode, so this bit is not used

B1_VSET01 – Buck1 Voltage Set1 Register

Address = 0x33h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1 [7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
VSET1 [7:0]	Buck1 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck1 output voltage. B1_VSET1 is used in DVS or SLEEP modes. The output voltage setting is the same as the B1_VSET0 register.

B1_REG04 – Buck1 Configuration Register

Address = 0x34h	Default = 0xD4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DP_SLEEP_EN	ILIM_SET	RFU
Default	1	1	0	1	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Buck1 is enabled through normal sequencing 1 – Buck1 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	0 – Buck1 does not respond to push button inputs 1 – Buck1 turns on and responds to push button inputs	This bit should not be changed during operation to avoid unexpected behavior.
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Auxiliary Input cannot turn on / turn off regulator 1 – Auxiliary Input can be used to turn on / turn off regulator	An Auxiliary input could be a GPIO control input pin as an example.
DP_SLEEP_EN	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	
ILIM_SET	0 – Peak current limit set to 4.6A 1 – Peak current limit set to 3.0A	
RFU	Reserved for Future Use	Do not change this register bit. Changing the register bit may result in unexpected IC behavior.

B1_REG05 – Buck1 Configuration Register

Address = 0x35h	Default = 0x9Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	011			100		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck1 does not affect nRESET output 1 – Buck1 turning off asserts nRESET output low	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG06 – Buck1 Configuration Register

Address = 0x36h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				ON_DELAY [1:0]		DBSTBY [1:0]	
Default	0000				10		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ON_DELAY [1:0]	00 = no delay 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms	Programs the delay time between the Buck1 input trigger and when it turns on.
DBSTBY [1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG07 – Buck1 Configuration Register

Address = 0x37h	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	DISLPM	OFF_DELAY [4:0]				
Default	1	1	0	00010				
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	
DISLPM	0 – Low Power Mode enabled 1 – Low Power Mode disabled	
OFF_DELAY [4:0]	Sets the delay time between the Buck1 disable input to when it turns off.	Buck1 turnoff delay time is equal to OFF_DELAY * 0.25ms

BUCK2 REGULATOR REGISTERS

B2_REG00 – Buck2 Configuration Register

Address = 0x40h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	0 – Buck2 voltage is below the power good threshold 1 – Buck2 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck2 voltage is above the overvoltage threshold 1 – Buck2 voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – Buck2 is below the ILIM threshold 1 – Buck2 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	0 – Buck2 is below the ILIM warning threshold 1 – Buck2 is above the ILIM warning threshold	Provides real-time current limit warning status
UV_FLTMSK	0 – Unmasks the Buck2 POK signal 1 – Masks the Buck2 POK signal	When 1, the Buck2 POK signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is disabled or drops out of regulation. B1_POK still provides real-time power good status.
OV_FLTMSK	0 – Unmasks the Buck2 OV register 1 – Masks the Buck2 OV register	When 1, the Buck2 OV signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. OV still provides real-time OV status.
ILIM_FLTMSK	0 – Unmasks the Buck2 ILIM register 1 – Masks the Buck2 ILIM register	When 1, the ILIM fault bit is masked from the master fault register. ILIM still provides real-time current limit status.
ILIM_WARN_FLTMSK	0 – Unmasks the Buck2 ILIM_WARN register 1 – Masks the Buck2 ILIM_WARN register	When 1, the ILIM_WARN fault bit is masked from the master fault register. ILIM_WARN still provides real-time current limit warning status.

B2_REG01 – Buck2 Configuration Register

Address = 0x41h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
RFU [7:0]	Reserved for future use	Do not change these bits

B2_VSET00 – Buck2 Voltage Set0 Register

Address = 0x42h	Default = 0x20h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0 [7:0]							
Default	00100000							
Access	R/W							

Name	Description	Notes
VSET0 [7:0]	Buck2 output voltage setting in ACTIVE mode.	Controls the Buck2 output voltage. B2_VSET0 is used in ACTIVE mode. When the Buck2 reference voltage is set to 0.8V, the output voltage is equal to VSET * 0.0125 + 0.8V. When the Buck2 reference voltage is set to 0.6V, the output voltage is equal to VSET*0.009375 + 0.6V. The reference voltage is set by register REF_SEL_B2.

B2_VSET01 – Buck2 Voltage Set1 Register

Address = 0x43h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1 [7:0]							
Default	00010000							
Access	R/W							

Name	Description	Notes
VSET1 [7:0]	Buck2 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck2 output voltage. B2_VSET1 is used in DVS or SLEEP modes. The output voltage setting is the same as the B2_VSET0 register.

B2_REG04 – Buck2 Configuration Register

Address = 0x44h	Default = 0xD0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DP_SLEEP_EN	ILIM_SET	RFU
Default	1	1	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Buck2 is enabled through normal sequencing 1 – Buck2 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Auxiliary Input cannot turn on / turn off regulator 1 – Auxiliary Input can be used to turn on / turn off regulator	An Auxiliary input could be a GPIO control input pin as an example.
DP_SLEEP_EN	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	
ILIM_SET	0 – Peak current limit set to 3.0A 1 – Peak current limit set to 2.0A	
RFU	Reserved for Future Use	Do not change this register bit. Changing the register bit may result in unexpected IC behavior.

B2_REG05 – Buck2 Configuration Register

Address = 0x45h	Default = 0x93h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	010			011		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck2 does not affect nRESET output 1 – Buck2 turning off asserts nRESET output low	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG06 – Buck2 Configuration Register

Address = 0x46h	Default = 0x09h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				ON_DELAY [1:0]		DBSTBY [1:0]	
Default	0000				10		01	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ON_DELAY [1:0]	00 = no delay 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms	Programs the delay time between the Buck2 input trigger and when it turns on.
DBSTBY [1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG07 – Buck2 Configuration Register

Address = 0x47h	Default = 0xC0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	DISLPM	OFF_DELAY [4:0]				
Default	0	1	0	00100				
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	
DISLPM	0 – Low Power Mode enabled 1 – Low Power Mode disabled	
OFF_DELAY [4:0]	Sets the delay time between the Buck2 disable input to when it turns off.	Buck2 turnoff delay time is equal to OFF_DELAY * 0.25ms

BUCK3 REGULATOR REGISTERS

B3_REG00 – Buck3 Configuration Register

Address = 0x50h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	0 – Buck3 voltage is below the power good threshold 1 – Buck3 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck3 voltage is above the overvoltage threshold 1 – Buck3 voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM	0 – Buck3 is below the ILIM threshold 1 – Buck3 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	0 – Buck3 is below the ILIM warning threshold 1 – Buck3 is above the ILIM warning threshold	Provides real-time current limit warning status
UV_FLTMSK	0 – Unmasks the Buck3 POK signal 1 – Masks the Buck3 POK signal	When 1, the Buck3 POK signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is disabled or drops out of regulation. B1_POK still provides real-time power good status.
OV_FLTMSK	0 – Unmasks the Buck3 OV register 1 – Masks the Buck3 OV register	When 1, the Buck3 OV signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. OV still provides real-time OV status.
ILIM_FLTMSK	0 – Unmasks the Buck3 B1_ILIM register 1 – Masks the Buck3 B1_ILIM register	When 1, the B1_ILIM fault bit is masked from the master fault register. ILIM still provides real-time current limit status.
ILIM_WARN_FLTMSK	0 – Unmasks the Buck3 ILIM_WARN register 1 – Masks the Buck3 ILIM_WARN register	When 1, the ILIM_WARN fault bit is masked from the master fault register. ILIM_WARN still provides real-time current limit warning status.

B3_REG01 – Buck3 Configuration Register

Address = 0x51h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	00000000							
Access	R/W							

Name	Description	Notes
RFU [7:0]	Reserved for future use	Do not change these bits

B3_VSET00 – Buck3 Voltage Set0 Register

Address = 0x52h	Default = 0x50h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0[7:0]							
Default	01010000							
Access	R/W							

Name	Description	Notes
VSET0[7:0]	Buck3 output voltage setting in ACTIVE mode.	Controls the Buck3 output voltage. VSET0 is used in ACTIVE mode. The output voltage is equal to VSET * 0.0125 + 0.8V

B3_VSET01 – Buck3 Voltage Set1 Register

Address = 0x53h	Default = 20xh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1[7:0]							
Default	0020000							
Access	R/W							

Name	Description	Notes
VSET1 [7:0]	Buck3 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck3 output voltage. VSET1 is used in DVS or SLEEP modes. The output voltage is equal to VSET * 0.0125 + 0.8V

B3_REG04 – Buck3 Configuration Register

Address = 0x54h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	DP_SLEEP_EN	ILIM_SET	RFU
Default	1	1	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Buck3 is enabled through normal sequencing 1 – Buck3 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
AUXIN_EN	0 – Auxiliary Input cannot turn on / turn off regulator 1 – Auxiliary Input can be used to turn on / turn off regulator	An Auxiliary input could be a GPIO control input pin as an example.
DP_SLEEP_EN	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	
ILIM_SET	0 – Peak current limit set to 3.0A 1 – Peak current limit set to 2.0A	
RFU	Reserved for Future Use	Do not change this register bit. Changing the register bit may result in unexpected IC behavior.

B3_REG05 – Buck3 Configuration Register

Address = 0x55h	Default = 0xA0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	1	000			100		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck3 does not affect nRESET output 1 – Buck3 turning off asserts nRESET output low	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG06 – Buck3 Configuration Register

Address = 0x56h	Default = 0x0Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				ON_DELAY [1:0]		DBSTBY [1:0]	
Default	0000				10		10	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ON_DELAY [1:0]	00 = no delay 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms	Programs the delay time between the Buck3 input trigger and when it turns on.
DBSTBY [1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG07 – Buck3 Configuration Register

Address = 0x57h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	DISLPM	OFF_DELAY [4:0]				
Default	0	0	0	00000				
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	
DISLPM	0 – Low Power Mode enabled 1 – Low Power Mode disabled	
OFF_DELAY [4:0]	Sets the delay time between the Buck3 disable input to when it turns off.	Buck3 turnoff delay time is equal to OFF_DELAY * 0.25ms

LDO REGISTERS

LDO12_REG00 – LDO1 Configuration Register

Address = 0xA0h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	RW	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO1	0 – LDO1 voltage is below the power good threshold 1 – LDO1 voltage is above the power good threshold	Provides real-time power good status
OV_LDO1	0 – LDO1 voltage is above the overvoltage threshold 1 – LDO1voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO1	0 – LDO1 is below the ILIM threshold 1 – LDO1 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this bit
UV_FLTMSK_LDO1	0 - Unmasks the LDO1 UV_LDO1 register 1 - Masks the LDO1 UV_LDO1 register	When 1, the UV_LDO1 fault bit is masked from the master UV fault register, MSTR06. UV_LDO1 still provides real-time current limit status.
OV_FLTMSK_LDO1	0 - Unmasks the LDO1 OV_LDO1 register 1 - Masks the LDO1 OV_LDO1 register	When 1, the OV_LDO1 fault bit is masked from the master OV fault register, MSTR05. OV_LDO1 still provides real-time overvoltage status.
ILIM_FLTMSK_LDO1	0 - Unmasks the LDO1 ILIM_LDO1 register 1 - Masks the LDO1 ILIM_LDO1 register	When 1, the ILIM_LDO1 fault bit is masked from the master ILIM fault register, MSTR04. ILIM_LDO1 still provides real-time current limit status.
RFU	Reserved for future use	Do not change this bit

LDO1_VSET – LDO1 Voltage Set0 Register

Address = 0xA1h	Default = 0x50h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_VSET [7:0]							
Default	01010000							
Access	R/W							

Name	Description	Notes
LDO1_VSET [7:0]	LDO1 output voltage setting.	Controls the LDO1 output voltage. The LDO reference voltage is set to 0.8V, the output voltage is equal to LDO1_VSET * 0.0125 + 0.8V When the LDO reference voltage is set to 0.6V, the output voltage is equal to LDO1_VSET*0.009375 + 0.6V. Note that the LDO reference voltage setting is not user controllable. The CMI 101 LDO reference voltage is set to 0.8V

LDO1_REG02 – LDO1 Configuration Register

Address = 0xA2h	Default = 0xC1h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_LDO1	PBINEN_LDO1	AUXIN_EN_LDO1	SLEEPEN_LDO1	DPSLEEP_EN_LDO1	DBQL_LDO1[2:0]		
Default	1	1	0	0	0	001		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_LDO1	0 – LDO1 is enabled through normal sequencing 1 – LDO1 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_LDO1	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
AUXIN_EN_LDO1	0 – Auxiliary Input cannot turn on / turn off regulator 1 – Auxiliary Input can be used to turn on / turn off regulator	An Auxiliary input could be a GPIO control input pin as an example. This bit is only available with the ACT88326 CMIs.
SLEEPEN_LDO1	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	
DPSLEEP_EN_LDO1	0 – LDO1 stays on when the IC enters Deep Sleep mode 1 – LDO1 turns off when the IC enters Deep Sleep mode	
DBQL_LDO1[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG03 – LDO1 Configuration Register

Address = 0xA3h	Default = 0x42h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF_DELAY_LDO1[4:0]					DBOK [2:0]		
Default	01000					0010		
Access	R/W					R/W		

Name	Description	Notes
OFF_DELAY_LDO1 [4:0]	Sets the delay time between the LDO1 disable input to when it turns off.	LDO1 turnoff delay time is equal to OFF_DELAY_LDO1 * 0.25ms
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG04 – LDO1 Configuration Register

Address = 0xA4h	Default = 0x0Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE_LDO1	RST_LDO1	ONDLY_LDO1[1:0]	
Default	0000				1	0	10	
Access	R/W						R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MODE_LDO1	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_LDO1	0 – LDO1 does not affect nRESET output 1 – LDO1 turning off asserts nRESET output low	
ONDLY_LDO1[1:0]	00 = no delay 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms	Programs the delay time between the LDO1 input trigger and when it turns on.

LDO12_REG05 – LDO1 Configuration Register

Address = 0xA5h	Default = n/a	Type = n/a

BIT	7	6	5	4	3	2	1	0
Name	n/a							
Default	n/a							
Access	R/W							

Name	Description	Notes
n/a	Reserved for factory use	Do not write to this register. Writing to this register may result in unexpected IC behavior

LDO12_REG06 – LDO1 Configuration Register

Address = 0xA6h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_ LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_ LDO2	OV_FLTMSK_ LDO2	ILIM_FLTMSK_ LDO2	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	RW	R/W	R/W	RO

Name	Description	Notes
PWR_GOOD_LDO2	0 – LDO2 voltage is below the power good threshold 1 – LDO2 voltage is above the power good threshold	Provides real-time power good status
OV_LDO2	0 – LDO2 voltage is above the overvoltage threshold 1 – LDO2voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO2	0 – LDO2 is below the ILIM threshold 1 – LDO2 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Do not change this bit
UV_FLTMSK_LDO2	0 - Unmasks the LDO2 UV_LDO2 register 1 - Masks the LDO2 UV_LDO2 register	When 1, the UV_LDO2 fault bit is masked from the master UV fault register, MSTR06. UV_LDO2 still provides real-time current limit status.
OV_FLTMSK_LDO2	0 - Unmasks the LDO2 OV_LDO2 register 1 - Masks the LDO2 OV_LDO2 register	When 1, the OV_LDO2 fault bit is masked from the master OV fault register, MSTR05. OV_LDO2 still provides real-time overvoltage status.
ILIM_FLTMSK_LDO2	0 - Unmasks the LDO2 ILIM_LDO2 register 1 - Masks the LDO2 ILIM_LDO2 register	When 1, the ILIM_LDO2 fault bit is masked from the master ILIM fault register, MSTR04. ILIM_LDO2 still provides real-time current limit status.
RFU	Reserved for future use	Do not change this bit

LDO12_VSET – LDO2 Voltage Set0 Register

Address = 0xA7h	Default = 0xFFh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO2_VSET [7:0]							
Default	11111111							
Access	R/W							

Name	Description	Notes
LDO2_VSET [7:0]	LDO2 output voltage setting.	Controls the LDO2 output voltage. When the LDO reference voltage is set to 0.8V, the output voltage is equal to LDO2_VSET * 0.0125 + 0.8V When the LDO reference voltage is set to 0.6V, the output voltage is equal to LDO2_VSET*0.009375 + 0.6V. Note that the LDO reference voltage setting is not user controllable. The CMI 101 LDO reference voltage is set to 0.8V

LDO12_REG02 – LDO2 Configuration Register

Address = 0xA8h	Default = 0xC0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON_LDO2	PBINEN_LDO2	AUXIN_EN_LDO2	SLEEPEN_LDO2	DPSLEEP_EN_LDO2	DBQL_LDO2[2:0]		
Default	1	1	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON_LDO2	0 – LDO2 is enabled through normal sequencing 1 – LDO2 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBINEN_LDO2	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
AUXIN_EN_LDO2	0 – Auxiliary Input cannot turn on / turn off regulator 1 – Auxiliary Input can be used to turn on / turn off regulator	An Auxiliary input could be a GPIO control input pin as an example.
SLEEPEN_LDO2	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	
DPSLEEP_EN_LDO2	0 – LDO2 stays on when the IC enters Deep Sleep mode 1 – LDO2 turns off when the IC enters Deep Sleep mode	
DBQL_LDO2[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG09 – LDO2 Configuration Register

Address = 0xA9h	Default = 0x31h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF_DELAY_LDO2[4:0]					DBOK [2:0]		
Default	00110					001		
Access	R/W					R/W		

Name	Description	Notes
OFF_DELAY_LDO2[4:0]	Sets the delay time between the LDO2 disable input to when it turns off.	LDO2 turnoff delay time is equal to OFF_DELAY_LDO2 * 0.25ms
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG0A – LDO2 Configuration Register

Address = 0xAAh	Default = 0x0Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE_LDO2	RST_LDO2	ONDLY_LDO2 [1:0]	
Default	0000				1	1	00	
Access	R/W						R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MODE_LDO2	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_LDO2	0 – LDO2 does not affect nRESET_AUX1 output 1 – LDO2 turning off asserts nRESET_AUX1 output low	
ONDLY_LDO2[1:0]	00 = no delay 01 = 0.25ms 10 = 0.5ms 11 = 1.0ms	Programs the delay time between the LDO2 input trigger and when it turns on.

LDO12_REGAC – LDO1 Configuration Register

Address = 0xACh	Default = 0x00h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VREF_CTRL	RFU					
Default	0	0	000000					
Access	RO	RO	RO					

Name	Description	Notes
RFU		Do not change these register values. Changing the register values can affect IC functionality.
VREF_CTRL	0 – LDO1 and LDO2 reference voltage = 0.8V 1 – LDO1 and LDO2 reference voltage = 0.6V	
RFU		Do not change these register values. Changing the register values can affect IC functionality.

LDO12_REG0D – LDO1 Configuration Register

Address = 0xADh	Default = 0x3Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	QLTCH_LDO2	QLTCH_LDO1	ILIM2[1:0]		ILIM1[1:0]		LDO2_ILIM_SHUTDOWN_DIS	LDO2_ILIM_SHUTDOWN_DIS
Default	0	0	11		11		1	1
Access	R/W	R/W	R/W		R/W		R/W	R/W

Name	Description	Notes
QLTCH_LDO2	0 – LDO2 shuts down when its sequenced input shuts down 1 – LDO2 stays on when its sequenced input shuts down	
QLTCH_LDO1	0 – LDO1 shuts down when its sequenced input shuts down 1 – LDO1 stays on when its sequenced input shuts down	
ILIM2[1:0]	00 = 190mA +/-30% 01 = 250mA +/-30% 10 = 330mA +/-30% 11 = 465mA +/-30%	LDO2 output current limit.
ILIM1[1:0]	00 = 190mA +/-30% 01 = 250mA +/-30% 10 = 330mA +/-30% 11 = 465mA +/-30%	LDO1 output current limit.
LDO2_ILIM_SHUTDOWN_DIS	0 – Shut down LDO2 after current limit 1 – Disable LDO2 Shut down function after current limit	LDO can shut down with current limit and restart after 14ms when this function is enabled.
LDO1_ILIM_SHUTDOWN_DIS	0 – Shut down LDO1 after current limit 1 – Disable LDO1 Shut down function after current limit	LDO can shut down with current limit and restart after 14ms when this function is enabled.

LOAD SWITCH REGISTERS

LSW12_REG00 – Load Switch Configuration Register

Address = 0xE5h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	LOAD SW1 PGOOD/UV	LOAD SW1 ILIM FLT	RFU	RFU	LOAD SW1 PGOOD FLTMSK	LOAD SW1 ILIM FLTMSK
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	RW	R/W	R/W	RO

Name	Description	Notes
RFU	Reserved for future use	Do not change these register values. Changing the register values can affect IC functionality.
RFU	Reserved for future use	Do not change these register values. Changing the register values can affect IC functionality.
LOAD SW1 PGOOD/UV	0 – LSW1 output voltage is below the power good threshold 1 – LSW1 output voltage is above the power good threshold	Provides real-time power good status
LOAD SW1 ILIM FLT	0 – Load Switch 1 is operating normally 1 – Load Switch 1 is in current limit	Provides real-time current limit status
RFU	Reserved for future use	Do not change these register values. Changing the register values can affect IC functionality.
RFU	Reserved for future use	Do not change these register values. Changing the register values can affect IC functionality.
LOAD SW1 PGOOD FLTMSK	0 - Unmasks the LOAD SW1 (LSW1) ILIM Interrupt 1 - Masks the LOAD SW1 (LSW1) ILIM Interrupt	When 1, the LOAD SW1 PGOOD/UV fault bit is masked from generating interrupts. LOAD SW1 PGOOD/UV still provides real-time current limit status.
LOAD SW1 ILIM FLTMSK	0 - Unmasks the LOAD SW1 ILIM FLT Interrupt 1 - Masks the LOAD SW1 ILIM FLT Interrupt	When 1, the LOAD SW1 ILIM FLT fault bit is masked from generating interrupts. LOAD SW1 ILIM FLT still provides real-time overvoltage status.

LSW12_REG01 – Load Switch12 Configuration Register

Address = 0xE6h	Default = 0x20h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BUCK1_BYP_ISS [1:0]		GATE1 SLEW [1:0]		RFU [1:0]		QLTCH1	RFU
Default	00		10		00		0	0
Access	R/W		R/W		R/W		R/W	R/W

Name	Description	Notes
BUCK1_BYP_ISS [1:0]	00 = 0.6A 01 = 1.0A 10 = 1.5A 11 = 2.0A	Buck1 bypass mode current limit setting. Only effective if BUCK1 is configured as a bypass switch or in bypass mode
GATE1 SLEW [1:0]	00 = 2.5 µA 01 = 5.0 µA 10 = 7.5 µA 11 = 10.0 µA	LSW GATE driver strength
RFU [1:0]	Reserved for future use	Do not change these bits
QLTCH1	0 – Load Switch 1 shuts down when its sequenced input shuts down 1 – Load Switch 1 stays on when its sequenced input shuts down	
RFU	Reserved for future use	Do not change this bit

LSW12_REG02 – Load Switch12 Configuration Register

Address = 0xE7h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LSW1	PBIN EN LSW1	AUXIN EN LSW1	SLEEP EN LSW1	DPSLEEP EN LSW1	DBQL LSW1[2:0]		
Default	0	1	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON LSW1	0 – LSW1 is enabled through normal sequencing 1 – LSW1 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN EN LSW1	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
AUXIN EN LSW1	0 – Load Switch 1 can be turned on /Off with Auxiliary input 1 – Load Switch 1 can be turned on /Off with Auxiliary input	Auxiliary input can be a GPIO input pin for example.
SLEEP EN LSW1	0 – LSW1 stays on when the IC enters Sleep mode 1 – LSW1 turns off when the IC enters Sleep mode	
DPSLEEP EN LSW1	0 – LSW1 stays on when the IC enters Deep Sleep mode 1 – LSW1 turns off when the IC enters Deep Sleep mode	
DBQL LSW1[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LSW12_REG03 – Load Switch12 Configuration Register

Address = 0xE8h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF_DELAY_LSW1 [5:0]					DBOK_LSW1[2:0]		
Default	00000					000		
Access	R/W					R/W		

Name	Description	Notes
OFF_DELAY_LSW1[5:0]	Sets the delay time between the LSW1 disable input to when it turns off.	LSW1 turnoff delay time is equal to OFF_DELAY_LSW1 * 0.25ms
DBOK_LSW1[2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LSW12_REG04 – Load Switch12 Configuration Register

Address = 0xE9h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON_LSW1 [3:0]				MODE_LSW1	RST_LSW1	ON_DELAY_LSW1 [1:0]	
Default	0000				1	0	00	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON_LSW1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MODE_LSW1	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST_LSW1	0 – LSW1 does not affect nRESET output 1 – LSW1 turning off asserts nRESET output low	
ON_DELAY_LSW1 [1:0]	0 – LSW1 shuts down when its sequenced input shuts down 1 – LSW1 stays on when its sequenced input shuts down	

LSW12_REG05 – Load Switch12 Configuration Register

Address = 0xEBh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU			LDO1_ADJ_ILIM	LDO2_ADJ_ILIM	EN_DVS_I2C	SEL_DVS_IN	I2C_DVS_ON
Default	000			0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
LDO1_ADJ_ILIM	0 – Normal LDO1 current limit 1 – LDO1 current limit increased by 12%	
LDO2_ADJ_ILIM	0 – Normal LDO2 current limit 1 – LDO2 current limit increased by 12%	
EN_DVS_I2C	0 – I2C DVS functionality is disabled. 1 – I2C DVS functionality is enabled.	
SEL_DVS_IN	0 – DVS is a function of the I2C_DVS_ON bit 1 – IC enters DVS when the IC enters SLEEP state	
I2C_DVS_ON	0 – Normal IC operation 1 – Puts IC into DVS mode	This bit is only valid when SEL_DVS_IN bit = 1

LSW12_REG06 – Load Switch12 Configuration Register

Address = 0xECh	Default = 0x1Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EXT_EN_DWN_AT_SLEEP_EN	EXT_EN_DWN_AT_DPSLEEP_EN	LDO1_LSW_MODE	LDO2_LSW_MODE	ILIM_BUCK3[0]	ILIM_BUCK1[0]	ILIM_BUCK2[0]	REF_SEL_BUCK2
Default	0	0	0	1	1	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
EXT_EN_DWN_AT_SLEEP_EN	0 – Normal operation 1 – Pulls GPIO2 low when IC enters SLEEP mode	
EXT_EN_DWN_AT_DPSLEEP_EN	0 – Normal operation 1 – Pulls GPIO2 low when IC enters DPSLEEP mode	
LDO1_LSW_MODE	0 – LDO1 operates as LDO 1 – LDO1 operates as a load switch	
LDO2_LSW_MODE	0 – LDO2 operates as LDO 1 – LDO2 operates as a load switch	
ILIM_BUCK3[0]	0 – 1 –	LSB for Buck3 current limit setting
ILIM_BUCK1[0]	0 – 1 –	LSB for Buck1 current limit setting
ILIM_BUCK2[0]	0 – 1 –	LSB for Buck2 current limit setting
REF_SEL_BUCK2	0 – Buck2 voltage reference = 0.6V 1 – Buck2 voltage reference = 0.8V	This bit should only be changed at the factory. Changing this bit during operation may result in unexpected IC operation.

References

The following data sheets can be used as references for details for electrical parameters and available configuration settings and values.

1. *ACT88325 Datasheet*
2. *ACT88326 Datasheet*