ACT85610 Register Definitions – CMI 101

Abstract

This paper identifies and explains the ACT85610 internal registers that help make this IC flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. This application note is specific to the Code Matrix Index, CMI 101.

Introduction

The ACT85610 device is a highly integrated, high configurable multiple output power management unit (PMIC) with built-in power loss protection (PLP) IC. There are four high efficiency Bucks that can supply 3 x 6A and 1 x 3A current with the output voltage as low as 0.6V. In addition, there is a 12V Boost regulator with and a fixed output VCC Buck to provide the IC's bias and gate drive power for IC itself and to supply power to the gate drivers in regulators for maximum efficiency.

The power loss protection provides backup storage power in the event of an input power failure. A built-in Boost converter provides high voltage energy storage to minimize storage capacitor size requirements. The built-in supplement Buck converter regulates the storage voltage to a fixed output voltage. It contains internal, back-to-back eFuse FETs to provide bi-directional input to output isolation. The IC also provides hot swap and inrush current control.

The ACT85610 features a programmable storage capacitor voltage to optimize the storage capacitor sizing and system run time. The internal ADC and health monitoring provide an extra layer of protection and improve system reliability and early capacitor failure notification. It automatically checks the storage capacitor health and notifies the user when the energy in the storage caps is not sufficient for backup power. The ADC also measures the input voltage, output voltage, storage voltage, eFuse current, and die temperature. The built-in synchronous supplement Buck converter maximizes energy transfer from the storage caps to the system.

The high voltage step-down regulators use a proprietary control architecture that is based on a constant on-time (COT) topology. It is designed for high efficiency, has programmable switching frequency options, is suitable for high conversion ratios to support output voltages as low as 0.6V and can therefore operate at very low duty cycles as required in low output voltage cases. It is therefore suitable for a variety of step-down applications.

The ACT85610 also has a Boost regulator. The input to the Boost regulator is typically in the range of 2.5V – 14V and the output voltage is configurable in the range of 10.8V – 13.2V in Boost mode.

The fixed output VCC Buck regulator is used as the power supply to the IC itself and to supply power to the gate drivers in the regulators, with 100mA max current capability for external circuits and LDO input.

The ACT85610 contains the following register types:

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

I2C REGISTER MAP

ADDR (HEX)	7	6	5	4	3	2	1	0
MASTER BASIC VOLATILE (I2C ADDR=0x4Ah)								
00	WD_TIMER_Expired	WD_TIMER_ALERT	THERMAL_WARN	VBUS_STAT	WD_PC_STAT	WD_SR_STAT	RFU	RFU
01	WD_TIMER_MASK	WD_ALERT_MASK	THERMAL_MASK	VBUS_MASK	WD_PC_STAT_MASK	WD_SR_STAT_MASK	MINIBUCK_OV_INT_MASK	MINIBUCK_OC_INT_MASK
02	RFU	RFU	RFU	RFU	RFU	RFU	OVER_TEMP_SHUTDOWN	VBUS_DAT
03	INTADR [7:0]							
04	POWER_UP_FLT	RFU	POWER_OFF	MR	RFU	WD_INT_EN	WD_PC_EN	WD_SR_EN
05	RFU							
06	RFU	GPIO7 STAT	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO1 STAT
07	RFU	GPIO7 Toggled	GPIO6 Toggled	GPIO5 Toggled	GPIO4 Toggled	GPIO3 Toggled	GPIO2 Toggled	GPIO1 Toggled
08	RFU	GPIO7 MASK	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
09	RFU							
0A	UNLOCK REGISTER KEY							
MASTER BASIC NON-VOLATILE (I2C ADDR=0x4Ah)								
0F	RESET DELAY [1:0]		DPSLP_EN	SLEEP_EN	IO Output Falling Delay DISABLE	VBUS_MON [2:0]		
10	EN_PullUp_IO1_Delay	EXT_IOD5 Output Delay	EXT_IOD4 Output Delay	EXT_IOD3 Output Delay EN	EXT_IOD2 Output Delay EN	EXT_IOD1 Output Delay EN	DIS UVOV FLT	ANA MODE EN
11	STR_nRST	GPIO7 Pullup Enable	GPIO6 Pullup Enable	GPIO5 Pullup Enable	GPIO4 Pullup Enable	GPIO3 Pullup Enable	GPIO2 Pullup Enable	GPIO1 Pullup Enable
12	RFU				RFU			
13	RFU				RFU			
14	RFU				RFU			
15	RFU				RFU			
16	RFU				RFU			
17	RFU				RFU			
18	RFU				RFU			
19	CMI REV ID [3:0]				EXT_PG_blank_time	RFU		
1A	Enter sleep	RFU	VINIO1_SEL	VINI2C_SEL	RFU	RFU	RFU	

ADDR (HEX)	7	6	5	4	3	2	1	0
PLP BASIC VOLATILE (I2C ADDR=0x4Ch)								
E0	CAP_VALUE<12:8>					CURRENT_STATE [2:0]		
E1	PVIN_OV	THERMAL_SHUTDOWN	THERMAL_PWRDWN	THERMAL_ALERT	VIN_FAULT	VIN_OV_2ND	EFUSE_NPG	EFUSE_VINLOSS
E2	EFUSE_ILIM_ALERT	EFUSE_OC_SHUTDOWN	MINIBUCK_UV	VIN_UV_2ND	STR_UV	STR_OV	STR_PG	BUCKIN_UV
E3	BUCK_ILIM__SHUTDOWN	BUCK_ILIM_ALERT	BUCK_NPG	BUCK_COMPFAIL	ADC_DRDY_IRQ	HCHK_NG	SPLMNT_MODE	BOOTCAPFAIL
E4	CAP_VALUE<7:0>							
E5	ADC_DOUT [13:6]							
E6	RFU	RFU	ADC_DOUT [5:0]					
E7	ADC_DATA_READY	ADC_VREF_SEL	ADC_VREF_BYPASS	ADC_CLK_HALF	RFU	ADC_CH_READ [2:0]		
E8	ADC_SWAP	EN_ADC	ADC_ONE_SHOT	ADC_CH_SCAN	EN_ADCBUF	ADC_CH_CONV [2:0]		
E9	MSTR_OK	RFU	RFU	RFU	RFU	RFU	PVIN_NUV	EFUSE_ISETLOW
EA	LDO_UV	LDO_OV	BFET_HIC_STATUS	FAIL_MEASURE	RFU	EN_STR10MASINK	FORCE_HLTCHK	FORCE_PWROFF
EB	RFU	RFU	RFU	RFU	RFU	EN_GPIO_DISCHARGE_ALL	DISCHARGE_ALL	EN_BFET

ADDR (HEX)	7	6	5	4	3	2	1	0
PLP BASIC NON-VOLATILE (I2C ADDR=0x4Ch)								
26	LDO_LV_UV_IRQ_MASK	LDO_LV_OV_IRQ_MASK	BFET_HIC_IRQ_MASK	MINIBUCK_ILIM2_MSK	PULL_DOWN_GPIO2_IF_NO_VCC	PLI_FUNC_SEL<1:0>		N_DIS_BOOST
27	PVIN_OV_IRQ_MASK	THML_SD_IRQ_MASK	THML_PD_IRQ_MASK	THML_ALERT_IRQ_MASK	VIN_FAULT_IRQ_MASK	EN_PIN_OV_IRQ_MASK	EFUSE_NPG_IRQ_MASK	EFUSE_VL_IRQ_MASK
28	EFUSE_ILIM_ALERT_IRQ_MASK	EFUSE_OC_SD_IRQ_MASK	MINIBUCK_UVLO_IRQ_MASK	ENPIN_UV_IRQ_MASK	STR_UV_IRQ_MASK	STR_OV_IRQ_MASK	STR_PG_IRQ_MASK	BUCKIN_UV_IRQ_MASK
29	BUCK_ILIM_SD_IRQ_MASK	BUCK_ILIM_ALERT_IRQ_MASK	BUCK_NPG_IRQ_MASK	BUCK_COMPFAIL_IRQ_MASK	ADC_DRDY_IRQ_MASK	HCHK_NG_IRQ_MASK	SPLMNT_IRQ_MASK	BOOTCAPFAIL_IRQ_MASK
2A	ADC_OUTRG_IRQ_MASK	GLOBAL_IRQ_MASK	DIS_HEALTH_CKH	EN_DIS_CHG_VBUS_STR	HMON_TSET<3:0>			
2B	GPIO2 TO ADC	GPIO1 TO ADC	AFF_EN	EN_STARTDELAY	HMON_THR<3:0>			
2C	EN_LATCH_SPLMNT	EN_OT155_TO_SPLMNT	LATCH_UVSTATE	EN_DEG_1MS	EFUSE_OC SETTING		MINIBUCK_VSET<1:0>	
2D	VIN_UV_2ND_PER<3:0>				EFUSE_ISET<3:0>			
2E	ADC_DOUT_OS<13:6>							
2F	BFET_ISS<1:0>	ADC_DOUT_GE<5:0>						
30	VIN_OV_2ND_PER<3:0>				RFU	RFU	RFU	RFU
31	STR_PG_CALL_NIRQ	DIS_ADC	RFU	RFU	SCALE_TSET_2X	SCALE_TSET_4X	SCALE_HCHK_2X	SCALE_HCHK_4X
32	PULL_DOWN_GPIO6_IF_NO_VCC	MASK_PVIN_OV	MES_POWER	MASK_BUCK_COMPFAIL	MASK_BOOT_CAP_FAIL	PULL_DOWN_GPIO5_IF_NO_VCC	PULL_DOWN_GPIO4_IF_NO_VCC	PULL_DOWN_GPIO1_IF_NO_VCC
33	MASK_BUCKIN_NUV	MASK_EFUSE_OC	MASK_EFUSE_VIN_LT_VO	MASK_MINIBUCK_FAULT	MASK_STR_OV	MASK_STR_UV	MASK_BUCK_OV	MASK_BUCK_UV
34	RFU			MINIBUCK_FORCE_OFF_BUCK_ON_LDO	MINIBUCK_5V_LDO	RST_LDO_LV	BFET_AUTO_TURN_ON_SEL	BFET_HIC_OPTION
35	MINIBUCK_DIS_DISCHG	RFU			RFU	PULL_DOWN_GPIO3_IF_NO_VCC	RFU	RFU
PLP BASIC NON-VOLATILE (I2C ADDR=0x4Ah)								
CA	BST_VSET<7:0>							
CB	MASK_SW_FAULT_BUCK	BK_VOUT_SET<6:0>						
CC	BUCK_HSILIM<2:0>			RFU	RFU	RFU	BUCK_VOUT_UVSET<1:0>	

ADDR (HEX)	7	6	5	4	3	2	1	0
PMIC BUCK1 BASIC VOLATILE (I2C ADDR=0x4Ah)								
40	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
41	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
PMIC BUCK1 BASIC NON-VOLATILE (I2C ADDR=0x4Ah)								
45	VSET0<7:0>							
46	VSET1<7:0>							
47	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
48	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
49	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
4A	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
4B	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
4C	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			

ADDR (HEX)	7	6	5	4	3	2	1	0
PMIC BUCK2 BASIC VOLATILE (I2C ADDR=0x4Ah)								
60	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
61	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
PMIC BUCK2 BASIC NON-VOLATILE (I2C ADDR=0x4Ah)								
65	VSET0<7:0>							
66	VSET1<7:0>							
67	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
68	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
69	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
6A	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
6B	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
6C	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			

ADDR (HEX)	7	6	5	4	3	2	1	0
PMIC BUCK3 BASIC VOLATILE (I2C ADDR=0x4Ah)								
80	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
81	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
PMIC BUCK3 BASIC NON-VOLATILE (I2C ADDR=0x4Ah)								
85	VSET0<7:0>							
86	VSET1<7:0>							
87	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
88	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
89	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
8A	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
8B	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
8C	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			

ADDR (HEX)	7	6	5	4	3	2	1	0
PMIC BUCK4 BASIC VOLATILE (I2C ADDR=0x4Ah)								
A0	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
A1	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
PMIC BUCK4 BASIC NON-VOLATILE (I2C ADDR=0x4Ah)								
A5	VSET0<7:0>							
A6	VSET1<7:0>							
A7	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
A8	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
A9	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
AA	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
AB	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
AC	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			

ADDR (HEX)	7	6	5	4	3	2	1	0
PMIC BOOST BASIC VOLATILE (I2C ADDR=0x4Ah)								
C0	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
C1	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
PMIC BOOST BASIC NON-VOLATILE (I2C ADDR=0x4Ah)								
C5	RFU	RFU	VSET0<5:0>					
C6	BST_DBON<3:0>				BST_ON	QLTCH	SLEEP EN	DP SLEEP EN
C7	RFU	RST	DBQL<2:0>			DBOK<2:0>		
C8	RFU	ON DELAY<2:0>			OFF DELAY<3:0>			
C9	ILIM_LDO<1:0>		VSET_LDO<5:0>					

MASTER BASIC VOLATILE

0x00h - MASTER1 – MASTER CONFIGURATION Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	WD_TIMER_Expired	WD_TIMER_ALERT	THERMAL_WARN	VBUS_STAT	WD_PC_STAT	SR_STAT	RFU	RFU
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
WD_TIMER_Expired	0 = Watchdog timer has not expired 1 = Watchdog timer has expired (8.2s)	When this bit = 1, an interrupt is generated on the nIRQ pin if WDINT_EN = 1 and WD_TIMER_MASK=0. This bit is latched and must be read via I2C to clear it back to 0
WD_TIMER_ALERT	0 = Watchdog timer alert has not expired 1 = Watchdog timer alert has expired (7.4s)	When this bit = 1, an interrupt is generated on the nIRQ pin if WDINT_EN = 1 and WD_ALERT_MASK = 0. This bit is latched and must be read via I2C to clear it back to 0
THERMAL_WARN	0 = Junction temperature < 125 deg C. 1 = Junction temperature > 125 deg C.	When this bit = 1, an interrupt is generated on the nIRQ pin if THERMAL_MASK = 0. This bit is cleared to 0 when die temperature < THERMAL_WARN falling threshold and this bit is read.
VBUS_STAT	0 = VBUS voltage is above the VBUS_MON threshold 1 = VBUS voltage is below the VBUS_MON threshold	When this bit = 1, an interrupt is generated on the nIRQ pin if VBUS_MASK = 0. When VBUS_STAT = 1, this bit is latched until the register contents are read via I2C. The VBUS_MON warning threshold is programmed with the VBUS_MON bits in the 0x0F [2:0] register bits. VBUS_MON monitors voltage at the VBUS pins.
WD_PC_STAT	0 = Power Cycle status is cleared 1 = Power Cycle has occurred.	Enable Watch Dog Power Cycle by setting register 0x04h bit 1 (WD_PC_EN) to 1. When a Watch Dog Power Cycle occurs, WD_PC_STAT is set to 1 and an interrupt is generated on the nIRQ pin if the PC_STAT_MASK = 0. Reading this register automatically clears this bit to a 0.
WD_SR_STAT	0 = Soft reset status is cleared 1 = Soft reset has occurred	Enable Watch Dog Soft Reset by setting register 0x04h bit 0 (WD_SR_EN) to 1. When a Watch Dog Soft Restet occurs, WD_SR_STAT is set to 1 and an interrupt is generated on the nIRQ pin if the SR_STAT_MASK = 0. Reading this register automatically clears this bit to a 0.
RFU	Reserved for future use	Always returns 0
RFU	Reserved for future use	Always returns 0

0x01h - MASTER2 – MASTER CONFIGURATION Register

Address = 0x01h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	WD_TIMER_MASK	WD_ALERT_MASK	THERMAL_MASK	VBUS_MASK	WD_PC_STAT_MASK	WD_SR_STAT_MASK	MINIBUCK_OV_INT_MASK	MINIBUCK_OC_INT_MASK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
WD_TIMER_MASK	0 = unmasks the watch dog timer interrupt 1 = masks the watch dog timer interrupt	When this bit =1, the WD TIMER interrupt is masked but WD_TIMER_Expired bit still provides the status
WD_ALERT_MASK	0 = unmasks the watch dog alert interrupt 1 = masks the watch dog alert interrupt	When this bit = 1, the WD_ALERT interrupt is masked but WD_TIMER_ALERT still provides watchdog status.
THERMAL_MASK	0 = unmasks the thermal warning interrupt 1 = masks the thermal warning interrupt	When this bit = 1, the THERMAL_WARN interrupt is masked but THERMAL_WARN still provides temperature warning status.
VBUS_MASK	0 = unmasks the VBUS_STAT interrupt 1 = masks the VBUS_STAT interrupt	When this bit = 1, the VBUS_STAT interrupt is masked but VBUS_STAT still provides UV warn status.
WD_PC_STAT_MASK	0 = unmasks the WD_PC_STAT interrupt 1 = masks the WD_PC_STAT interrupt	When this bit = 1, the WD_PC_STAT interrupt is masked but WD_PC_STAT still provides status.
WD_SR_STAT_MASK	0 = unmasks the WD_SR_STAT interrupt 1 = masks the WD_SR_STAT interrupt	When this bit = 1, the WD_SR_STAT interrupt is masked but WD_SR_STAT still provides status.
MINIBUCK_OV_INT_MASK	0 = unmasks the miniBUCK over voltage interrupt 1 = masks the miniBUCK over voltage interrupt	When this bit = 1, the MINIBUCK_OV_INT interrupt is masked but MINIBUCK_OV_STAT still provides status.
MINIBUCK_OC_INT_MASK	0 = unmasks the miniBUCK over current interrupt 1 = masks the miniBUCK over current interrupt	When this bit=1, the MINIBUCK_OC interrupt is masked but MINIBUCK_OC_STAT still provides status.

0x02h - MASTER3 – MASTER CONFIGURATION Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	DVS_FROM_I2C_DB			RFU	RFU	RFU	OVER_TEMP_SHUTDOWN	VBUS_DAT
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	RO	RO	RO	RO

Name	Description	Notes
DVS_FROM_I2C_DB		EN_DVS_BY_I2C=1, these bits can be used to activate I2C. The specific setting to active I2C is CMI dependent, so contact the factory for the details on each specific CMI.
RFU	Reserved for future use	Always returns 0
RFU	Reserved for future use	Always returns 0
RFU	Reserved for future use	Always returns 0
OVER_TEMP_SHUTDOWN	0 = not in thermal shutdown 1 = in thermal shutdown	Real time status bit for thermal shutdown
VBUS_DAT	0 = VBUS voltage is below UV warning threshold 1 = VBUS voltage is above UV warning threshold	Real time status bit for VBUS_MON threshold set in register 0x0Fh

0x03h – INTERRUPT– INTERRUPT TILE ADDRESS Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INTADR [7:0]							
Default	0							
Access	RO							

Name	Description	Notes
RFU	Provides the hex address of the function that generated the interrupt on nIRQ	MSTR Interrupt Addr, 0x01h GPIO Interrupt Addr, 0x02h Buck1 Interrupt Addr, 0x41h Buck2 Interrupt Addr, 0x61h Buck3 Interrupt Addr, 0x81h Buck4 Interrupt Addr, 0xA1h BuckBoost Interrupt Addr, 0xC1h

0x04h – MASTER4 – MASTER CONFIGURATION Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POWER_UP_FLT	RFU	POWER_OFF	MR	RFU	WD_INT_EN	WD_PC_EN	WD_SR_EN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
POWER_UP_FLT	0: Normal, can write to 0 as condition to power start sequence. 1: Fault retry (100ms) occurred 7 times -> assert flag and move to RESET state.	Power up fault status/flag. User can write a 0 to clear the fault bit. It is not possible to write a 1 into this bit.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
POWER_OFF	0: Normal 1: Moves the IC into the RESET state and turns off all Regulators. This bit must be changed back to 0 to restart a power on sequence.	
MR	0: Normal. 1: Writing 1 to this bit power cycles all PMU bucks, clears all VM registers, moves IC to RESET state, then restarts the PMU after 0.5s. This is the hard-reset function for PMU bucks.	Hard reset or Manual reset only shuts down the buck converters. It does not affect the LDO or Boost
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
WD_INT_EN	0 = Disables interrupt when the watchdog timer expires 1 = Enables interrupt when the watchdog timer expires	
WD_PC_EN	0 = Disables power cycling when the watchdog timer expires 1 = Enables power cycling when the watchdog timer expires	It's used to turn on /off Buck1/2/3/4 when watchdog time expires. VCC,LDO,Boost not power cycle.
WD_SR_EN	0 = Disables soft reset when the watchdog timer expires 1 = Enables soft reset when the watchdog timer expires	When a watch dog soft reset occurs, WD_SR_STAT is triggered. nRESET is also triggered then released. nRESET goes low to tell the external MCU to check the fault registers to find the fault.

0x05h - RFU

Address = 0x05h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU				ILED6<3:0>			
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ILED6<3:0>	Config current setting for GPIO6 in case LED driver.	

0x06h – GPIO1 – GPIO STATUS Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO1 STAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
GPIO6 STAT	GPIO 6 real time status	When a GPIO is configured as input, user can use this bit to monitor status of GPIO. When = ”1” the input voltage is a logic H. When = ”0” the input voltage is logic L.
GPIO5 STAT	GPIO 5 real time status	
GPIO4 STAT	GPIO 4 real time status	
GPIO3 STAT	GPIO 3 real time status	
GPIO2 STAT	GPIO 2 real time status	
GPIO1 STAT	GPIO 1 real time status	

0x07h – GPIO2 – GPIO TOGGLED STATUS Register

Address = 0x07h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	GPIO6 Toggled	GPIO5 Toggled	GPIO4 Toggled	GPIO3 Toggled	GPIO2 Toggled	GPIO1 Toggled
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
GPIO6 Toggled	GPIOx toggle detected. Bit set to 1 when GPIOx toggle L to H or H to L. Bit set to 0 means there is no toggle.	When a GPIO is configured as input, user can use this bit to monitor status of GPIO toggle. These bits are latched and must be read via I2C to clear them back to 0
GPIO5 Toggled		
GPIO4 Toggled		
GPIO3 Toggled		
GPIO2 Toggled		
GPIO1 Toggled		

0x08h – GPIO3 – GPIO MASK Register

Address = 0x08h	Default = 0x7Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
Default	N/A	N/A	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
GPIO6 MASK	GPIOx generates the interrupt signal individually when GPIOx config as input. If the MASK bit is asserted, no interrupt is generated when toggle event happens.	
GPIO5 MASK		
GPIO4 MASK		
GPIO3 MASK		
GPIO2 MASK		
GPIO1 MASK		

0x09h - RFU

Address = 0x09h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	00000000							
Access	R/W							

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x0Ah – PASSCODE – GPIO MASK Register

Address = 0x0Ah	Default = 0xAAh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	UNLOCK REGISTER KEY							
Default	10101010							
Access	R/W							

Name	Description	Notes
UNLOCK REGISTER KEY	The IC implements a special register passcode that enables I^2C write transactions. This prevents accidental register changes. Enable I^2C write functionality by writing a value of 0xAAh to register 0x0Ah (Unlock Register Key). Change this register to any other value to prevent accidental changes to the I^2C register values.	

MASTER BASIC NON-VOLATILE

0x0Fh - MASTER1 – MASTER CONFIGURATION Register

Address = 0x0Fh	Default = 0x30h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RESET DELAY [1:0]		DPSLP_EN	SLEEP_EN	IO Output Falling Delay DISABLE	VBUS_MON [2:0]		
Default	0	0	1	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RESET DELAY [1:0]	Reset Timer Setting: 00=20ms 01=40ms 10=60ms 11=100ms	For PMU
DPSLP_EN	DPSLP mode enable 1: Enables DPSLP 0: Disables DPSLP	
SLEEP_EN	SLEEP mode enable 1: Enables SLEEP 0: Disables SLEEP	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
VBUS_MON [2:0]	000 = 3.0V 001 = 3.2V 010 = 3.4V 011 = 3.6V 100 = 3.8V 101 = 4.0V 110 = 8.0V 111 = 9.0V	PMIC VBUS pin voltage monitor setting bits.

0x10h – GPIO – GPIO CONFIGURATION Register

Address = 0x10h	Default = 0x04h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_PullUp_IO1_Delay	GPIO5_Output DelayEn	GPIO4_Output DelayEn	GPIO3_Output DelayEn	GPIO2_Output DelayEn	GPIO1_Output DelayEn	DIS UVOV FLT	ANA MODE EN
Default	0	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
EN_PullUp_IO1_Delay	0: no delay (after NVM load done) 1: Delay 2ms.	Enable delay pull up for GPIO1
GPIO5_OutputDelayEn GPIO4_OutputDelayEn GPIO3_OutputDelayEn GPIO2_OutputDelayEn GPIO1_OutputDelayEn	0: no delay (after NVM load done) 1: enable delay.	Enable delay for GPIOx config at Output mode (both edge default. Note that the delay time is set by bits EXT_DLY_GPIOx[1:0]. These bits are not customer configurable.
DIS UVOV FLT	0: normal 1: Disables OV_UV shutdown for the Bucks and LDOs.	
ANA MODE EN	0: GPIO analog mode is disabled 1: GPIO analog mode is enabled	Analog mode makes GPIO the input to an internal comparator with a 0.8V reference.

0x11h – GPIO5 – GPIO PULLUP CONFIGURATION Register

Address = 0x11h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	STR_nRST	GPIO7 Pullup Enable	GPIO6 Pullup Enable	GPIO5 Pullup Enable	GPIO4 Pullup Enable	GPIO3 Pullup Enable	GPIO2 Pullup Enable	GPIO1 Pullup Enable
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
STR_nRST	0: STR_UV will not affect nRESET status 1: STR_UV (95%@Rising/90%@Falling) will control nRESET pin	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
GPIO6 Pullup Enable		When this bit = 1, GPIOx will be pulled up to an internal 1.8V rail through a 200k resistor.
GPIO5 Pullup Enable		
GPIO4 Pullup Enable		
GPIO3 Pullup Enable		
GPIO2 Pullup Enable		
GPIO1 Pullup Enable		

0x12h - RFU

Address = 0x12h	Default = 0x07h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	0	0	0	0	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x13h - RFU

Address = 0x13h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x14h - RFU

Address = 0x14h	Default = 0x2Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	0	0	1	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x15h - RFU

Address = 0x15h	Default = 0x0Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	0	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x16h - RFU

Address = 0x16h	Default = 0x01h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x17h - RFU

Address = 0x17h	Default = 0x6Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	0	1	1	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x18h - RFU

Address = 0x18h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU							
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x19h – MASTER4 – MASTER CONFIGURATION Register

Address = 0x19h	Default = 0x13h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	CMI REV ID [3:0]				EXT_PG_blank_time	RFU		
Default	0	0	0	1	0	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
CMI REV ID [3:0]	CMI version number	
EXT_PG_blank_time	External PG blank time 0: 40 ms 1: 20 ms	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x1Ah – MASTER5 – MASTER CONFIGURATION Register

Address = 0x1Ah	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Enter sleep	RFU	VINIO1_SEL	VINI2C_SEL	RFU	RFU	RFU	
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
Enter sleep	0: Normal mode 1: Enables SLEEP mode	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
VINIO1_SEL	Select Vsupply for GPIO1: 0: VIO 1: VCC5	
VINI2C_SEL	Select Vsupply for SCL/SDA: 0: VIO 1: VCC5	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

PLP BASIC VOLATILE

0xE0h - STATUS0 – Status Register

Address = 0xE0h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	CAP_VALUE[12:8]					CURRENT_STATE[2:0]		
Default	00000					000		
Access	RO					RO		

Name	Description	Notes
CAP_VALUE[12:8]	5 MSB of STR cap value.	STR cap will be measurement each time IC enter Health check mode.
CURRENT_STATE[2:0]	000 = UV/POR 001 = SOFTSTART 010 = NORMAL 011 = HEALTH CHECK 100 = SUPPLEMENT 101 = SHUTDOWN1 110 = SHUTDOWN2 111 = NA	Shows the current state of the state machine.

0xE1h - STATUS1 - Status Register

Address = 0xE1h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PVIN_OV	THERMAL_ SHUTDOWN	THERMAL_ PWRDWN	THERMAL_ ALERT	VIN_FAULT	VIN_OV_ 2nd	eFUSE_ nPG	eFUSE_VI NLOSS
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
PVIN_OV	0 = VIN < OVLO 14.4V 1 = VIN > OVLO 14.4V	When this bit = 1, nIRQ goes low if VIN_OV_IRQ_Mask(0x27h bit 7) is not masked. It stays high until VIN < POK_OV and it is read.
THERMAL_SHUTDOWN	0 = Junction temperature < 155 deg C. 1 = Junction temperature > 155 deg C.	When this bit = 1,nIRQ goes low if THML_SD_IRQ_Mask((0x27h bit 6) is not masked. It stays high until die temperature < THERMAL_SHUTDOWN falling threshold and it is read.
THERMAL_PWRDWN	0 = Junction temperature < 145 deg C. 1 = Junction temperature < 145 deg C.	When this bit = 1,nIRQ goes low if THML_PD_IRQ_Mask((0x27h bit 5) is not masked. It stays high until die temperature < THERMAL_PWRDWN falling threshold and it is read.
THERMAL_ALERT	0 = Junction temperature < 125 deg C. 1 = Junction temperature > 125 deg C.	When this bit = 1,nIRQ goes low if THML_ALERT_IRQ_Mask((0x27h bit 4) is not masked. It stays high until die temperature < THERMAL_ALERT falling threshold and it is read.
VIN_FAULT	0 = no fault condition 1 = fault condition exists	VIN_FAULT is the logical OR of VIN_UV_2nd, VIN_OV_2nd, and PVIN_OV. When this bit = 1, nIRQ goes low if VIN_FAULT_IRQ_Mask((0x27h bit 3) is not masked. This bit stays high until all faults are cleared and it is read.
VIN_OV_2nd	0 = EN is < OV_REF 1 = EN is > OV_REF	Used to check for VIN OV. VIN_OV_2nd threshold can be programed by SEL<1:0> andVIN_OV_2nd_PER<3:0> When this bit = 1, nIRQ goes low if EN_PIN_OV_IRQ_Mask((0x27h bit 2) is not masked. This bit stays high until the fault is cleared and it is read.
eFUSE_nPG	0 = VIN - VOUT < 200mV 1 = VIN - VOUT > 560mV	When this bit = 1 (drop in output voltage), nIRQ goes low if eF_nPG_IRQ_Mask (0x27h bit 1) is not masked. This bit stays high until the fault is cleared and it is read.
eFUSE_VINLOSS	0 = VOUT - VIN < -390mV 1 = VOUT - VIN > 120mV	When this bit = 1 (drop in input voltage), nIRQ goes low if eF_VL_IRQ_Mask (0x27h bit 0) is not masked. This bit stays high until the fault is cleared and it is read.

0xE2h - STATUS2 - Status Register

Address = 0xE2h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	eFUSE_ILIM_ALERT	eFUSE_OC_SHUTDOWN	MINIBUCK_UV	VIN_UV_2nd	STR_UV	STR_OV	STR_PG	BUCKIN_UV
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
eFUSE_ILIM_ALERT	0 = ISET < 0.88*ILIM_SET 1 = ISET > 0.9* ILIM_SET	When this bit = 1, nIRQ goes low if eF_ILIM_Alert_IRQ_Mask(0x28h bit 7) is not masked. This bit stays high until the fault is cleared and it is read.
eFUSE_OC_SHUTDOWN	0 = eFuse current is below shutdown level 1 = eFuse current is above shutdown level	When this bit = 1, nIRQ goes low if eFUSE_OC_SD_IRQ_Mask(0x28h bit 6) is not masked. This bit stays high until the fault is cleared and it is read.
MINIBUCK_UV	0 = VCC voltage is lower than nUVLO threshold 1 = VCC voltage is higher than nUVLO threshold	When this bit = 1, nIRQ goes low if mBK_UVLO_IRQ_Mask(0x28h bit 5) is not masked. This bit stays high until the fault is cleared and it is read.
VIN_UV_2nd	0 = VIN higher than programed UV threshold 1 = VIN lower than programed UV threshold	When this bit = 1, nIRQ goes low if ENPIN_UV_IRQ_Mask(0x28h bit 4) is not masked. VIN_UV_2nd threshold can be programed by VIN_UV_SEL<1:0> and VIN_UV_2nd_PER<3:0>. Note that VIN_UV_SEL<1:0> can only be changed at the factory. This bit stays high until the fault is cleared and it is read.
STR_UV	0 = STR voltage is > programmed under voltage limit 1 = STR voltage is < programmed under voltage limit	When this bit = 1, nIRQ goes low if STR_UV_IRQ_Mask((0x28h bit 3) is not masked. STR_UV = 95% rising, 90% falling This bit stays high until the fault is cleared and it is read.
STR_OV	0 = STR voltage is < programmed over voltage limit 1 = STR voltage is > programmed over voltage limit	When this bit = 1, nIRQ goes low if STR_OV_IRQ_Mask((0x28h bit 2) is not masked. STR_OV = 110% rising, 107% falling This bit stays high until the fault is cleared and it is read.
STR_PG	0 = STR voltage is < STR_PG 1 = STR voltage is > STR_PG	When this bit = 1, nIRQ goes low if STR_PG_IRQ_Mask((0x28h bit 1) is not masked. In NORMAL or HCHK: real status of STR_PG In other state: force to 0 This bit stays high until STR voltage < STR_PG and it is read.
BUCKIN_UV	0 = STR > BUCKIN_UV threshold 1 = STR < BUCKIN_UV threshold at supplement state	When this bit = 1 (drop in input voltage), goes to UV/POR state, nIRQ goes low if BKIN_UV_IRQ_Mask((0x28h bit 0) is not masked. BUCKIN_UV = 3.08V rising, 2.78V falling This bit stays high until the fault is cleared and it is read.

0xE3h - STATUS3 - Status Register

Address = 0xE3h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	BUCK_ILIM_SHUTDOWN	BUCK_ILIM_ALERT	BUCK_nPG	BUCK_COMPFAIL	ADC_DRDY_IRQ	HCHK_NG	SPLMNT_MODE	BOOTCAPFAIL
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
BUCK_ILIM_SHUTDOWN	0 = PLP Buck is below the ILIM2 threshold 1 = PLP Buck is above the ILIM2 threshold	When this bit = 1, goes to UV/POR state. nIRQ goes low if BK_ILIM_SD_IRQ_Mask((0x29h bit 7) is not masked. This bit stays high until the fault is cleared and it is read.
BUCK_ILIM_ALERT	0 = PLP Buck is below the ILIM1 threshold 1 = PLP Buck is above the ILIM1 threshold	When this bit = 1, nIRQ goes low if BK_ILIM_Alert_IRQ_Mask((0x29h bit 6) is not masked. This bit stays high until the fault is cleared and it is read.
BUCK_nPG	0 = PLP Buck output is above the UV threshold 1 = PLP Buck output is below the UV threshold	When this bit = 1, goes to UV/POR state, nIRQ goes low if BK_nPG_IRQ_Mask((0x29h bit 5) is not masked. This bit stays high until the fault is cleared and it is read.
BUCK_COMPFAIL	0 = External impedance on COMP pin is ok 1 = COMP pin is shorted	When this bit = 1, nIRQ goes low if BK_CompFail_IRQ_Mask(0x29h bit 4) is not masked. This bit stays high until the fault is cleared and it is read.
ADC_DRDY_IRQ	0 = ADC has not finished conversion 1 = ADC has finished one shot conversion	When this bit = 1, nIRQ goes low if ADC_DRDY_IRQ_Mask(0x29h bit 3) is not masked.This bit is latched until read. This bit stays high until the fault is cleared and it is read.
HCHK_NG	0 = No error at Health check 1 = Error at Health check	When this bit = 1, nIRQ goes low if HCHCK_NG_IRQ_Mask(0x29h bit 2) is not masked. This bit stays high until the fault is cleared and it is read.
SPLMNT_MODE	0 = IC not in supplement mode 1 = IC is in supplement mode	When this bit = 1, nIRQ goes low if SPLMNT_IRQ_Mask(0x29h bit 1) is not masked. This bit is latched until read. Real status of supplement mode This bit stays high until the IC goes out of supplement and it is read.
BOOTCAPFAIL	0 = HSB voltage is ready for switching 1 = HSB voltage is not ready for switching	When this bit = 1, nIRQ goes low if BootCapFail_IRQ_Mask(0x29h bit 4) is not masked. This bit stays high until the fault is cleared and it is read.

0xE4h - Capacitance – Capacitance Read Register

Address = 0xE4h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	CAP_VALUE[7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
CAP_VALUE[12:8]	8 LSB of STR cap value.	

0xE5h - ADC1 – ADC Read Register

Address = 0xE5h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_DOUT[13:6]							
Default	0x00h							
Access	RO							

Name	Description	Notes
ADC_DOUT[13:6]	Contains the most significant eight bits for the result of an ADC read.	The register contains an 8-bit unsigned binary integer.

0xE6h - ADC2 – ADC Read Register

Address = 0xE6h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[1:0]		ADC_DOUT[5:0]					
Default	00		000000					
Access	RO		RO					

Name	Description	Notes
RFU[1:0]	Reserved for future use	Always returns 00
ADC_DOUT[5:0]	Contains the least significant six bits for the result of an ADC read.	The register contains a 6-bit unsigned binary integer.

0xE7h - ADC3 – ADC Configuration Register

Address = 0xE7h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_DATA_READY	ADC_VREF_SEL	ADC_VREF_BYPASS	ADC_CLK_HALF	RFU	ADC_CH_READ[2:0]		
Default	0	0	0	0	0	0		
Access	RO	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ADC_DATA_READY	0 = ADC data is not ready to read 1 = ADC conversion is finished. Data is ready to read	Automatically cleared when ADC data is read from register 0x05h and 0x06h
ADC_VREF_SEL	N/A	Do not change this register value. Changing this value will result in unexpected IC behavior.
ADC_VREF_BYPASS	N/A	Do not change this register value. Changing this value will result in unexpected IC behavior.
ADC_CLK_HALF	0 = ADC operates at normal frequency 1 = ADC operates at half frequency	
RFU	Reserved for future use	Always returns 0
ADC_CH_READ[2:0]	000 = reads input current 001 = reads VIN voltage 010 = reads STR voltage 011 = reads VBUS voltage 100 = reads die temperature 101 = reads VOUT_B1 voltage 110 = reads GPIO1 ADC input voltage 111 = reads GPIO2 ADC input voltage	Selects the desired ADC output to be read. Connects the ADC output to register ADC1 0xE5h and 0xE6h.

0xE8h - ADC4 – ADC Configuration Register

Address = 0xE8h	Default = 0x10h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_SWAP	EN_ADC	ADC_ONE_SHOT	ADC_CH_SCAN	EN_ADCBUF	ADC_CH_CONV[2:0]		
Default	0	0	0	1	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ADC_SWAP	0 = ADC inputs have normal polarity 1 = Swaps ADC positive and negative inputs	
EN_ADC	0 = ADC disabled 1 = ADC enabled	In one-time conversion mode, EN_ADC resets to 0 after each ADC conversion. Changing back to 1 initiates another ADC conversion.
ADC_ONE_SHOT	0 = ADC continually converts data when EN_ADC=1 1 = ADC performs a one-time conversion when EN_ADC=1	
ADC_CH_SCAN	0 = Scan single channel specified by ADC_CH_CONV 1 = Scan all channels	
EN_ADCBUF	0 = Disable ADC buffer 1 = Enable ADC buffer	
ADC_CH_CONV[2:0]	000 = Connects ADC input to the Input Current channel 001 = Connects ADC input to VIN channel 010 = Connects ADC input to STR channel 011 = Connects ADC input to the VOUT channel 100 = Connects ADC input to the temperature sensor 101 = Connects ADC input to the VOUT_B1 channel 110 = Connects ADC input to the GPIO1 channel 111 = Connects ADC input to the GPIO2 channel	In ADC one shot mode (ADC_ONE_SHOT = 1) this register connects the ADC input to the input signal to be converted. 101: VOUT_B1 (1/3 ratio) 110 : GPIO1 voltage (ratio=1) 111: GPIO2 voltage (ratio=1)

0xE9h - STATUS4 - Status Register

Address = 0xE9h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	MSTR_OK	RFU[4:0]					PVIN_nUV	eFUSE_ISETLOW
Default	0	00000					0	0
Access	RO	RO					RO	RO

Name	Description	Notes
MSTR_OK	0 = Internal references are not ready 1 = Internal references are ready	This bit stays high until master is not OK and it is read.
RFU[4:0]	Reserved for future use	Always returns a 00000
PVIN_nUV	0 = VIN is above UVLO threshold 1 = VIN is below UVLO threshold	PVIN_nUV=2.55V falling, hys 50mV. When VIN<PVIN_nUV, the IC totally turn-off. This bit stays high until the fault is cleared and it is read.
eFUSE_ISETLOW	0 = eFUSE current is > 12.5% ISET 1 = eFUSE current is > 10% ISET	This bit stays high until the fault is cleared and it is read.

0xEAh - CONTROL1 - Control Register

Address = 0xEAh	Default = 0x10h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO_UV	LDO_OV	BFET_HIC_STATUS	FAIL_MEASURE	RFU	EN_STR10mASINK	FORCE_HLTHCHK	FORCE_PWROFF
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	R/W	R/W	R/W

Name	Description	Notes
LDO_UV	0 = Vout_LDO is higher than POK threshold 1 = Vout LDO is lower than POK threshold or LDO is off	LDO_UV=1 can call nIRQ if not mask. This bit stays high until the fault is cleared and it is read.
LDO_OV	0 = Vout_LDO is lower than OV threshold or LDO is off 1 = Vout LDO is higher than OV threshold	LDO_OV=1 can call nIRQ if not mask This bit stays high until the fault is cleared and it is read..
BFET_HIC_STATUS	0 = BFET has not enter HICCUP state 1 = BFET has enter HICCUP state	BFET_HIC=1 can call nIRQ if not mask This bit stays high until BFET exit HICCUP and it is read.
FAIL_MEASURE	0: Pass capacitance measurement 1: Fail capacitance measurement.	Returns a 1 if the capacitance measurement cannot be completed before the 5s timer times out. It also returns a 1 if the measurement finishes but the result is all 1s. This bit stays high until the fault is cleared and it is read.
RFU	Reserved for future use	Always returns 0
EN_STR10mASINK	0 = Normal operation 1 = Enable 10mA storage cap discharge current	
FORCE_HLTHCHK	0 = Normal operation 1 = Forces a one-shot health check cycle	Forces health check even if EN_HCHK=0. This bit automatically resets to 0 after the health check is completed.
FORCE_PWROFF	0 = Normal operation 1 = Forces IC into the UV/POR state	

0xEBh - CONTROL2 - Control Register

Address = 0xEBh	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU[4:0]					EN_GPIO_DISCHARGE_ALL	DISCHARGE_ALL	EN_BFET
Default	00000					0	0	0
Access	RO					R/W	R/W	R/W

Name	Description	Notes
RFU[4:0]	Reserved for future use	Always returns 00000
EN_GPIO_DISCHARGE_ALL	Set this bit to 1 to enable the GPIO to put IC to turn off sequence.	
DISCHARGE_ALL	Set this bit to 1 put IC to turn off sequence. STR cap, VBUS cap will be discharge by 50mA pull down current. The bit will be reset to 0 if VINT lower than POR threshold or STR & VBUS discharge done.	
EN_BFET	0 = Turns blocking FET (BFET) off 1 = Turns blocking FET (BFET) on	This bit is only enabled when the NBFET_AUTO_TURN_ON_SEL bit in register 0x34h = 1.

PLP BASIC NON-VOLATILE

0x26h - MASK1 – Masking Register

Address = 0x26h	Default = 0xA9h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO_LV_UV_IRQ_MASK	LDO_LV_OV_IRQ_MASK	BFET_HIC_IRQ_MASK	MINIBUCK_ILIM2_MSK	Pull_down_GPIO2_if_no_VCC	PLI_FUNC_SEL<1:0>		n_DIS_BOOST
Default	1	0	1	0	1	00		1
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W

Name	Description	Notes
LDO_LV_UV_IRQ_MASK	0 – unmasks the LDO_UV register 1 – masks the LDO_UV register	When 1, LDO_UV register will not assert nIRQ. LDO_UV register still provides a status
LDO_LV_OV_IRQ_MASK	0 – unmasks the LDO_OV register 1 – masks the LDO_OV register	When 1, LDO_OV register will not assert nIRQ. LDO_OV register still provides a status
BFET_HIC_IRQ_MASK	0 – unmasks the BFET_HIC register 1 – masks the BFET_HIC register	When 1, BFET_HIC register will not assert nIRQ. BFET_HIC register still provides a status
MINIBUCK_ILIM2_MSK	0 – unmasks the ILIM2 of mini Buck 1 – masks the ILIM2 of mini Buck	
Pull_down_GPIO2_if_no_VCC	0 – not allow pull down 1 – allow pull down GPIO2 by 2kOhm res if VCC< VCC_nUVLO	
PLI_FUNC_SEL[1:0]	00 = PLI function enabled 01 = PG_STR function enabled 10 = VOUT_READY function enabled 11 = PLI & VOUT_READY function enabled	
nDIS_BOOST	0 = Boost and health checking are disabled 1 = Boost and health checking are enabled by state machine	

0x27h - MASK2 – Masking Register

Address = 0x27h	Default = 0x09h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PVIN_OV_IRQ_MASK	THML_SD_IRQ_MASK	THML_PD_IRQ_MASK	THML_ALERT_IRQ_MASK	VIN_FAULT_IRQ_MASK	ENPIN_OV_IRQ_MASK	eFUSE_nPG_IRQ_MASK	eFUSE_VL_IRQ_MASK
Default	0	0	0	0	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PVIN_OV_IRQ_MASK	0 – unmasks the PVIN_OV register 1 – masks the PVIN_OV register	When 1, PVIN_OV register will not assert nIRQ. PVIN_OV register still provides a status
THML_SD_IRQ_MASK	0 – unmasks the THERMAL_SHUTDOWN register 1 – masks the THERMAL_SHUTDOWN register	When 1, THERMAL_SHUTDOWN register will not assert nIRQ. THERMAL_SHUTDOWN register still provides a status
THML_PD_IRQ_MASK	0 – unmasks the THERMAL_PWRDOWN register 1 – masks the THERMAL_PWRDOWN register	When 1, THERMAL_PWRDOWN register will not assert nIRQ. THERMAL_PWRDOWN register still provides a status
THML_ALERT_IRQ_MASK	0 – unmasks the THERMAL_ALERT register 1 – masks the THERMAL_ALERT register	When 1, THERMAL_ALERT register will not assert nIRQ. THERMAL_ALERT register still provides a status
VIN_FAULT_IRQ_MASK	0 – unmasks the VIN_FAULT register 1 – masks the VIN_FAULT register	When 1, VIN_FAULT register will not assert nIRQ. VIN_FAULT register still provides a status
ENPIN_OV_IRQ_MASK	0 – unmasks the ENPIN_OV register 1 – masks the ENPIN_OV register	When 1, ENPIN_OV register will not assert nIRQ. ENPIN_OV register still provides a status
eFUSE_nPG_IRQ_MASK	0 – unmasks the eFUSE_nPG register 1 – masks the eFUSE_nPG register	When 1, eFUSE_nPG register will not assert nIRQ. eFUSE_nPG register still provides a status
eFUSE_VL_IRQ_MASK	0 – unmasks the eFUSE_VINLOSS register 1 – masks the eFUSE_VINLOSS register	When 1, eFUSE_VINLOSS register will not assert nIRQ. eFUSE_VINLOSS register still provides a status

0x28h - MASK3 – Masking Register

Address = 0x28h	Default = 0x3Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	eFUSE_ILIM_ALERT_IRQ_MASK	eFUSE_OC_SD_IRQ_MASK	MINIBUCK_UVLO_IRQ_MASK	ENPIN_UV_IRQ_MASK	STR_UV_IRQ_MASK	STR_OV_IRQ_MASK	STR_PG_IRQ_MASK	BUCKIN_UV_IRQ_MASK
Default	0	0	1	1	1	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
eFUSE_ILIM_ALERT_IRQ_MASK	0 – unmasks the eFUSE_ILIM_ALERT register 1 – masks the eFUSE_ILIM_ALERT register	When 1, eFUSE_ILIM_ALERT register will not assert nIRQ. eFUSE_ILIM_ALERT register still provides a status
eFUSE_OC_SD_IRQ_MASK	0 – unmasks the eFUSE_OC_SHUTDOWN register 1 – masks the eFUSE_OC_SHUTDOWN register	When 1, eFUSE_OC_SHUTDOWN register will not assert nIRQ. eFUSE_OC_SHUTDOWN register still provides a status
MINIBUCK_UV_IRQ_MASK	0 – unmasks the miniBK_UV register 1 – masks the miniBK_UV register	When 1, miniBK_UV register will not assert nIRQ. miniBK_UV register still provides a status
ENPIN_UV_IRQ_MASK	0 – unmasks the VIN_UV_2nd register 1 – masks the VIN_UV_2nd register	When 1, VIN_UV_2nd register will not assert nIRQ. VIN_UV_2nd register still provides a status
STR_UV_IRQ_MASK	0 – unmasks the STR_UV register 1 – masks the STR_UV register	When 1, STR_UV register will not assert nIRQ. STR_UV register still provides a status
STR_OV_IRQ_MASK	0 – unmasks the STR_OV register 1 – masks the STR_OV register	When 1, STR_OV register will not assert nIRQ. STR_OV register still provides a status
STR_PG_IRQ_MASK	0 – unmasks the STR_PG register 1 – masks the STR_PG register	When 1, STR_PG register will not assert nIRQ. STR_PG register still provides a status
BUCKIN_UV_IRQ_MASK	0 – unmasks the BUCKIN_UV register 1 – masks the BUCKIN_UV register	When 1, BUCKIN_UV register will not assert nIRQ. BUCKIN_UV register still provides a status

0x29h - MASK4 – Masking Register

Address = 0x29h	Default = 0x22h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BUCK_ILIM_SD_IRQ_MASK	BUCK_ILIM_ALERT_IRQ_MASK	BUCK_nPG_IRQ_MASK	BUCK_COMPFAIL_IRQ_MASK	ADC_DRDY_IRQ_MASK	HCHK_NG_IRQ_MASK	SPLMNT_IRQ_MASK	BOOTCAPFAIL_IRQ_MASK
Default	0	0	1	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
BUCK_ILIM_SD_IRQ_MASK	0 – unmasks the BUCK_ILIM_SHUTDOWN register 1 – masks the BUCK_ILIM_SHUTDOWN register	When 1, BUCK_ILIM_SHUTDOWN register will not assert nIRQ. BUCK_ILIM_SHUTDOWN register still provides a status
BUCK_ILIM_ALERT_IRQ_MASK	0 – unmasks the BUCK_ILIM_ALERT register 1 – masks the BUCK_ILIM_ALERT register	When 1, BUCK_ILIM_ALERT register will not assert nIRQ. BUCK_ILIM_ALERT register still provides a status
BUCK_nPG_IRQ_MASK	0 – unmasks the BUCK_nPG register 1 – masks the BUCK_nPG register	When 1, BUCK_nPG register will not assert nIRQ. BUCK_nPG register still provides a status
BUCK_COMPFAIL_IRQ_MASK	0 – unmasks the BUCK_ COMPFAIL register 1 – masks the BUCK_ COMPFAIL register	When 1, BUCK_ COMPFAIL register will not assert nIRQ. BUCK_ COMPFAIL register still provides a status
ADC_DRDY_IRQ_MASK	0 – unmasks the ADC_DRDY_IRQ register 1 – masks the ADC_DRDY_IRQ register	When 1, ADC_DRDY_IRQ register will not assert nIRQ. ADC_DRDY_IRQ register still provides a status
HCHK_NG_IRQ_MASK	0 – unmasks the HCHK_NG register 1 – masks the HCHK_NG register	When 1, HCHK_NG register will not assert nIRQ. HCHK_NG register still provides a status
SPLMNT_IRQ_MASK	0 – unmasks the SPLMNT_MODE register 1 – masks the SPLMNT_MODE register	When 1, SPLMNT_MODE register will not assert nIRQ. SPLMNT_MODE register still provides a status
BOOTCAPFAIL_IRQ_MASK	0 – unmasks the BOOTCAPFAIL register 1 – masks the BOOTCAPFAIL register	When 1, BOOTCAPFAIL register will not assert nIRQ. BOOTCAPFAIL register still provides a status

0x2Ah - MASK5 – Masking Register

Address = 0x2Ah	Default = 0x14h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OUTRNG_IRQ_MASK	GLOBAL_IRQ_MASK	DIS_HEALTH_CHK	EN_DIS_CHG_VBUS_STR	HMON_TSET[3:0]			
Default	0	0	0	1	0100			
Access	R/W	R/W	R/W	RO	R/W			

Name	Description	Notes
ADC_OUTRNG_IRQ_MASK	0 – unmasks all ADC_OUTRNGE_CHx registers 1 – masks all ADC_OUTRNGE_CHx registers	When 1, ADC_OUTRNGE_CHx registers will not assert nIRQ. ADC_OUTRNGE_CHx registers still provide a real-time status
GLOBAL_IRQ_MASK	0 – unmasks inputs to the nIRQ pin 1 – All IRQs are masked	When 1, nIRQ is forced to be deasserted, regardless of any operating condition.
DIS_HEALTH_CHK	0 – Health check is enabled 1 – Health check is disabled	When disabled, one-shot Health Check can still be run by writing 1 into FORCE_HCHK.
EN_DIS_CHG_VBUS_STR	0 = Normal operation 1 = Enable discharge VBUS and STR	
HMON_TSET[3:0]	0000 = 2ms 0001 = 4ms 0010 = 8ms 0011 = 16ms 0100 = 32ms 0101 = 64ms 0110 = 128ms 0111 = 256ms 1000 = 512ms 1001 = 768ms 1010 = 1024ms 1011 = 1280ms 1100 = 1536ms 1101 = 1792ms 1110 = 2048ms 1111 = 2304ms	Sets the Health Check current discharge time.

0x2Bh - CONTROL3 - Control Register

Address = 0x2Bh	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	GPIO2 to ADC	GPIO1 to ADC	AFF_EN	EN_STARTDELAY	HMON_THR[3:0]			
Default	0	0	0	0	1111			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
GPIO2 to ADC	1 = Pass GPIO2 directly to ADC	
GPIO1 to ADC	1 = Pass GPIO1 directly to ADC	
AFF_EN	0 = Not enable anti-alias filter for ADC 1 = Enable anti-alias filter for ADC	
EN_STARTDELAY	0 = Sets eFuse delay to 0ms 1 = Sets eFuse delay to 125ms	Delay time from VIN going above UV threshold to when the eFuse starts turning on
HMON_THR[3:0]	0000 = 90.5% 0001 = 91.0% 0010 = 91.5% 0011 = 92.0% 0100 = 92.5% 0101 = 93.0% 0110 = 93.5% 0111 = 94.0% 1000 = 94.5% 1001 = 95.0% 1010 = 95.5% 1011 = 96.0% 1100 = 96.5% 1101 = 97.0% 1110 = 97.5% 1111 = 98.0%	Health Check voltage threshold.

0x2Ch - CONTROL4 - Control Register

Address = 0x2Ch	Default = 0x81h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_LATCH_SPLMNT	EN_OT155_TO_SPLMNT	LATCH_UVSTATE	EN_DEG_1ms	eFUSE_OC setting <1:0>		MINIBUCK_VSET<1:0>	
Default	1	0	0	0	00		01	
Access	R/W	R/W	R/W	R/W	R/W		R/W	

Name	Description	Notes
EN_LATCH_SPLMNT	0 = If the IC is in supplement mode, this setting allows the IC to exit supplement mode before fully discharging the storage capacitors. 1 = Forces IC to stay in supplement mode until the STR voltage drops below BKIN_UV or VOUT drops below BUCK PG threshold	
EN_OT155_TO_SPLMNT	0 = IC does not enter supplement mode when the IC temperature goes above 155 deg C. 1 = IC does enter supplement mode when the temperature goes above 155 deg C.	
LATCH_UVSTATE	0 = After supplement mode is completed, the IC goes back to the Soft Start state when Vin rises above the UV threshold. 1 = After supplement mode is completed, the IC is latched off. The IC requires an input voltage transition from below VIN_UV to above VIN_UV before it restarts.	
EN_DEG_1ms	0: Set falling delay of VIN_UV_2nd & VIN_OV_2nd to 125us 1: Set falling delay of VIN_UV_2nd & VIN_OV_2nd to 1ms	
eFUSE_OC setting <1:0>	Fast eFuse OC protection thresholds: 00: 6.5A 01: 10.5A 10: 14.5A 11: 18.5A	
MINIBUCK_VSET<1:0>	VCC voltage setting: 00 = 4.9V 01 = 5.0V 10 = 5.1V 11 = 5.2V	

0x2Dh - CONTROL5 - Control Register

Address = 0x2Dh	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	VIN_UV_2nd_PER<3:0>				EFUSE_ISET<3:0>			
Default	0000				0010			
Access	R/W				R/W			

Name	Description	Notes
VIN_UV_2nd_PER<3:0>	0000 = 80% 0001 = 81% 0010 = 82% 0011 = 83% 0100 = 84% 0101 = 85% 0110 = 86% 0111 = 87% 1000 = 88% 1001 = 89% 1010 = 90% 1011 = 91% 1100 = 92% 1101 = 93% 1110 = 94% 1111 = 95%	The VIN_SEL_UV and VIN_UV_2nd_PER registers set the ICs undervoltage threshold. The undervoltage threshold, VIN_UV, is equal to the VIN_SEL_UV voltage times the VIN_UV_2nd_PER register value. For example, if VIN_SEL_UV = 11 and VIN_UV_2nd_PER= 0000, the VIN_UV threshold = 12V*80% = 9.6V. Note that VIN_SEL_UV can only be changed at the factory.
EFUSE_ISET<3:0>	0000 = 1.5A 0001 = 2A 0010 = 3A 0011 = 4A 0100 = 5A 0101 = 6A 0110 = 7A 0111 = 8A 1000 = 9A 1001 = 10A 1010 = 11A 1011 = 12A 1100 = 12A 1101 = 12A 1110 = 12A 1111 = 12A	eFUSE ILIM setting

0x2Eh - ADC_OFFSET – ADC Offset Register

Address = 0x2Eh	Default = N/A	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ADC_OS[13:6]							
Default	N/A							
Access	RO							

Name	Description	Notes
ADC_OS[13:6]	ADC TRIM BIT	Do not write to this register. Changing this register affects ADC read accuracy

0x2Fh - ADC_GAIN – ADC Gain Register

Address = 0x2Fh	Default = N/A	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BFET_ISS<1:0>		ADC_GE[5:0]					
Default	01		N/A					
Access	R/W		R/W					

Name	Description	Notes
BFET_ISS<1:0>	00 = 147mA 01 = 212mA 10 = 305mA 11 = 483mA	Set the soft start current limit for BFET to charge storage cap.
ADC_GE[5:0]	ADC TRIM BIT	Do not write to this register. Changing this register affects ADC read accuracy

0x30h – CONTROL6 - Control Register

Address = 0x30h	Default = 0x4Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VIN_OV_2nd_PER<3:0>				RFU	RFU	RFU	RFU
Default	0100				1	1	1	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
VIN_OV_2nd_PER<3:0>	0000 = Disabled 0001 = 106% 0010 = 107% 0011 = 108% 0100 = 109% 0101 = 110% 0110 = 111% 0111 = 112% 1000 = 113% 1001 = 114% 1010 = 115% 1011 = 116% 1100 = 117% 1101 = 118% 1110 = 119% 1111 = 120%	The VIN_SEL and VIN_OV_2nd_PER registers set the ICs overvoltage threshold. The overvoltage threshold, VIN_OV, is equal to the VIN_SEL voltage times the VIN_OV_2nd_PER register value. For example, if VIN_SEL = 11 and VIN_1V_2nd_PER= 1111, the VIN_OV threshold = 12V*120% = 14.4V Note that setting VIN_OV_2nd_PER = 0000 disables VIN_OV Note that VIN_SEL_OV can only be changed at the factory.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x31h – CONTROL7 - Control Register

Address = 0x31h	Default = 0x20h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	STR_PG_call_nIRQ	DIS_ADC	RFU	RFU	SCALE_TSET_2X	SCALE_TSET_4X	SCALE_HCHK_2X	SCALE_HCHK_4X
Default	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
STR_PG_call_nIRQ	1 = nIRQ stays low when STR_PG=0	
DIS_ADC	1 = Disable ADC function	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
SCALE_TSET_2X	0 – Normal HMON_TSET 1 – HMON_TSET timing slowed by 2x	
SCALE_TSET_4X	0 – Normal HMON_TSET 1 – HMON_TSET timing slowed by 4x	
SCALE_HCHK_2X	0 – Health check performed every 4 minutes 1 – Health check performed every 8 minutes	
SCALE_HCHK_4X	0 – Health check performed every 4 minutes 1 – Health check performed every 16 minutes	

0x32h – CONTROL8 - Control Register

Address = 0x32h	Default = 0xA3h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Pull_down_GPIO6_if_no_VCC	mask_pvin_ov	MES_POWER	Mask_BUCK_COMPFAIL	mask_boot_cap_fail	Pull_down_GPIO5_if_no_VCC	Pull_down_GPIO4_if_no_VCC	Pull_down_GPIO1_if_no_VCC
Default	1	0	1	0	0	0	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
Pull_down_GPIO6_if_no_VCC	1 = allow pull down GPIO6 by 2kOhm res if VCC< VCC_nUVLO	
MASK_PVIN_OV	0 – Normal operation 1 = No state transition by PVIN_OV	
MES_POWER	1 = when measure Input power	
Mask_BUCK_COMPFAIL	0 – Normal operation 1 = No state transition by BUCK_COMPFAIL	
mask_boot_cap_fail	0 – Normal operation 1 = No state transition by BOOTCAPFAIL	
Pull_down_GPIO5_if_no_VCC	1: allow pull down GPIO5 by 2kOhm res if VCC< VCC_nUVLO	
Pull_down_GPIO4_if_no_VCC	1: allow pull down GPIO4 by 2kOhm res if VCC< VCC_nUVLO	
Pull_down_GPIO1_if_no_VCC	1: allow pull down GPIO1 by 2kOhm res if VCC< VCC_nUVLO	

0x33h - State_Machine – State Machine Register

Address = 0x33h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Mask_BUCKIN_nUV	Mask_eFUSE_OC	Mask_eFUSE_VIN_LT_VO	Mask_NINIBUCK_FAULT	Mask_STR_OV	Mask_STR_UV	Mask_BUCK_OV	Mask_BUCK_UV
Default	0	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
Mask_BUCKIN_nUV	0 – Normal operation 1 = No state transition by BUCKIN_nUV	
Mask_eFUSE_OC	0 – Normal operation 1 = No state transition by eFUSE_OC	
Mask_eFUSE_VIN_LT_VO	0 – Normal operation 1 = No state transition by eFUSE_VINLOSS=1	
Mask_mininBK_FAULT	0 – Normal operation 1 = No state transition by VCC_nUVLO =0	
Mask_STR_OV	0 – Normal operation 1 = No state transition by STR_OV = 1	
Mask_STR_UV	0 – Normal operation 1 = No state transition by STR_UV=1	
Mask_BUCK_OV	0 – Normal operation 1 = No state transition by BUCK_OV=1	
Mask_BUCK_UV	0 – Normal operation 1 = No state transition by BUCK_UV=1	

0x34h - MiniBuck 1 – MiniBuck Control Register

Address = 0x34h	Default = 0x01h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU			Force_Off_mBK	MINIBUCK_5V_LDO	RST_LDO	NBFET_AUTO_TURN_ON_SEL	BFET_HIC_OPTION
Default	0			0	0	0	0	1
Access	RO			R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
Force_Off_mBK	0 = Normal operation 1 = Turn off buck but still keep LDO_VCC to generate VCC	
mBK_5V_LDO	0 = set LDO_VCC=4.5V 1 = set LDO_VCC=5V	
RST_LDO	0 = Normal operation 1 = LDO pull nRESET if not OK	
NBFET_AUTO_TURN_ON_SEL	0= The BFET automatically turns on. With this setting, the BFET cannot be manually turned off. 1= The BFET can be turned on and off with the EN_BFET bit	
BFET_HIC_OPTION	0 = BFET retry permanent 1= allow BFET hiccup up 1 time if not success then move IC to shutdown1 Boost" state	

0x35h - MiniBuck 2 – MiniBuck Control Register

Address = 0x35h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	mBK_DIS_DISCHG	RFU			RFU	Pull_down_GPIO3_if_no_VCC	RFU	RFU
Default	1	000			0	0	0	0
Access	R/W	RO			R/W	R/W	R/W	R/W

Name	Description	Notes
mBK_DIS_DISCHG	0 = Allow the miniBUCK discharge function 1 = Disable discharge VCC when entire miniBUCK turn off	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
Pull_down_GPIO3_if_no_VCC	1: allow pull down GPIO3 by 2kOhm res if VCC< VCC_nUVLO	
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0xCAh - PLP BOOST – PLP Boost Configuration Register

Address = 0xCAh	Default = 0xE1h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BST_VSET [7:0]							
Default	11100001							
Access	R/W							

Name	Description	Notes
BST_VSET [7:0]	00000000 = 5.5V 11111111 = 31V 100mV steps	VSTR=5.5+0.1* BST_VSET<7:0>

0xCBh - SPL Buck1 – Buck Configuration Register

Address = 0xCBh	Default = 0x92h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MASK_SW_FAULT_BUCK	BK_VOUT_SET<6:0>						
Default	1	0010011						
Access	R/W	R/W						

Name	Description	Notes
MASK_SW_FAULT_BUCK	1 = Mask SW_FAULT for PLP_BUCK	
BK_VOUT_SET<6:0>	0000000 = 2.5V 1111111 = 12V 100mV steps	Vbus_reg=2.5+BK_VOUT_SET<6:0>*0.1

0xCCh - SPL Buck2 – Buck Configuration Register

Address = 0xCCh	Default = 0x6Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BUCK_HSILIM<2:0>			RFU	RFU	RFU	BUCK_VOUT_UVSET<1:0>	
Default	011			0	1	1	01	
Access	R/W			R/W	R/W	R/W	R/W	

Name	Description	Notes
BUCK_HSILIM<2:0>	000 = 3A 001 = 4A 010 = 5A 011 = 6A 100 = 7A 101 = 8A 110 = 9A 111 = 10A	High side FET ILIM of the BUCK
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
BUCK_VOUT_UVSET<1:0>	00: 60% 01: 70% 10: RFU 11: RFU	select VBUS UV threshold:

PMIC BUCK1 BASIC VOLATILE

0x40h - B1_REG01 – PMIC BUCK1 Configuration Register

Address = 0x40h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV (110%/107%) 0: VOUT < VOUT OV	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdown is triggered 0: Output Ilim Shutdown is not triggered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is triggered 0: Output Ilim Fault is not triggered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is triggered 0: Output Ilim Warning is not triggered	If the peak switch current reaches the 78% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 78% of ILIMSET and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x41h - B1_REG02 – PMIC BUCK1 Configuration Register

Address = 0x41h	Default = 0xDCh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
Default	1	1	N/A	0	1	1	N/A	N/A
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MASK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck1 POK signal does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is disabled or drops out of regulation. B1_POK still provides real-time power good status.
OV_INT_MASK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck1 OV signal does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ISHUT_INT_MASK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck1 ILIM shutdown signal does not go to the master controller. . ILIM_SHUT still provides current limit status.
IFLT_INT_MASK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck1 ILIM fault signal does not go to the master controller. ILIM_FLT still provides current limit status.
IWARN_INT_MASK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck1 ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

PMIC BUCK1 BASIC NON-VOLATILE

0x45h - B1_REG03 – PMIC BUCK1 Configuration Register

Address = 0x45h	Default = 0x2Bh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0 [7:0]							
Default	00101000							
Access	R/W							

Name	Description	Notes
VSET0 [7:0]	Buck1 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0<7:0>

0x46h - B1_REG04 – PMIC BUCK1 Configuration Register

Address = 0x46h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1 [7:0]							
Default	00011110							
Access	R/W							

Name	Description	Notes
VSET1 [7:0]	Buck1 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1<7:0>

0x47h - B1_REG05 – PMIC BUCK1 Configuration Register

Address = 0x47h	Default = 0x0Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	1	0	0
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON<3:0>	Determines startup sequencing from the CMI code	Do not change this
ON	0 – Buck1 is enabled through normal sequencing 1 – Buck1 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	

0x48h - B1_REG06 – PMIC BUCK1 Configuration Register

Address = 0x48h	Default = 0x0Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
Default	0	0	001			010		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
RST	0 – Buck1 does not affect nRESET output 1 – Buck1 turning off asserts nRESET output low	
DBQL<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0x49h - B1_REG07 – PMIC BUCK1 Configuration Register

Address = 0x49h	Default = 0xB2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
Default	1	011			0010			
Access	R/W	R/W			R/W			

Name	Description		Notes
HSON_DL	Adjust the delay of high side FET turn-on 0: 0ns 1: 3ns		
ON DELAY<2:0>	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms	100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck1 input trigger and when it turns on.
OFF DELAY<3:0>	Sets the delay time between the Buck1 disable input to when it turns off.		Buck1 turnoff delay time is equal to OFF_DELAY * 1ms

0x4Ah - B1_REG08 – PMIC BUCK1 Configuration Register

Address = 0x4Ah	Default = 0x41h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
Default	01		0	0	0	0	01	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM<1:0>	00: IPEAK=5A, IVALLEY=5A 01: IPEAK=6A, IVALLEY=6.1A 10: IPEAK=7A, IVALLEY=6.8A 11: IPEAK=8A, IVALLEY=7.5A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck1 will shutdown if VIN_Buck1 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck1 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck1 will shutdown if Buck1_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck1_OUT occurs UV/OV.	
DB_DVS<1:0>	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0x4Bh - B1_REG09 – PMIC BUCK1 Configuration Register

Address = 0x4Bh	Default = 0xDCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
Default	1	1	0	1	1	1	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
POK_OPT	Option POK thresholds 0: Rising/Falling(87/84 % of VOUT) 1: Rising/Falling(90/87 % of VOUT)	
HSD_SLEW	0: Slow 1: High	
LSD_SLEW<1:0>	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0x4Ch - B1_REG10 – PMIC BUCK1 Configuration Register

Address = 0x4Ch	Default = 0x12h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			
Default	0	0	0	1	0010			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DISPLDN	0: VOUT discharge at turn off 1: VOUT not discharge at turn off	
PD_OPTION	0: Rdis = 6Ohm 1: Rdis = 20Ohm	Set the discharge resistance
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_RANGE_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> - 1.875V
FREQ<3:0>	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

PMIC BUCK2 BASIC VOLATILE

0x60h - B2_REG01 – PMIC BUCK2 Configuration Register

Address = 0x60h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV(110%/107%) 0: VOUT is Normal	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdown is triggered 0: Output Ilim Shutdown is not triggered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is triggered 0: Output Ilim Fault is not trigered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is triggered 0: Output Ilim Warning is not triggered	If the peak switch current reaches the 78% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 78% of ILIMSET and it is read.
RFU		
RFU		

0x61h - B2_REG02 – PMIC BUCK2 Configuration Register

Address = 0x61h	Default = 0xDCh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
Default	1	1	N/A	1	1	1	N/A	N/A
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MASK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck2 POK signal does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is disabled or drops out of regulation. B2_POK still provides real-time power good status.
OV_INT_MASK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck2 OV signal does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ISHUT_INT_MASK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck2 ILIM shutdown signal does not go to the master controller.. ILIM_SHUT still provides current limit status.
IFLT_INT_MASK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck2 ILIM fault signal does not go to the master controller ILIM_FLT still provides current limit status.
IWARN_INT_MASK		When 1, the Buck2 ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

PMIC BUCK2 BASIC NON-VOLATILE

0x65h - B2_REG03 – PMIC BUCK2 Configuration Register

Address = 0x65h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0 [7:0]							
Default	00011110							
Access	R/W							

Name	Description	Notes
VSET0 [7:0]	Buck2 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0<7:0>

0x66h - B2_REG04 – PMIC BUCK2 Configuration Register

Address = 0x66h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1 [7:0]							
Default	00011110							
Access	R/W							

Name	Description	Notes
VSET1 [7:0]	Buck2 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1<7:0>

0x67h - B2_REG05 – PMIC BUCK2 Configuration Register

Address = 0x67h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	1	1	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON<3:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
ON	0 – Buck2 is enabled through normal sequencing 1 – Buck2 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	

0x68h - B2_REG06 – PMIC BUCK2 Configuration Register

Address = 0x68h	Default = 0x1Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
Default	0	0	011			110		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
RST	0 – Buck2 does not affect nRESET output 1 – Buck2 turning off asserts nRESET output low	
DBQL<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0x69h - B2_REG07 – PMIC BUCK2 Configuration Register

Address = 0x69h	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
Default	1	100			0010			
Access	R/W	R/W			R/W			

Name	Description		Notes
HSON_DL	Adjust the delay of high side FET turn-on 0: 0ns 1: 3ns		
ON DELAY<2:0>	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms	100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck2 input trigger and when it turns on.
OFF DELAY<3:0>	Sets the delay time between the Buck2 disable input to when it turns off.		Buck2 turnoff delay time is equal to OFF_DELAY * 1ms

0x6Ah - B2_REG08 – PMIC BUCK2 Configuration Register

Address = 0x6Ah	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
Default	01		0	0	0	0	00	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM<1:0>	00: IPEAK=5A, IVALLEY=5A 01: IPEAK=6A, IVALLEY=6.1A 10: IPEAK=7A, IVALLEY=6.8A 11: IPEAK=8A, IVALLEY=7.5A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck2 will shutdown if VIN_Buck2 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck2 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck2 will shutdown if Buck2_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck2_OUT occurs UV/OV.	
DB_DVS<1:0>	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0x6Bh - B2_REG09 – PMIC BUCK2 Configuration Register

Address = 0x6Bh	Default = 0xDCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
Default	1	1	0	1	1	1	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
POK_OPT	Option POK thresholds 0: Rising/Falling(87/84 % of OUT) 1: Rising/Falling(90/87 % of OUT)	
HSD_SLEW	0: Slow 1: High	
LSD_SLEW<1:0>	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0x6Ch - B2_REG10 – PMIC BUCK2 Configuration Register

Address = 0x6Ch	Default = 0x04h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			
Default	0	0	0	0	0100			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DISPLDN	0: VOUT discharge at turn off 1: VOUT not discharge at turn off	
PD_OPTION	0: Rdis = 6Ohm 1: Rdis = 20Ohm	Set the discharge resistance
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_RANGE_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> 1.875V
FREQ<3:0>	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

PMIC BUCK3 BASIC VOLATILE

0x80h - B3_REG01 – PMIC BUCK3 Configuration Register

Address = 0x80h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK Status. 1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV(110%/107%) 0: VOUT is Normal	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdownis trigered 0: Output Ilim Shutdown is not trigered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is trigered 0: Output Ilim Fault is not trigered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is trigered 0: Output Ilim Warning is not trigered	If the peak switch current reaches the 78% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 78% of ILIMSET and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0x81h - B3_REG02 – PMIC BUCK3 Configuration Register

Address = 0x81h	Default = 0xDCh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
Default	1	1	N/A	1	1	1	N/A	N/A
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MASK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck3 POK signal does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is disabled or drops out of regulation. B3_POK still provides real-time power good status.
OV_INT_MASK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck3 OV signal does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ISHUT_INT_MASK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck3 ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
IFLT_INT_MASK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck3 ILIM fault signal does not go to the master controller ILIM_FLT still provides current limit status.
IWARN_INT_MASK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck3 ILIM warn signal does not go to the master controller.ILIM_WARN still provides current limit warning status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

PMIC BUCK3 BASIC NON-VOLATILE

0x85h - B3_REG03 – PMIC BUCK3 Configuration Register

Address = 0x85h	Default = 0x5Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0 [7:0]							
Default	01011111							
Access	R/W							

Name	Description	Notes
VSET0 [7:0]	Buck3 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0<7:0>

0x86h - B3_REG04 – PMIC BUCK3 Configuration Register

Address = 0x86h	Default = 0x5Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1 [7:0]							
Default	01011111							
Access	R/W							

Name	Description	Notes
VSET1 [7:0]	Buck3 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1<7:0>

0x87h - B3_REG05 – PMIC BUCK3 Configuration Register

Address = 0x87h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	1	1	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON<3:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
ON	0 – Buck3 is enabled through normal sequencing 1 – Buck3 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	

0x88h - B3_REG06 – PMIC BUCK3 Configuration Register

Address = 0x88h	Default = 0x13h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
Default	0	0	010			011		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
RST	0 – Buck3 does not affect nRESET output 1 – Buck3 turning off asserts nRESET output low	
DBQL<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0x89h - B3_REG07 – PMIC BUCK3 Configuration Register

Address = 0x89h	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
Default	1	100			0010			
Access	R/W	R/W			R/W			

Name	Description		Notes
HSON_DL	Adjust the delay of high side FET turn-on 0: 0ns 1: 3ns		
ON DELAY<2:0>	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms	100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck3 input trigger and when it turns on.
OFF DELAY<3:0>	Sets the delay time between the Buck3 disable input to when it turns off.		Buck3 turnoff delay time is equal to OFF_DELAY * 1ms

0x8Ah - B3_REG08 – PMIC BUCK3 Configuration Register

Address = 0x8Ah	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
Default	01		00	0	0	0	01	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM<1:0>	00: IPEAK=5A, IVALLEY=5A 01: IPEAK=6A, IVALLEY=6.1A 10: IPEAK=7A, IVALLEY=6.8A 11: IPEAK=8A, IVALLEY=7.5A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck3 will shutdown if VIN_Buck3 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck3 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck3 will shutdown if Buck3_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck3_OUT occurs UV/OV.	
DB_DVS<1:0>	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0x8Bh - B3_REG09 – PMIC BUCK3 Configuration Register

Address = 0x8Bh	Default = 0xDCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
Default	1	1	0	1	1	1	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
POK_OPT	Option POK thresholds 0: Rising/Falling(87/84 % of OUT) 1: Rising/Falling(90/87 % of OUT)	
HSD_SLEW	0: Slow 1: High	
LSD_SLEW<1:0>	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0x8Ch - B3_REG10 – PMIC BUCK3 Configuration Register

Address = 0x8Ch	Default = 0x06h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			
Default	0	0	0	0	0110			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DISPLDN	0: VOUT discharge at turn off 1: VOUT not discharge at turn off	
PD_OPTION	0: Rdis = 6Ohm 1: Rdis = 20Ohm	Set the discharge resistance
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_RANGE_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> 1.875V
FREQ<3:0>	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

PMIC BUCK4 BASIC VOLATILE

0xA0h - B4_REG01 – PMIC BUCK4 Configuration Register

Address = 0xA0h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK Status. 1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV(110%/107%) 0: VOUT is Normal	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdownis trigered 0: Output Ilim Shutdown is not trigered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is trigered 0: Output Ilim Fault is not trigered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is trigered 0: Output Ilim Warning is not trigered	If the peak switch current reaches the 80% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 80% of ILIMSET and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0xA1h - B4_REG02 – PMIC BUCK4 Configuration Register

Address = 0xA1h	Default = 0xDCh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
Default	1	1	N/A	1	1	1	N/A	N/A
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MASK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Buck4 POK signal does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is disabled or drops out of regulation. B4_POK still provides real-time power good status.
OV_INT_MASK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Buck4 OV signal does not go to the master controller. This prevents Buck4 from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ISHUT_INT_MASK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Buck4 ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
IFLT_INT_MASK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Buck4 ILIM fault signal does not go to the master controller ILIM_FLT still provides current limit status.
IWARN_INT_MASK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Buck4 ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

PMIC BUCK4 BASIC NON-VOLATILE

0xA5h - B4_REG03 – PMIC BUCK4 Configuration Register

Address = 0xA5h	Default = 0x3Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET0 [7:0]							
Default	00111100							
Access	R/W							

Name	Description	Notes
VSET0 [7:0]	Buck4 output voltage setting in ACTIVE mode.	VOUT0 = 0.6 +(20 mV or 5mV step)* VSET0<7:0>

0xA6h - B4_REG04 – PMIC BUCK4 Configuration Register

Address = 0xA6h	Default = 0x3Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSET1 [7:0]							
Default	00111100							
Access	R/W							

Name	Description	Notes
VSET1 [7:0]	Buck4 output voltage setting for dynamic voltage scaling and SLEEP mode.	VOUT1 = 0.6 +(20 mV or 5mV step)* VSET1<7:0>

0xA7h - B4_REG05 – PMIC BUCK4 Configuration Register

Address = 0xA7h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON<3:0>				ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	1	1	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
DBON<3:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
ON	0 – Buck4 is enabled through normal sequencing 1 – Buck4 is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Buck4 shuts down when its sequenced input shuts down 1 – Buck4 stays on when its sequenced input shuts down	
SLEEP EN	0 – Buck4 stays on when the IC enters Sleep mode 1 – Buck4 turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Buck4 stays on when the IC enters Deep Sleep mode 1 – Buck4 turns off when the IC enters Deep Sleep mode	

0xA8h - B4_REG06 – PMIC BUCK4 Configuration Register

Address = 0xA8h	Default = 0x21h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBOK_SEL	RST	DBQL<2:0>			DBOK<2:0>		
Default	0	0	100			001		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
DBOK_SEL	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
RST	0 – Buck4 does not affect nRESET output 1 – Buck4 turning off asserts nRESET output low	
DBQL<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0xA9h - B4_REG07 – PMIC BUCK4 Configuration Register

Address = 0xA9h	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	HSON_DL	ON DELAY<2:0>			OFF DELAY<3:0>			
Default	1	100			0010			
Access	R/W	R/W			R/W			

Name	Description		Notes
HSON_DL	Adjust the delay of high side FET turn-on 0: 0ns 1: 3ns		
ON DELAY<2:0>	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms	100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Buck4 input trigger and when it turns on.
OFF DELAY<3:0>	Sets the delay time between the Buck3 disable input to when it turns off.		Buck4 turnoff delay time is equal to OFF_DELAY * 1ms

0xAAh - B4_REG08 – PMIC BUCK4 Configuration Register

Address = 0xAAh	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM<1:0>		VINUVOV_REG_SHUT_MASK	VINUVOV_SYS_SHUT_MASK	UVOV_REG_SHUT_MASK	UVOV_SYS_SHUT_MASK	DB_DVS<1:0>	
Default	10		0	0	0	0	00	
Access	R/W		R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
ILIM<1:0>	00: IPEAK=2A, IVALLEY=2A 01: IPEAK=2.6A, IVALLEY=2.5A 10: IPEAK=3.1A, IVALLEY=3.1A 11: IPEAK=4A, IVALLEY=3.8A	
VINUVOV_REG_SHUT_MASK	When this bit =0, Buck4 will shutdown if VIN_Buck4 occurs UV/OV.	
VINUVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if VIN_Buck4 occurs UV/OV.	
UVOV_REG_SHUT_MASK	When this bit =0, Buck4 will shutdown if Buck4_OUT occurs UV/OV.	
UVOV_SYS_SHUT_MASK	When this bit =0, system will shutdown if Buck4_OUT occurs UV/OV.	
DB_DVS<1:0>	Determines DVS setting from the CMI code	Changing this bit may result in unexpected IC behavior.

0xABh - B4_REG09 – PMIC BUCK4 Configuration Register

Address = 0xABh	Default = 0xDCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	POK_OPT	HSD_SLEW	LSD_SLEW<1:0>	
Default	1	1	0	1	1	1	00	
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Name	Description	Notes
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
POK_OPT	Option POK thresholds 0: Rising/Falling(87/84 % of OUT) 1: Rising/Falling(90/87 % of OUT)	
HSD_SLEW	0: Slow 1: High	
LSD_SLEW<1:0>	Adjust Slew Rate Low-Side 00: Weak 01: Slow 10: Normal 11: Fast	

0xACh - B4_REG10 – PMIC BUCK4 Configuration Register

Address = 0xACh	Default = 0x04h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DISPLDN	PD_OPTION	FORCE_PWM	VOUT_RANGE_OPT	FREQ<3:0>			
Default	0	0	0	0	0100			
Access	R/W	R/W	R/W	R/W	R/W			

Name	Description	Notes
DISPLDN	0: VOUT discharge at turn off 1: VOUT not discharge at turn off	
PD_OPTION	0: Rdis = 6Ohm 1: Rdis = 20Ohm	Set the discharge resistance
FORCE_PWM	0: Not Force PWM Mode 1: Force PWM Mode	
VOUT_RANGE_OPT	0 = 20mV steps 1 = 5mV steps	Select VOUT Range 0: 0.6V --> 5.25V 1: 0.6V --> 1.875V
FREQ<3:0>	0000: 400kHz 1111: 1.9MHz Step: 100kHz	Select Frequency Switching

PMIC BOOST BASIC VOLATILE

0xC0h - BOOST_REG01 – PMIC Boost Configuration Register

Address = 0xC0h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	VOUT_OV_FLT	RFU	ILIM_SHUT	ILIM_FLT	ILIM_WARN	RFU	RFU
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	POK Status. 1: VOUT OK 0: VOUT NOT OK	Provides real-time power good status
VOUT_OV_FLT	OV Status. 1: VOUT > VOUT OV(110%/107%) 0: VOUT is Normal	When VOUT > OV, this bit goes high. It stays high until VOUT < OV and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ILIM_SHUT	ILIM Shutdown Status. 1: Output Ilim Shutdownis trigered 0: Output Ilim Shutdown is not trigered	If the peak switch current reaches the 125% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 125% of ILIMSET and it is read.
ILIM_FLT	ILIM Fault Status. 1: Output Ilim Fault is trigered 0: Output Ilim Fault is not trigered	If the peak switch current reaches the ILIMSET threshold, this bit goes high. It stays high until peak switch current < ILIMSET and it is read.
ILIM_WARN	ILIM Warning Status. 1: Output Ilim Warning is trigered 0: Output Ilim Warning is not trigered	If the peak switch current reaches the 80% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 80% of ILIMSET and it is read.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

0xC1h - BOOST_REG02 – PMIC Boost Configuration Register

Address = 0xC1h	Default = 0xDCh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	UV_INT_MASK	OV_INT_MASK	RFU	ISHUT_INT_MASK	IFLT_INT_MASK	IWARN_INT_MASK	RFU	RFU
Default	1	1	N/A	1	1	1	N/A	N/A
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
UV_INT_MASK	Mask POK Interrupt 1: Mask POK Interrupt 0: Unmask POK Interrupt	When 1, the Boost POK signal does not go to the master controller. This prevents Boost from asserting the nIRQ pin when it is disabled or drops out of regulation. BST_POK still provides real-time power good status.
OV_INT_MASK	Mask VOUT_OV Interrupt 1: Mask VOUT_OV Interrupt 0: Unmask VOUT_OV Interrupt	When 1, the Boost OV signal does not go to the master controller. This prevents Boost from asserting the nIRQ pin when it is above regulation limits. VOUT_OV_FLT still provides OV status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
ISHUT_INT_MASK	Mask ILIM SHUTDOWN Interrupt 1: Mask ILIM SHUTDOWN Interrupt 0: Unmask ILIM SHUTDOWN Interrupt	When 1, the Boost ILIM shutdown signal does not go to the master controller. ILIM_SHUT still provides current limit status.
IFLT_INT_MASK	Mask ILIM FAULT Interrupt 1: Mask ILIM FAULT Interrupt 0: Unmask ILIM FAULT Interrupt	When 1, the Boost ILIM fault signal does not go to the master controller ILIM_FLT still provides current limit status.
IWARN_INT_MASK	Mask ILIM WARM Interrupt 1: Mask ILIM WARM Interrupt 0: Unmask ILIM WARM Interrupt	When 1, the Boost ILIM warn signal does not go to the master controller. ILIM_WARN still provides current limit warning status.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.
RFU	Reserved for future use	Changing this bit may result in unexpected IC behavior.

PMIC BOOST BASIC NON-VOLATILE

0xC5h - BOOST_REG03 – PMIC Boost Configuration Register

Address = 0xC5h	Default = 0x98h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO_ON	ILIM2_SW_FLT_MSK	VSET0 [5:0]					
Default	1	0	011000					
Access	R/W	R/W	R/W					

Name	Description	Notes
LDO_ON	1: LVLDO will turn on when VCC> vcc_uvlo	
ILIM2_SW_FLT_MSK	1: Mask Boost ILIM and SW fault	
VSET0 [7:0]	Boost output voltage setting.	VOUT = 10.8V +50mV* VSET0<5:0>

0xC6h - BOOST_REG04 – PMIC Boost Configuration Register

Address = 0xC6h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	BST_DBON<3:0>				BST_ON	QLTCH	SLEEP EN	DP SLEEP EN
Default	0000				1	1	1	1
Access	R/W				R/W	R/W	R/W	R/W

Name	Description	Notes
BST_DBON<3:0>	Determines Boost startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
BST_ON	0 – Boost is enabled through normal sequencing 1 – Boost is enabled via I2C that bypasses normal sequencing	
QLTCH	0 – Boost shuts down when its sequenced input shuts down 1 – Boost stays on when its sequenced input shuts down	
SLEEP EN	0 – Boost stays on when the IC enters Sleep mode 1 – Boost turns off when the IC enters Sleep mode	
DP SLEEP EN	0 – Boost stays on when the IC enters Deep Sleep mode 1 – Boost turns off when the IC enters Deep Sleep mode	

0xC7h - BOOST_REG05 – PMIC Boost Configuration Register

Address = 0xC7h	Default = 0x77h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Faults_REG_MASK	RST	DBQL<2:0>			DBOK<2:0>		
Default	0	1	110			111		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
Faults_REG_MASK	1: Prevent Boost regulator react to BOOST Output OVUV fault	
RST	0 – Boost does not affect nRESET output 1 – Boost turning off asserts nRESET output low	
DBQL<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.
DBOK<2:0>	Determines startup sequencing from the CMI code	Changing this bit may result in unexpected IC behavior.

0xC8h - BOOST_REG06 – PMIC Boost Configuration Register

Address = 0xC8h	Default = 0x42h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	Faults_SYS_MASK	ON DELAY<2:0>			OFF DELAY<3:0>			
Default	0	100			0010			
Access	R/W	R/W			R/W			

Name	Description		Notes
Faults_SYS_MASK	1: prevent the system react to BOOST Output OVUV		
ON DELAY<2:0>	000 = 0ms 001 = 0.25ms 010 = 0.5m 011 = 1ms	100 = 2ms 101 = 4ms 110 = 8m 111 = 16ms	Programs the delay time between the Boost input trigger and when it turns on.
OFF DELAY<3:0>	Sets the delay time between the Buck3 disable input to when it turns off.		Boost turnoff delay time is equal to OFF_DELAY * 1ms

0xC9h - LDO_REG01 – PMIC LDO Configuration Register

Address = 0xC9h	Default = 0x66h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ILIM_LDO<1:0>		VSET_LDO<5:0>					
Default	01		100110					
Access	R/W		R/W					

Name	Description	Notes
ILIM_LDO<1:0>	ILIM of LDO: 00: 88mA 01: 148mA 10: 228mA 11: 393mA	
VSET_LDO<5:0>		VLDO= 0.6V+50mV*VSET0<5:0>