



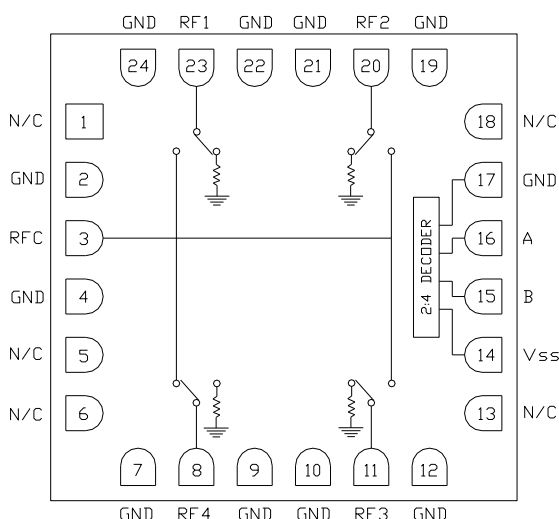
CMD203C4

DC-20 GHz SP4T Non-reflective Switch

Product Overview

The CMD203C4 is a broadband MMIC SP4T switch housed in a leadless 4x4 mm surface mount package. The CMD203C4 covers DC to 20 GHz and offers a low insertion loss of 2.4 dB and high isolation of 39 dB at 10 GHz. The switch also includes an on board binary decoder circuit which reduces the number of required logic control lines from four to two. The CMD203C4 operates using complementary control voltage logic lines of 0/-5 V and consumes little DC current.

Functional Block Diagram



Key Features

- Low Loss Broadband Performance
- High Isolation
- Non-Reflective Design
- Integrated 2:4 TTL Decoder
- Pb-Free RoHs Compliant 4x4 SMT Package

Ordering Information

Part No.	Description
CMD203C4	DC-20 GHz SP4T Non-reflective Switch, 100 Piece 7" Reel
CMD203C4-EVB	Evaluation Board

Electrical Performance ($V_{ctl} = 0/-5 V$, $V_{ss} = -5 V$, $T_A = 25 ^\circ C$, $F = 10 GHz$)

Parameter	Min	Typ	Max	Units
Frequency Range		DC - 20		GHz
Insertion Loss		2.4		dB
Isolation		39		dB
Return Loss - On State		9		dB
Return Loss RF1, RF2, RF3, RF4 - Off State		9		dB
Input P1dB		21		dBm
Switching Characteristics				
tRISE, tFALL (10/90% RF)		66		ns
tON, tOFF (50% CTL to 10/90% RF)		81/8		ns

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+27 dBm
Bias Voltage (V_{SS})	-7V
Control Voltage Range (A, B)	+0.5V to -7.5V
Channel Temperature, T_{ch}	150 °C
Operating Temperature	-40 to 85 °C
Storage Temperature	-55 to 150 °C
Power Dissipation, P_{diss}	531 mW
Thermal Resistance, θ_{JC}	122.23 °C/W

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Bias Voltage & Current

V_{SS} Range = -5.0V \pm 10%		
V_{SS} (V)	I_{SS} (Typ) (mA)	I_{SS} (Max) (mA)
-5	4.5	8.0

TTL/CMOS Control Voltages

State	Bias Condition
Low	-1V to 0V @ 0.5 mA Typ
High	-7V to -3V @ 1 uA Typ

Truth Table

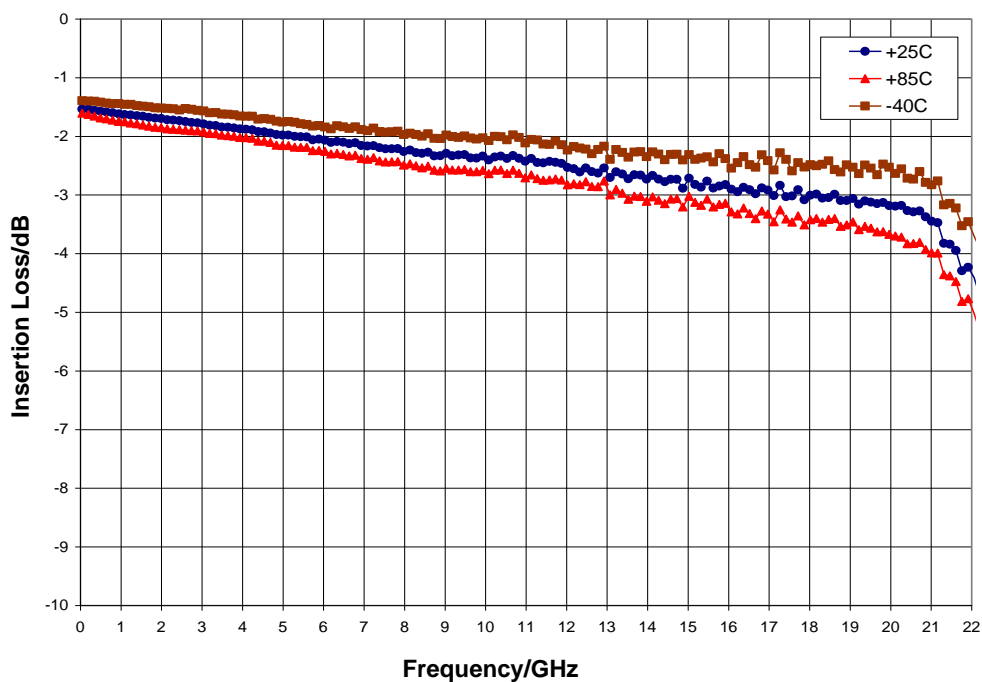
Control Input		Signal Path State
A	B	RFC to:
High	High	RF1
Low	High	RF2
High	Low	RF3
Low	Low	RF4

Electrical Specifications ($V_{ctl} = 0/-5$ V, $V_{SS} = -5$ V $T_A = 25$ °C)

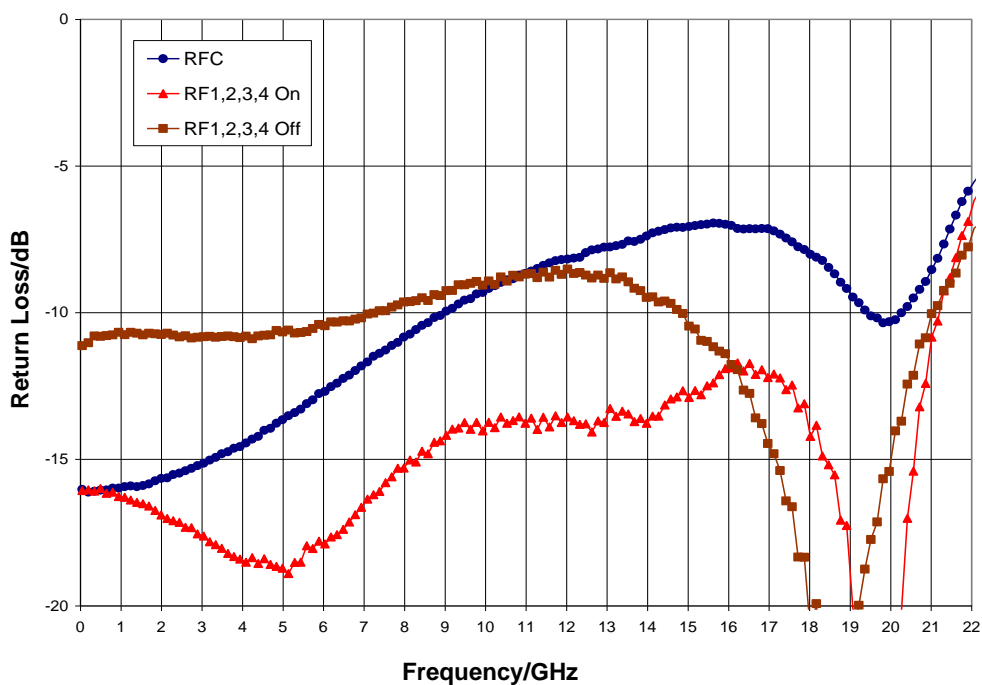
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range	DC - 6			DC - 14			DC - 20			GHz
Insertion Loss		2	2.4		2.7	3.1		3.2	3.6	dB
Isolation	37	44		27	35		22	30		dB
Return Loss - On State		11			8			8		dB
Return Loss - Off State		17			14			13		dB
Input P1dB		19.5			21			22		dBm
Input IP3		28			30			30		dBm
Switching Characteristics										
tRISE, tFALL (10/90% RF)		66			66			66		ns
tON, tOFF (50% CTL to 10/90% RF)		81/8			81/8			81/8		ns

Typical Performance

Insertion Loss vs. Temperature

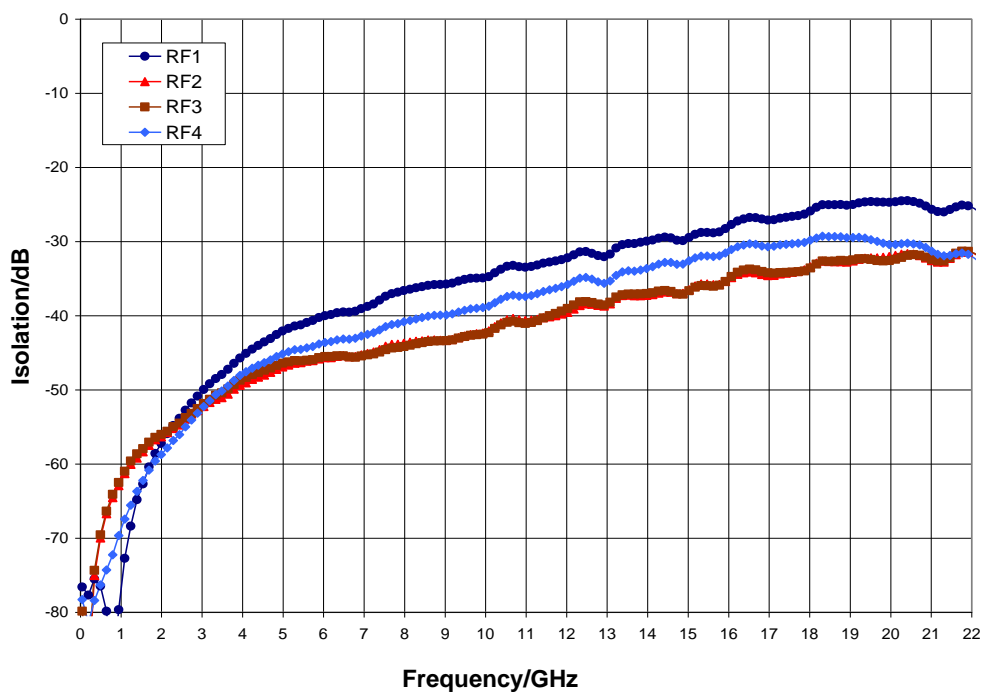


Return Loss

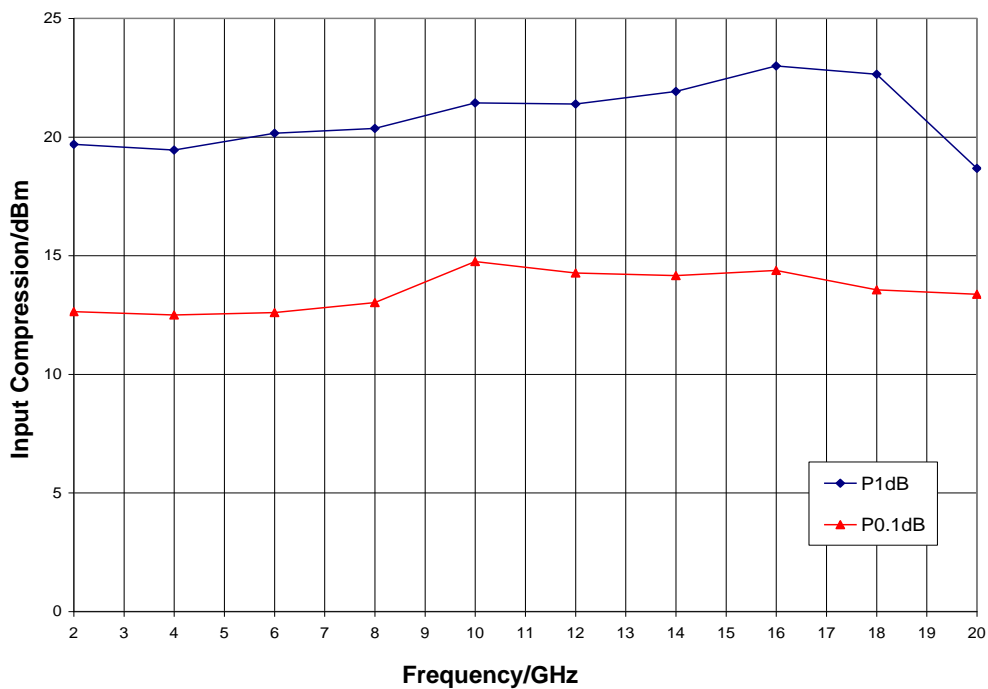


Typical Performance

Isolation Between Ports RFC and RF1/RF2/RF3/RF4

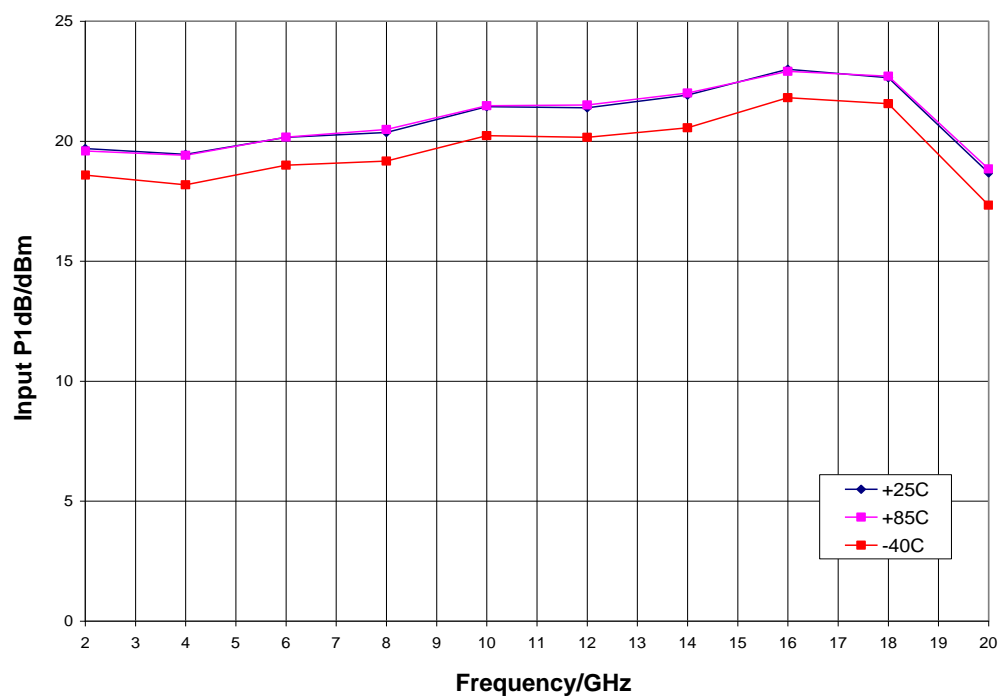


Input P1dB and P0.1dB Compression Point

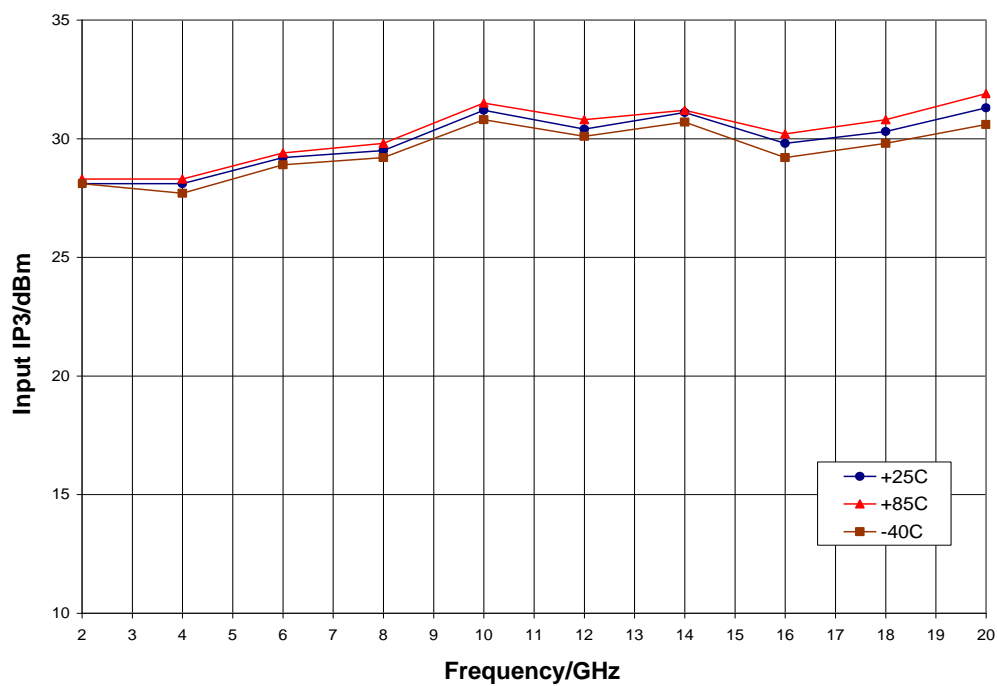


Typical Performance

Input P1dB vs. Temperature

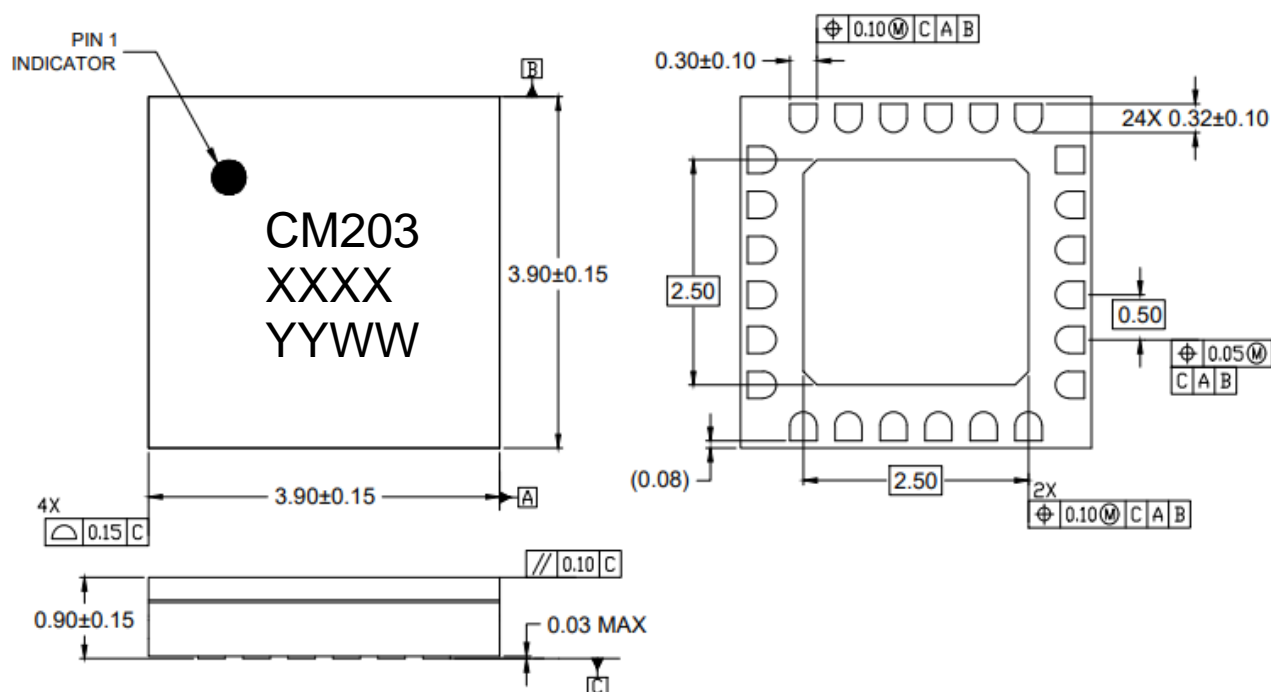


Input Third Order Intercept Point vs. Temperature



Mechanical Information

Package Information and Dimensions



Notes:

- All dimensions shown in mm.
- Material: Black alumina
- Lead finish:
 - Ni: 8.89 μ m max 1.27 μ m min
 - Pd: 0.17 μ m max, 0.07 μ m min
 - Au: 0.254 μ m max, 0.03 μ m min
- Marking
 - Line 1: Part number as indicated
 - Example: CMD203C4 shall be marked as CM203
 - Line 2: Lot number shall consist of the last 4 digits of unique alphanumeric trace code
 - Line 3: Date code shall consist of the last 2 digits of the year of manufacture followed by a 2-digit week code
- Alternate pin #1 identifier is a single square pad
- Alternate die paddle may have chamfered corners

Recommended PCB Land Pattern

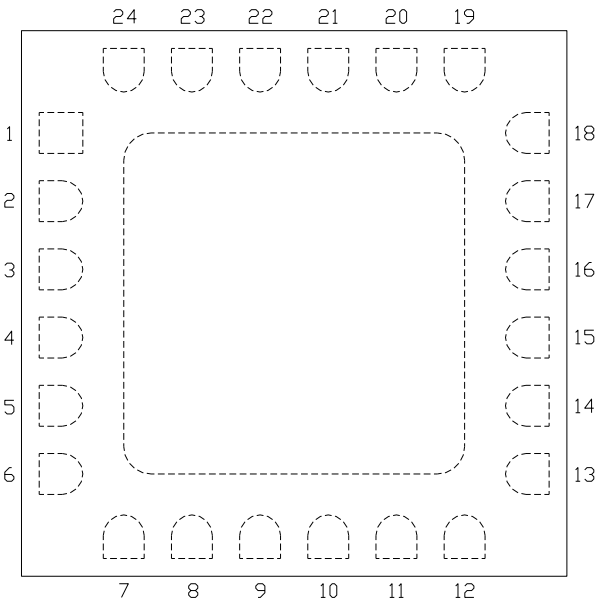
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile


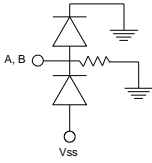
Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile.

Pin Description

Pin Diagram



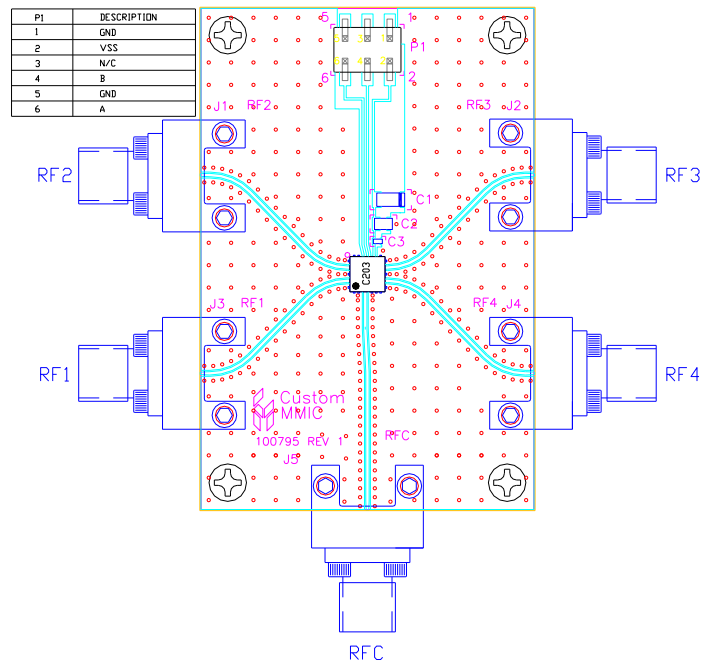
Functional Description

Pin	Function	Description	Schematic
1, 5, 6, 13, 18	N/C	No connection required These pins may be connected to RF / DC ground	
2, 4, 7, 9, 10, 12, 17, 19, 21, 22, 24 and die paddle	Ground	Connect to RF / DC ground	
3, 8, 11, 20, 23	RFC, RF4, RF3, RF2, RF1	These pins are DC coupled and matched to 50 ohm Blocking capacitors are required if RF line potential is not equal to 0 V	
14	V _{SS}	Power supply voltage	
15	CTLB	See truth table and control voltage table	
16	CTLA	See truth table and control voltage table	

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



Bill of Material

Designator	Value	Description
J1 - J5		SMA End Launch Connector
P1		6 Pin Header
C1	0.33 μ F	Capacitor, Tantalum
C2	1000 pF	Capacitor, 0603
C3	100 pF	Capacitor, 0402
U1		CMD203C4 SP4T Switch
PCB		100795 Evaluation PCB

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1A	ESDA / JEDEC JS-001-2012
MSL – Moisture Sensitivity Level	Level 1	JEDEC standard IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- SVHC Free
- Halogen Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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