APPLICATION NOTE AN-116

ACT81460 Register Definitions – CMI 101

Abstract

This application note identifies and explains the ACT81460 and ACT81461 internal registers that help make this IC flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. The default register settings in this application note are only valid for the ACT81460VM101. Refer to each datasheet for each specific IC's functional differences from the settings in this document.

Introduction

The ACT81460 is an ActivePMU power management unit from Qorvo. It is designed to power a wide range of processors, FPGA's, peripherals, and microcontrollers. The ACT81460 core includes Two DC/DC step down converters using integrated power FETs, one Buck-boost converter, three LDOs, three load switches, a high voltage boost, and constant current sink for driving LEDs, and a linear battery charger. Each of these regulators can be configured for a wide range of output voltages through the I^2C interface.

Today's applications require more complexity in their startup and sequencing requirements. The ACT81460 I2C registers allow for customized configurations for these requirements. Although the ACT81460 is programmed at the factory with a default configuration, these settings can be changed through the I^2C interface to provide customized configurations optimized for a specific processor and/or end application. IC configurability includes many options such as output voltage, startup sequencing, startup timing, slew rates, GPIO configuration, fault responses, and more. Qorvo identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT81460's CMI 101. Refer to the datasheet for the specific changes to other CMI versions.

Register Types

The ACT88329 ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult Sales@Qorvo.com for custom options and minimum order quantities.

Factory Non-Volatile – Factory bits. These bits are used by the factory to set IC functionality. The customer can read these bits but cannot write to them. The default values can be modified at the factory to optimize IC functionality for specific applications.

The ACT81460 contains nine major register spaces.

MASTER REGISTERS & PBIO Reg	0x00h to 0x23h
LDOLS12 Reg	0x30h to 0x3Dh
LDOLS34 Reg	0x40h to 0x4Dh
LSW56 Reg	0x50h to 0x5Dh
BUCK1 Reg	0x60h to 0x67h
BUCK2 Reg	0x70h to 0x77h
BOOST Reg	0x80h to 0x85h
BB Reg	0x90h to 0x97h
APLC Reg	0xC0h to 0xC9h

Register Map Overview

The following table shows an overview of the ACT81460 register map. Note that not all register addresses are sequential.

AADR (HEX)	7	6	5	4	3	2	1	0
	MASTER REGISTERS & PBIO ADDRESS							
00	RFU	WD TIMER ALERT	TWARN (Warning)	VSYSSTAT	PC STAT (power cycle)	SR STAT (soft reset)	PBASTAT	PBDSTAT
01	RFU	WD ALERT MSK	TMSK (Interrupt Mask)	VSYSMSK	PC STAT MASK	SR STAT MASK	PBAMSK	PBDMSK
02	FACTORY MODE	RFU	OTS	VSYSDAT	DVS_FROM_I2C_DB11	DVS_FROM_I2C_DB10	DVS_FROM_I2C_DB9	PBDAT
03	TRST_DLY[1:0]		PB WAIT TIME SET [1:0]		VSYSMON			
04	RFU	RFU	RFU	DIS DPSLP PWROFF DELAY	IOB2 DELAY EN (2.5ms)	IOB1 DEL EN (2.5ms)	DIS OV UV SHUTDOWN	ANA MODE EN
05	MODEB1				MUXB1			
06	MODEB2				MUXB2			
07	MODE D1				MUXD1[3:0]/ANALOG MODES:BYPASS_BUFF,OUTMODE,AMUX[1:0]			
08	MODE D2				MUXD2[3:0]/ANALOG MODES:BYPASS_BUFF,OUTMODE,AMUX[1:0]			
09	DPSLP EN	SLEEP EN	IREF_ BUF HP MODE	TM_DISOTP	BST_SNK_IN	SEL_BST_SNK[1:0]		EN_HPWR_BG_ALLTIME
18	INTADR							
19	PB COUNTER/TIMER [7:0] = CODE*64ms							
1A	RFU	RFU	RFU	OK_START	RFU	WAKETRG (UNUSED)	WDPCEN	WDSREN
1B	SHIP MODE (Not used)	RFU	POWER OFF	MR	SLEEP	RFU	DPSLP	RFU
1C	LED1 DBL BLINK	LED_DELAY1<2:0>			ILED1<3:0>			
1D	LED2 DBL BLINK	LED_DELAY2<2:0>			ILED2<3:0>			
1E	LED_BREATHE1_EN	PWMFREQ1			PWMDUTY1			
1F	LED_BREATHE2_EN	PWMFREQ2			PWMDUTY2			
20	PASSWD							
21	RFU	RFU	RFU	RFU	RFU	RFU	GPIO2 STAT	GPIO1 STAT
22	RFU	RFU	RFU	RFU	RFU	RFU	GPIO2 INTR	GPIO1 INTR
23	RFU	RFU	RFU	RFU	RFU	RFU	GPIO2 MASK	GPIO1 MASK
	LDOLS12 ADDRESS							
30	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
31	RFU	RFU	LDO 1 VSET					
32	ON LDO1 (DEFAULT 1)	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
33	OFF DELAY <3:0>				RST	DBOK		
34	DBON				MODE	ON DELAY <2:0>		
35	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_LDO2	OV_FLTMSK_LDO2	ILIM_FLTMSK_LDO2	RFU
36	RFU	RFU	LDO 2 VSET					
37	ON LDO2 (DEFAULT 1)	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
38	OFF DELAY <3:0>				RST	DBOK		
39	DBON				MODE	ON DELAY <2:0>		
3D	QLTCH LDO2	QLTCH LDO1	LDO2 ILIM SHUTDOWN DIS	LDO1 ILIM SHUTDOWN DIS	RFU	EN_LDO12_ILIM	EN_LDO12_OK	EN_LDO12_OV
	LDOLS34 ADDRESS							
40	PWR_GOOD_LDO3	OV_LDO3	ILIM_LDO3	RFU	UV_FLTMSK_LDO3	OV_FLTMSK_LDO3	ILIM_FLTMSK_LDO3	RFU
41	EN_34_OK_OV_ILIM	EN LDO3 LOAD SW MODE	LDO 3 VSET					
42	ON LDO3 (DEFAULT 1)	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
43	OFF DELAY <3:0>				RST	DBOK		
44	DBON				MODE	ON DELAY <2:0>		
45	PWR_GOOD_LSW4	OV_LSW4	ILIM_LSW4	RFU	UV_FLTMSK_LSW4	OV_FLTMSK_LSW4	ILIM_FLTMSK_LSW4	RFU
46	NOT USED, NVM NOT POPULATED							
47	ON LSW4 (DEFAULT 1)	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
48	OFF DELAY <3:0>				RST	DBOK		
49	DBON				MODE	ON DELAY <2:0>		
4D	QLTCH LSW4	QLTCH LDO3	LSW4 ILIM SHUTDOWN DIS	LSW3 ILIM SHUTDOWN DIS	ILIM_TRIM_LSW4[1:0]		ILIM_TRIM_LDO3[1:0]	
	LSW56 ADDRESS							
50	PWR_GOOD_LSW5	OV_LSW5	ILIM_LSW5	RFU	UV_FLTMSK_LSW5	OV_FLTMSK_LSW5	ILIM_FLTMSK_LSW5	RFU
51	NOT USED, NVM NOT POPULATED							
52	ON LSW5 (DEFAULT 1)	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
53	OFF DELAY <3:0>				RST	DBOK		
54	DBON				MODE	ON DELAY <2:0>		
55	PWR_GOOD_LSW6	OV_LSW6	ILIM_LSW6	RFU	UV_FLTMSK_LSW6	OV_FLTMSK_LSW6	ILIM_FLTMSK_LSW6	RFU
56	NOT USED, NVM NOT POPULATED							
57	ON LSW6 (DEFAULT 1)	PBIN EN	AUXIN EN	SLEEP EN	DPSLEEP EN	DBQL		
58	OFF DELAY <3:0>				RST	DBOK		
59	DBON				MODE	ON DELAY <2:0>		
5D	QLTCH LSW6	QLTCH LSW5	LSW6 ILIM SHUTDOWN DIS	LSW5 ILIM SHUTDOWN DIS	ILIM SET 56 <1>	ILIM SET 56 <0>	EN_LOWVIN_ILIM_MODE	EN_LSW_ILIM_COMPS
	BUCK1 ADDRESS							
60	POK	OV_FLT	ILIM_FLT	RFU	RFU	RFU	ILIM_FLT_MSK	RFU
61	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
62	FSW_SEL<1:0>		VSET0<5:0>					
63	VFF_RES_SEL<1:0>		VSET1<5:0>					
64	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_STDN_DIS	ILIM_SET
65	MODE	RST	DBQL<2:0>			DBOK<2:0>		
66	DBON<3:0>				DIS_ILIM_CBC	BURST_SEL	DBSTBY<1:0>	
67	VFF_RES_SEL<2>	ON DELAY<2:0>			OFF DELAY<3:0>			
	BUCK2 ADDRESS							
70	POK	OV_FLT	ILIM_FLT	RFU	RFU	RFU	ILIM_FLT_MSK	RFU
71	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
72	FSW_SEL<1:0>		VSET0<5:0>					
73	VFF_RES_SEL<1:0>		VSET1<5:0>					
74	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_STDN_DIS	ILIM_SET
75	MODE	RST	DBQL<2:0>			DBOK<2:0>		
76	DBON<3:0>				DIS_ILIM_CBC	BURST_SEL	DBSTBY<1:0>	
77	VFF_RES_SEL<2>	ON DELAY<2:0>			OFF DELAY<3:0>			

	BOOST ADDRESS							
80	EN_PD	BST ILIM WARN	BST_OV	BST_UV	RFU	BST_ILIM_WARN_MASK	BST_OV_MASK	BST_UV_MASK
81	DIS FAULTS	DISCC	LED BOOST REG VSET[5:0]					
82	DIS ILIM2 TURN OFF	CC_ADJ	LED BOOST ISET[5:0]					
83	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	ONDEL<2:0>		
84	MODE	DP SLEEP EN	DBQL<2:0>			DBOK<2:0>		
85	DBON<3:0>				OFF DELAY <3:0>			
	BB ADDRESS							
90	POK	OV_FLT	ILIM_FLT	RFU	RFU	RFU	ILIM_FLT_MSK	RFU
91	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
92	FSW_SEL<1:0>		VSET0<5:0>					
94	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_STDN_DIS	RFU
95	MODE	RST	DBQL<2:0>			DBOK<2:0>		
96	DBON<3:0>				Dis_toff_extended_boost	Dis_toff_extended	DBSTBY<1:0>	
97	VFF_RES_SEL<2>	ON DELAY<2:0>			OFF DELAY<3:0>			
	APLC ADDRESS							
C0	VIN_OV	VIN_UV	VINOK	VBAT LOW	No use	Q2ILIM_PROT	Q1ILIM	SUSPEND
C1	BAT_TEMP[2:0]			BAT_SUP_MODE	BAT_DETECTED	BAT CHG STATUS[2:0]		
C2	VCHGINx_STAT	BAT_STAT	CHG_STAT_CHANGE	VBAT_LOW_STAT	BAT_TEMP_STAT	THERMAL_LOOP_ACITVE	FAULT_STAT	SFTY_TIMER_EXPIRED
C3	INT_CHGSTAT_INRG_MASK	INT_BAT_DETECT_MASK	INT_CHG_STAT_MASK	VBAT_LOW_MASK1	INT_BATTEMP_INRG_MASK	INT_THERMAL_LOOP_MASK	INT_FAULT_MASK	PRECOND_SFTY_TIMER_MASK
C4	INT_CHGSTAT_OUTRG_MASK	RFU	RFU	VBAT_LOW_MASK2	INT_BATTEMP_OUTRG_MASK	T_JEITA_THRM_FLDBLOOP_MA	RFU	FSTCHG_SFTY_TIMER_MASK
C5	RFU	RFU	RFU	RFU	RFU	RFU	CLR_FLT_TIMER	FLT_TIMER_PAUSE
C6	VPRE[3:0]				IPRE[1:0]		EN_AUXIN	CHG_EN
C7	DIS_THERM_REG	VDCCC[1:0]		VTERM[4:0]				
C8	VSYS[1:0]		IN_ILIM[1:0]		VIN_STRT_DLY[1:0]		ITERM[1:0]	
C9	CORD COMP SETTING [2:0] (default 000 = off)			BAT_RECHG_THRESHOLD		I_TRICKLE_SET	V_TRICKLE[1:0]	

Master & PBIO (Push Button & I/O) Configuration Registers

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	WD TIMER ALERT	TWARN	VSYS STAT	PCSTAT	SR STAT	PBASTAT	PBDSTAT
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
WD TIMER ALERT	0 = Watchdog timer has not expired 1 = Watchdog timer has expired	When this bit = 1, an interrupt is generated on the nIRQ pin if WD ALERT MSK = 0.
TWARN	0 = IC junction temperature is below TWARN setting of 125 ^{O}C 1 = IC junction temperature is above TWARN setting of 125 ^{O}C	When this bit = 1, an interrupt is generated on the nIRQ pin if TMSK = 0
VSYSSTAT	0 = VSYS voltage is above UV warning threshold 1 = VSYS voltage is below UV warning threshold	When this bit = 1, an interrupt is generated on the nIRQ pin if VSYSMSK = 0. VSYS UV warning threshold is programmed with the VSYSMON bits in the 0x03h[3:0] register.
PC_STAT	0 = Power Cycle status is cleared 1 = Power Cycle has occurred.	When a power cycle occurs, PC_STAT is set and triggers and interrupt on nIRQ if the PC STAT MSK = 0. This bit is automatically cleared when read.
SR_ STAT	0 = Soft reset status is cleared 1 = Soft reset has occurred	When a soft reset occurs, SR_STAT is set and triggers and interrupt on nIRQ if the SR STAT MSK = 0. This bit is automatically cleared when read.
PBASTAT	0 = Push button asserted status is cleared 1 = Push button was asserted.	When the push button is pressed, PBASTAT is set and triggers and interrupt on nIRQ if the PBAMSK = 0. This bit is automatically cleared when read.
PBDSTAT	0 = Push button de-asserted status is cleared 1 = Push button was de-asserted.	When the push button is released, PBDSTAT is set and triggers and interrupt on nIRQ if the PBDMSK = 0. This bit is automatically cleared when read.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	WD ALERT MSK	TMSK	VSYSMSK	PC STAT MASK	SR STAT MASK	PBAMSK	PBDMSK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
WD ALERT MSK	0 = Unmasks the WD ALERT interrupt 1 = Masks the WD ALERT interrupt	When 1, the WD ALERT interrupt is masked. WD ALERT STAT provides real-time watchdog status.
TMSK	0 = Unmasks the TSTAT interrupt 1 = Masks the TSTAT interrupt	When 1, the TSTAT interrupt is masked. TSTAT still provides real-time temperature warn status.
VSYSMSK	0 = Unmasks the VSYSSTAT interrupt 1 = Masks the VSYSTAT interrupt	When 1, the VSYSTAT interrupt is masked. VSYSTAT still provides real-time UV warn status.
PC STAT MASK	0 = Unmasks the PC STAT interrupt 1 = Masks the PC STAT interrupt	When 1, the PC STAT interrupt is masked. PC STAT still provides real-time status.
SR STAT MASK	0 = Unmasks the SR STAT interrupt 1 = Masks the SR STAT interrupt	When 1, the SR STAT interrupt is masked. SR STAT still provides real-time status.
PBAMSK	0 = Unmasks the PBASTAT interrupt 1 = Masks the PBASTAT interrupt	When 1, the PBASTAT interrupt is masked. PBASTAT still provides real-time status.
PBDMSK	0 = Unmasks the PBDSTAT interrupt 1 = Masks the PBDSTAT interrupt	When 1, the PBDSTAT interrupt is masked. PBDSTAT still provides real-time status.

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	FACTORY MODE/Qorvo Use Only	RFU	OTS	VSYSDAT	DVS FROM I2C DB11	DVS FROM I2C DB10	DVS FROM I2C DB9	PBDAT
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
FACTORY MODE	0 = IC is in normal operating mode 1 = IC is in factory programming mode	Qorvo use only
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
OTS	Over temperature shutdown	Temperature higher than shutdown threshold.
VSYSDAT	0 = VSYS voltage is above UV warning threshold 1 = VSYS voltage is below UV warning threshold	This bit provides the real time UV warn status
DVS FROM I2C DB11	0 = De-asserts DB11 low. 1 = Asserts DB11 high.	Do not change this register value. Changing the register value can affect IC functionality.
DVS FROM I2C DB10	0 = De-asserts DB11 low. 1 = Asserts DB11 high.	Do not change this register value. Changing the register value can affect IC functionality.
DVS FROM I2C DB9	0 = De-asserts DB11 low. 1 = Asserts DB11 high.	Do not change this register value. Changing the register value can affect IC functionality.
PBDAT	0 = Push button is de-asserted low. 1 = Push button is asserted high.	This bit provides the real time pushbutton status

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x4Ah	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	TRST DLY [1:0]		PB WAIT TIME SET [1:0]		VSYSMON [3:0]			
Default	01		00		0010			
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
TRST DLY [1:0]	Reset timer delay setting 00 = 20ms 01 = 40ms 10 = 60ms 11 = 100ms	Reset timer delay settings. Reset output is asserted after this delay period following the POK / PGOOD signal from the last regulator that controls the reset output signal (nRESET).
PB WAIT TIME SET [1:0]	00 = 32ms 01 = 500ms 10 = 1000ms 11 = 2000ms	This sets the minimum pushbutton wait time.
VSYSMON [3:0]	0000 to 0101= (not allowed) 0110 = 2.6V 0111 = 2.7V 1000 = 2.8V 1001 = 2.9V 1010 = 3.0V 1011 = 3.1V 1100 = 3.2V 1101 = 3.3V 1110 = 3.4V 1111 = 3.5V	This sets the VSYS warning threshold. When the VSYS voltage rises above this threshold, the regulators turn on. When the VSYS voltage drops below this threshold, an interrupt is generated to warn the system controller of low VSYS voltage. The regulators remain on when the VSYS voltage drops below this threshold. The output shut down if the VSYS voltage drops below the IC's UVLO falling threshold of 2.4V

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	DIS DPSLP POWEROFF DEL	IOB2 DELAY EN	IOB1 DELAY EN	DIS OV UV SHUT DOWN	ANA MODE EN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DIS DPSLP POWER OFF DEL	0 = Power off sequence is followed when IC enters DSPLP and POWER OFF modes. 1 = Power off sequence is DISABLED when IC enters DSPLP and POWER OFF modes.	Control bit to enable or disable power off delays during entry into DPSLP or POWER OFF modes.
IOB2 DEL EN	0 = IOB2 2.5ms Delay Disabled. 1 = IOB2 2.5ms Delay Enabled.	Control input to enable GPIO (pin C3) output delay
IOB1 DEL EN	0 = IOB1 2.5ms Delay Disabled. 1 = IOB1 2.5ms Delay Enabled.	Control input to enable GPIO (pin D3) output delay
DIS OV UV SHUT DOWN	0 = Leave OV UV FLT State enabled 1 = Disable OV UV FLT State	When a regulator POK or system UV/OV fault occurs, the OV UV FLT state is entered to shut down all regulators and re-try in 100ms
ANA MODE EN	0 = Analog mode GPIOs are disabled 1 = Analog mode GPIOs are enabled	Used for simple On/Off register bit control of analog GPIO functions.

MSTR05 - Master Configuration Register

Address = 0x05h	Default = 0x0Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE B1 [3:0]				MUX B1 [3:0]			
Default	0000				1110			
Access	R/W				R/W			

Name	Description	Notes
MODEB1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUXB1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR06 - Master Configuration Register

Address = 0x06h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODEB2 [3:0]				MUXB2 [3:0]			
Default	0000				1111			
Access	R/W				R/W			

Name	Description	Notes
MODEB2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUXB2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR07 - Master Configuration Register

Address = 0x07h	Default = 0x6Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODED1 [3:0]				MUXD1 [3:0]			
Default	0110				1101			
Access	R/W				R/W			

Name	Description	Notes
MODED1 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUXD2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR08 - Master Configuration Register

Address = 0x08h	Default = 0x29h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODED2 [3:0]				MUXD2 [3:0]			
Default	0010				1001			
Access	R/W				R/W			

Name	Description	Notes
MODED2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MUXD2 [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DPSLP EN	SLEEP EN	IREF BUF HP MODE	TM DISOTP	BST SNK IN	SEL BST SNK [1:0]		EN HPWR BG ALL TIME
Default	0	0	0	0	0	00		0
Access	R/W	R/W	R/W	R/W	R/W	R/W		R/W

Name	Description	Notes
DPSLP EN	0 = DPSLP Mode Enable = 0 1 = DPSLP Mode Enable = 1	When DPSLP EN = 1, IC can enter/exit DPSLP State with a GPIO. When DPSLP EN = 0, the IC requires an I2C command to set register bit DPSLP_EN = 1 to enter DPSLP, and set DPSLP_EN = 0 to exit DPSLP
SLEEP EN	0 = SLEEP Mode Enable = 0 1 = SLEEP Mode Enable = 1	When SLEEP EN = 1, IC can enter/exit SLEEP State with a GPIO. When SLEEP EN = 0, the IC requires an I2C command to set register bit SLEEP_EN = 1 to enter SLEEP, and set SLEEP_EN = 0 to exit SLEEP
IREF BUF HP MODE		This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
TM DISOTP	0 = Enable Over Temperature Protection (OTP) 1 = Disable Over Temperature Protection (OTP)	
BST SNK IN	Control BOOST DISCC enable signal 1: Enable 0: Disable	
SEL BST SNK [1:0]	Select line to control BOOST DISCC 00 = BST_SNK_IN (REG09[3]) 01 = DB7 10 = DB12 11 = DB13	
EN HPWR BG ALL TIME/Active-Semi Internal Use Only	0 = Disable the use of higher current and higher accuracy bandgap reference all the time. 1 = Enable the use of higher current and higher accuracy bandgap reference all the time.	If bit = 0, the Higher current bandgap is enabled when the charger input is powered and quiescent current is not critical.

MSTR18 - Master Configuration Register

Address = 0x18h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INTADR [7:0]							
Default	0							
Access	RO							

Name	Description	Notes
INTADR [7:0]	Provides the hex address of the tile that generated the interrupt on nIRQ	MSTR = 0x01 GPIO = 0x02 LDO1 = 0x31 LDO2 = 0x32 LDO3 = 0x41 LSW4 = 0x42 LSW5 = 0x51 LSW6 = 0x52 BUCK1 = 0x61 BUCK2 = 0x71 BB = 0x91 BOOST = 0x80 APLC = 0xC0

MSTR19 - Master Configuration Register

Address = 0x19h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PB_COUNTER/TIMER [7:0]							
Default	0							
Access	RO							

Name	Description	Notes
PB_COUNTER/ TIMER [7:0]	Indicates the time of the pushbutton timer. The actual time is 64ms * value of this register	

MSTR1A - Master Configuration Register

Address = 0x1Ah	Default = 0x10h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [2:0]			OK_START	RFU	WAKETRG	WDPCEN	WDSREN
Default	000			1	0	0	0	0
Access	R/W			R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU [2:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
OK_START	Not used	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
WAKETRG	Not used	Do not change this register value. Changing the register value can affect IC functionality.
WDPCEN	0 = Disables power cycling when the watchdog timer expires 1 = Enables power cycling when the watchdog timer expires	Watch Dog timer is disabled by default.
WDSREN	0 = Disables soft reset when the watchdog timer expires 1 = Enables soft reset when the watchdog timer expires	Watch Dog timer is disabled by default.

MSTR1B - Master Configuration Register

Address = 0x1Bh	Default = 0x20h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	SHIP MODE	RFU	POWER OFF	MR	SLEEP	RFU	DPSLP	RFU
Default	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
SHIP MODE	Not Used	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
POWER OFF	0 = Exit POWER OFF mode 1 = Enter POWER OFF mode	Control Input to enter/exit Power Off Mode.
MR	0 = IC is not in reset 1 = Forces a manual reset	
SLEEP	0 = Exit SLEEP mode 1 = Enter SLEEP mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP	0 = Exit DPSLP mode 1 = Enter DPSLP mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR1C - Master Configuration Register

Address = 0x1Ch	Default = 0x08h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED1 DBL BLINK	LED1_DELAY<2:0>			ILED1<3:0>			
Default	0	000			1000			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED1 DBL BLINK	0 = LED1 in in single blink mode 1 = LED1 in in double blink mode	
LED1_DELAY<2:0>	000 = 0% 001 = 12.5% 010 = 25% 011 = 37.5% 100 = 50% 101 = 62.5% 110 = 75% 011 = 87.5%	
ILED1<3:0>	0000 = 0mA 0001 = 1.33mA 0010 = 2.66mA 0011 = 4mA 0100 = 5.33mA 0101 = 6.66mA 0110 = 8mA 0111 = 9.33mA 1000 = 10.66mA 1001 = 12mA 1010 = 13.33mA 1011 = 14.66mA 1100 = 16mA 1101 = 17.33mA 1110 = 18.66mA 1111 =20mA	

MSTR1D - Master Configuration Register

Address = 0x1Dh	Default = 0x08h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED2 DBL BLINK	LED2_DELAY<2:0>			ILED2<3:0>			
Default	0	000			1000			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED2 DBL BLINK	0 = LED2 in in single blink mode 1 = LED2 in in double blink mode	
LED2_DELAY<2:0>	000 = 0% 001 = 12.5% 010 = 25% 011 = 37.5% 100 = 50% 101 = 62.5% 110 = 75% 011 = 87.5%	
ILED2<3:0>	0000 = 0mA 0001 = 1.33mA 0010 = 2.66mA 0011 = 4mA 0100 = 5.33mA 0101 = 6.66mA 0110 = 8mA 0111 = 9.33mA 1000 = 10.66mA 1001 = 12mA 1010 = 13.33mA 1011 = 14.66mA 1100 = 16mA 1101 = 17.33mA 1110 = 18.66mA 1111 =20mA	

MSTR1E - Master Configuration Register

Address = 0x1Eh	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED1_BREATHE_EN	PWMFREQ1[2:0]			PWMDUTY1[3:0]			
Default	0	000			0010			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED1_BREATHE_EN	0 = Disables LED1 breathe mode 1 = Enables LED1 breathe mode	
PWMFREQ1[2:0]	000 = 2.15Hz = 0.466s 001 = 1.07Hz = 0.932s 010 = 0.54Hz = 1.864s 011 = 0.36Hz = 2.796s 100 = 0.27Hz = 3.728s 101 = 0.18Hz = 5.590s 110 = 0.13Hz = 7.450s 011 = 0.9Hz = 11.184s	
PWMDUTY1[3:0]	0000 = 6.25% 0001 = 12.5% 0010 = 18.75% 0011 = 25% 0100 = 31.25% 0101 = 37.5% 0110 = 43.75% 0111 = 50% 1000 = 56.25% 1001 = 62.5% 1010 = 68.75% 1011 = 75% 1100 = 81.25% 1101 = 87.5% 1110 = 93.75% 1111 = 100%	

MSTR1F - Master Configuration Register

Address = 0x1Fh	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LED2_BREATHE_EN	PWMFREQ2[2:0]			PWMDUTY2[3:0]			
Default	0	000			0010			
Access	R/W	R/W			R/W			

Name	Description	Notes
LED2_BREATHE_EN	0 = Disables LED2 breathe mode 1 = Enables LED2 breathe mode	
PWMFREQ2[2:0]	000 = 2.15Hz = 0.466s 001 = 1.07Hz = 0.932s 010 = 0.54Hz = 1.864s 011 = 0.36Hz = 2.796s 100 = 0.27Hz = 3.728s 101 = 0.18Hz = 5.590s 110 = 0.13Hz = 7.450s 011 = 0.9Hz = 11.184s	
PWMDUTY2[3:0]	0000 = 6.25% 0001 = 12.5% 0010 = 18.75% 0011 = 25% 0100 = 31.25% 0101 = 37.5% 0110 = 43.75% 0111 = 50% 1000 = 56.25% 1001 = 62.5% 1010 = 68.75% 1011 = 75% 1100 = 81.25% 1101 = 87.5% 1110 = 93.75% 1111 = 100%	

MSTR20 - Master Configuration Register

Address = 0x20h	Default = N/A	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	"PASSWD"							
Default	"Reserved for factory use only"							
Access	RO							

Name	Description	Notes
N/A	Reserved for factory use	Do not write to this register.

MSTR21 - Master Configuration Register

Address = 0x21h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU						GPIO2 STAT	GPIO1 STAT
Default	000000						0	0
Access	RO						RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
GPIO2 STAT	0 = The GPIO input is low 1 = The GPIO input is high	This bit is only valid when the GPIO is configured as an input.
GPIO1 STAT	0 = The GPIO input is low 1 = The GPIO input is high	This bit is only valid when the GPIO is configured as an input.

MSTR22 - Master Configuration Register

Address = 0x22h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU						GPIO2 INTR	GPIO1 INTR
Default	000000						0	0
Access	RO						RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
GPIO2 INTR	0 = No change in GPIO status since the last time this bit was read 1 = Indicates GPIO input change.	When set, this bit triggers an interrupt on nIRQ when mask bit = 0.
GPIO1 INTR	0 = No change in GPIO status since the last time this bit was read 1 = Indicates GPIO input change.	When set, this bit triggers an interrupt on nIRQ when mask bit = 0.

MSTR23 - Master Configuration Register

Address = 0x23h	Default = 0x03h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU						GPIO2 MASK	GPIO1 MASK
Default	000000						1	1
Access	RO						R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
GPIO2 MASK	0 = Unmasks GPIO2 1 = Masks GPIO2	When 1, GPIO2 interrupt is masked.
GPIO1 MASK	0 = Unmasks GPIO1 1 = Masks GPIO1	When 1, GPIO1 interrupt is masked.

LDO12_REG00 – LDO12 Configuration Register

Address = 0x30h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO1	OV_LDO1	ILIM_LDO1	RFU	UV_FLTMSK_LDO1	OV_FLTMSK_LDO1	ILIM_FLTMSK_LDO1	RFU
Default	0	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LDO1	0 – LDO1 voltage is below the power good threshold 1 – LDO1 voltage is above the power good threshold	Provides real-time power good status
OV_LDO1	0 – LDO1 voltage is below the overvoltage threshold 1 – LDO1voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO1	0 – LDO1 is below the ILIM threshold 1 – LDO1 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
UV_FLTMSK_LDO1	0 - Unmasks the PWR_GOOD_LDO1 register 1 - Masks the LDO1 UV register	When 1, the PWR_GOOD_LDO1 fault bit is masked from the master UV fault register. PWR_GOOD_LDO1 still provides real-time UV fault status.
OV_FLTMSK_LDO1	0 - Unmasks the OV_LDO1 register 1 - Masks the OV_LDO1 register	When 1, the OV_LDO1 fault bit is masked from the master OV fault register. OV_LDO1 still provides real-time OV status.
ILIM_FLTMSK_LDO1	0 - Unmasks the ILIM_LDO1 register 1 - Masks the ILIM_LDO1 register	When 1, the ILIM_LDO1 fault bit is masked from the master current limit fault register. ILIM_LDO1 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO1_VSET – LDO12 Voltage Set Register

Address = 0x31h	Default = 0x34h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	LDO1_VSET [5:0]					
Default	0	0	110100					
Access	R/W	R/W	R/W					

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO1_VSET [5:0]	LDO1 output voltage settin0g.	VOUT = 0.6V + LDO1_VSET [5:0] * 0.05V.

LDO12_REG02 – LDO12 Configuration Register

Address = 0x32h	Default = 0xC8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO1	PBINEN	AUXEN	SLEEPEN	DPSLEEPEN	DBQL [2:0]		
Default	1	1	0	0	1	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON LDO1	0 – LDO1 is enabled through normal sequencing routing 1 – LDO1 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	
AUXEN	0 – Cannot be turned on/off using Auxiliary Input 1 – Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	
DPSLEEPEN	0 – LDO1 stays on when the IC enters DEEP SLEEP mode 1 – LDO1 turns off when the IC enters DEEP SLEEP mode	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG03 – LDO12 Configuration Register

Address = 0x33h	Default = 0x50h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF DELAY [3:0]				RST	DBOK [2:0]		
Default	0101				0	0000		
Access	R/W				R/W	R/W		

Name	Description	Notes
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.
RST	0 – LDO1 does not affect nRESET output 1 – LDO1 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG04 – LDO12 Configuration Register

Address = 0x34h	Default = 0x0Bh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE	ON DELAY [2:0]		
Default	0000				0	1011		
Access	R/W				R/W	R/W		

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change these bits
MODE	Determines startup sequencing from the CMI code	Do not change this bit
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.

LDO12_REG05 – LDO12 Configuration Register

Address = 0x35h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO2	OV_LDO2	ILIM_LDO2	RFU	UV_FLTMSK_ LDO2	OV_FLTMSK_ LDO2	ILIM_FLTMSK_ LDO2	RFU
Default	0	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LDO2	0 – LDO2 voltage is below the power good threshold 1 – LDO2 voltage is above the power good threshold	Provides real-time power good status
OV_LDO2	0 – LDO2 voltage is below the overvoltage threshold 1 – LDO2 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO2	0 – LDO2 is below the ILIM threshold 1 – LDO2 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
UV_FLTMSK_LDO2	0 - Unmasks the PWR_GOOD_LDO2 register 1 - Masks the LDO2 UV register	When 1, the PWR_GOOD_LDO2 fault bit is masked from the master UV fault register. PWR_GOOD_LDO2 still provides real-time UV fault status.
OV_FLTMSK_LDO2	0 - Unmasks the OV_LDO2 register 1 - Masks the OV_LDO2 register	When 1, the OV_LDO2 fault bit is masked from the master OV fault register. OV_LDO2 still provides real-time OV status.
ILIM_FLTMSK_LDO2	0 - Unmasks the ILIM_LDO2 register 1 - Masks the ILIM_LDO2 register	When 1, the ILIM_LDO2 fault bit is masked from the master current limit fault register. ILIM_LDO2 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO2_VSET – LDO12 Voltage Set Register

Address = 0x36h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU		LDO2_VSET [5:0]					
Default	0		011000					
Access	R/W		R/w					

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO2_VSET [5:0]	LDO2 output voltage setting.	VOUT = 0.6V + LDO2_VSET [5:0] * 0.05V.

LDO12_REG07 – LDO12 Configuration Register

Address = 0x37h	Default = 0xC8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO2	PBINEN	AUXEN	SLEEPEN	DPSLEEPEN	DBQL [2:0]		
Default	1	1	0	0	1	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON LDO2	0 – LDO2 is enabled through normal sequencing routing 1 – LDO2 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	
AUXEN	0 – Cannot be turned on/off using Auxiliary Input 1 – Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	
DPSLEEPEN	0 – LDO2 stays on when the IC enters DEEP SLEEP mode 1 – LDO2 turns off when the IC enters DEEP SLEEP mode	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG08 – LDO12 Configuration Register

Address = 0x38h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF DELAY [3:0]				RST	DBOK [2:0]		
Default	0100				0	000		
Access	R/W				R/W	R/W		

Name	Description	Notes
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.
RST	0 – LDO2 does not affect nRESET output 1 – LDO2 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG09 – LDO12 Configuration Register

Address = 0x39h	Default = 0x0Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE	ON DELAY [2:0]		
Default	0000				1	100		
Access	R/W				R/W	R/W		

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change these bits
MODE	Determines startup sequencing from the CMI code	Do not change this bit
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.

LDO12_REG13 – LDO2 Configuration Register

LDO2 Address = 0x3Dh	Default = 0x37h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	QLTCH LDO2	QLTCH LDO1	LDO2 ILIM SHUTDOWN DIS	LDO1 ILIM SHUTDOWN DIS	RFU	EN LDO12 ILIM	EN LDO12 OK	EN LDO12 OV
Default	0	0	1	1	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
QLTCH LDO2	0 – LDO2 shuts down when its sequenced input shuts down 1 – LDO2 stays on when its sequenced input shuts down	
QLTCH LDO1	0 – LDO1 shuts down when its sequenced input shuts down 1 – LDO1 stays on when its sequenced input shuts down	
LDO2 ILIM SHUTDOWN DIS	0 = Enables the LDO2 shutdown during current limit 1 = Disables the LDO2 shutdown during current limit	
LDO1 ILIM SHUTDOWN DIS	0 = Enables the LDO1 shutdown during current limit 1 = Disables the LDO1 shutdown during current limit	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
EN LDO12 ILIM	0 = Disables the LDO1,2 current limit function 1 = Enables the LDO1,2 current limit function	
EN LDO12 OK	0 = Disables the LDO1,2 POK detection comparator 1 = Enables the LDO1,2 POK detection comparator	
EN LDO12 OV	0 = Disables the LDO1,2 OV detection comparator 1 = Enables the LDO1,2 OV detection comparator	

LDO34_REG00 – LDO34 Configuration Register

Address = 0x40h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LDO3	OV_LDO3	ILIM_LDO3	RFU	UV_FLTMSK_LDO3	OV_FLTMSK_LDO3	ILIM_FLTMSK_LDO3	RFU
Default	0	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LDO3	0 – LDO3 voltage is below the power good threshold 1 – LDO3 voltage is above the power good threshold	Provides real-time power good status
OV_LDO3	0 – LDO3 voltage is below the overvoltage threshold 1 – LDO3 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_LDO3	0 – LDO3 is below the ILIM threshold 1 – LDO3 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
UV_FLTMSK_LDO3	0 - Unmasks the PWR_GOOD_LDO3 register 1 - Masks the LDO3 UV register	When 1, the PWR_GOOD_LDO3 fault bit is masked from the master UV fault register. PWR_GOOD_LDO3 still provides real-time UV fault status.
OV_FLTMSK_LDO3	0 - Unmasks the OV_LDO3 register 1 - Masks the OV_LDO3 register	When 1, the OV_LDO3 fault bit is masked from the master OV fault register. OV_LDO3 still provides real-time OV status.
ILIM_FLTMSK_LDO3	0 - Unmasks the ILIM_LDO3 register 1 - Masks the ILIM_LDO3 register	When 1, the ILIM_LDO3 fault bit is masked from the master current limit fault register. ILIM_LDO3 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO3_VSET – LDO34 Voltage Set Register

Address = 0x41h	Default = 0x8Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN34_OK_ OV_ILIM	EN LDO3 LOAD SW MODE	LDO3_VSET [5:0]					
Default	1	0	001100					
Access	R/W	R/W	R/W					

Name	Description	Notes
EN 34 OK OV ILIM	0 – Disable LDO34 POK, OV and ILIM Comparators for lower quiescent current. 1 – Enable LDO34 POK, OV and ILIM Comparators for lower quiescent current.	
EN LDO3 LOAD SW MODE	0 – Operate in LDO mode 1 – Operate as a load switch	LDO3 Can be configured as load switch but only with a PMOS pass device and hence requires high input voltage (> 1.8V) for low on-resistance during operation as load switch.
LDO3_VSET [5:0]	LDO3 output voltage setting.	VOUT = 0.6V + LDO3_VSET [5:0] * 0.05V.

LDO34_REG02 – LDO34 Configuration Register

Address = 0x42h	Default = 0xC9h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LDO3	PBINEN	AUXEN	SLEEPEN	DPSLEEPEN	DBQL [2:0]		
Default	1	1	0	0	1	001		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON LDO3	0 – LDO3 is enabled through normal sequencing routing 1 – LDO3 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	
AUXEN	0 – Cannot be turned on/off using Auxiliary Input 1 – Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN	0 – LDO3 stays on when the IC enters Sleep mode 1 – LDO3 turns off when the IC enters Sleep mode	
DPSLEEPEN	0 – LDO3 stays on when the IC enters DEEP SLEEP mode 1 – LDO3 turns off when the IC enters DEEP SLEEP mode	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO34_REG03 – LDO34 Configuration Register

Address = 0x43h	Default = 0x10h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF DELAY [3:0]				RST	DBOK [2:0]		
Default	0001				0	000		
Access	R/W				R/W	R/W		

Name	Description	Notes
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.
RST	0 – LDO3 does not affect nRESET output 1 – LDO3 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO34_REG04 – LDO34 Configuration Register

Address = 0x44h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE	ON DELAY [2:0]		
Default	0000				1	111		
Access	R/W				R/W	R/W		

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change these bits
MODE	Determines startup sequencing from the CMI code	Do not change this bit
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.

LDO34_REG05 – LDO34 Configuration Register

Address = 0x45h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LSW4	OV_LSW4	ILIM_LSW4	RFU	UV_FLTMSK_LSW4	OV_FLTMSK_LSW4	ILIM_FLTMSK_LSW4	RFU
Default	0	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LSW4	0 – LSW4 voltage is below the power good threshold 1 – LSW4 voltage is above the power good threshold	Provides real-time power good status
OV_LSW4	0 – LSW4 voltage is above the overvoltage threshold 1 – LSW4 voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM_LSW4	0 – LSW4 is below the ILIM threshold 1 – LSW4 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
UV_FLTMSK_LSW4	0 - Unmasks the PWR_GOOD_LSW4 register 1 - Masks the LSW4 UV register	When 1, the PWR_GOOD_LSW4 fault bit is masked from the master UV fault register. PWR_GOOD_LSW4 still provides real-time UV fault status.
OV_FLTMSK_LSW4	0 - Unmasks the OV_LSW4 register 1 - Masks the OV_LSW4 register	When 1, the OV_LSW4 fault bit is masked from the master OV fault register. OV_LSW4 still provides real-time OV status.
ILIM_FLTMSK_LSW4	0 - Unmasks the ILIM_LSW4 register 1 - Masks the ILIM_LSW4 register	When 1, the ILIM_LSW4 fault bit is masked from the master current limit fault register. ILIM_LSW4 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO34_REG07 – LDO34 Configuration Register

Address = 0x47h	Default = 0xD8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LSW4	PBINEN	AUXEN	SLEEPEN	DPSLEEPEN	DBQL [2:0]		
Default	1	1	0	1	1	011		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON LSW4	0 – LSW4 is enabled through normal sequencing routing 1 – LSW4 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	
AUXEN	0 – Cannot be turned on/off using Auxiliary Input 1 – Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN	0 – LSW4 stays on when the IC enters Sleep mode 1 – LSW4 turns off when the IC enters Sleep mode	
DPSLEEPEN	0 – LSW4 stays on when the IC enters DEEP SLEEP mode 1 – LSW4 turns off when the IC enters DEEP SLEEP mode	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO34_REG08 – LDO34 Configuration Register

Address = 0x48h	Default = 0x30h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF DELAY [3:0]				RST	DBOK [2:0]		
Default	0011				0	000		
Access	R/W				R/W	R/W		

Name	Description	Notes
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in datasheet.
RST	0 – LSW4 does not affect nRESET output 1 – LSW4 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO34_REG09 – LDO34 Configuration Register

Address = 0x49h	Default = 0x0Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE	ON DELAY [2:0]		
Default	0000				1	101		
Access	R/W				R/W	R/W		

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.

LDO34_REG13 – LDO34 Configuration Register

Address = 0x4Dh	Default = 0x10h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	QLTCH LSW4	QLTCH LDO3	LSW4 ILIM SHUTDOWN DIS	LDO3 ILIM SHUTDOWN DIS	ILIM TRIM LSW4 [1:0]		ILIM TRIM LDO3 [1:0]	
Default	0	0	0	1	00		00	
Access	R/W	R/W	R/W	R/W	R/W		R/W	

Name	Description	Notes
QLTCH LSW4	0 – LS4 shuts down when its sequenced input shuts down 1 – LS4 stays on when its sequenced input shuts down	
QLTCH LDO3	0 – LDO3 shuts down when its sequenced input shuts down 1 – LDO3 stays on when its sequenced input shuts down	
LSW4 ILIM SHUTDOWN DIS	0 = Enables the LSW4 shutdown during current limit 1 = Disables the LSW4 shutdown during current limit	
LDO3 ILIM SHUTDOWN DIS	0 = Enables the LDO3 shutdown during current limit 1 = Disables the LDO3 shutdown during current limit	
ILIM TRIM LSW4 [1:0]	Trim registers for trimming the current limit value for LSW4	Trim registers, do not change.
ILIM TRIM LDO3 [1:0]	Trim registers for trimming the current limit value for LDO/LSW3	Trim registers, do not change.

LSW56_REG00 – LSW56 Configuration Register

Address = 0x50h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LSW5	OV_LSW5	ILIM_LSW5	RFU	UV_FLTMSK_LSW5	OV_FLTMSK_LSW5	ILIM_FLTMSK_LSW5	RFU
Default	0	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LSW5	0 – LSW5 voltage is below the power good threshold 1 – LSW5 voltage is above the power good threshold	Provides real-time power good status
OV_LSW5	0 – LSW5 voltage is below the overvoltage threshold 1 – LSW5 voltage is above the overvoltage threshold	Provides real-time overvoltage status
ILIM_LSW5	0 – LSW5 is below the ILIM threshold 1 – LSW5 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
UV_FLTMSK_LSW5	0 - Unmasks the PWR_GOOD_LSW5 register 1 - Masks the LSW5 UV register	When 1, the PWR_GOOD_LSW5 fault bit is masked from the master UV fault register. PWR_GOOD_LSW5 still provides real-time UV fault status.
OV_FLTMSK_LSW5	0 - Unmasks the OV_LSW5 register 1 - Masks the OV_LSW5 register	When 1, the OV_LSW5 fault bit is masked from the master OV fault register. OV_LSW5 still provides real-time OV status.
ILIM_FLTMSK_LSW5	0 - Unmasks the ILIM_LSW5 register 1 - Masks the ILIM_LSW5 register	When 1, the ILIM_LSW5 fault bit is masked from the master current limit fault register. ILIM_LSW5 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LSW56_REG02 – LSW56 Configuration Register

Address = 0x52h	Default = 0xD9h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LSW5	PBINEN	AUXEN	SLEEPEN	DPSLEEPEN	DBQL [2:0]		
Default	1	1	0	1	1	001		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON LSW5	0 – LSW5 is enabled through normal sequencing routing 1 – LSW5 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	
AUXEN	0 – Cannot be turned on/off using Auxiliary Input 1 – Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN	0 – LSW5 stays on when the IC enters Sleep mode 1 – LSW5 turns off when the IC enters Sleep mode	
DPSLEEPEN	0 – LSW5 stays on when the IC enters DEEP SLEEP mode 1 – LSW5 turns off when the IC enters DEEP SLEEP mode	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LSW56_REG03 – LSW56 Configuration Register

Address = 0x53h		Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF DELAY [3:0]				RST	DBOK [2:0]		
Default	0000				0	000		
Access	R/W				R/W	R/W		

Name	Description	Notes
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.
RST	0 – LSW5 does not affect nRESET output 1 – LSW5 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LSW56_REG04 – LSW56 Configuration Register

Address = 0x54h	Default = 0x0Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE	ON DELAY [2:0]		
Default	0000				1	111		
Access	R/W				R/W	R/W		

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.

LSW56_REG05 – LSW56 Configuration Register

Address = 0x55h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	PWR_GOOD_LSW6	OV_LSW6	ILIM_LSW6	RFU	UV_FLTMSK_LSW6	OV_FLTMSK_LSW6	ILIM_FLTMSK_LSW6	RFU
Default	0	0	0	0	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
PWR_GOOD_LSW6	0 – LSW6 voltage is below the power good threshold 1 – LSW6 voltage is above the power good threshold	Provides real-time power good status
OV_LSW6	0 – LSW6 voltage is above the overvoltage threshold 1 – LSW6 voltage is below the overvoltage threshold	Provides real-time overvoltage status
ILIM_LSW6	0 – LSW6 is below the ILIM threshold 1 – LSW6 is above the ILIM threshold	Provides real-time current limit status
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
UV_FLTMSK_LSW6	0 - Unmasks the PWR_GOOD_LSW6 register 1 - Masks the LSW6 UV register	When 1, the PWR_GOOD_LSW6 fault bit is masked from the master UV fault register. PWR_GOOD_LSW6 still provides real-time UV fault status.
OV_FLTMSK_LSW6	0 - Unmasks the OV_LSW6 register 1 - Masks the OV_LSW6 register	When 1, the OV_LSW6 fault bit is masked from the master OV fault register. OV_LSW6 still provides real-time OV status.
ILIM_FLTMSK_LSW6	0 - Unmasks the ILIM_LSW6 register 1 - Masks the ILIM_LSW6 register	When 1, the ILIM_LSW6 fault bit is masked from the master current limit fault register. ILIM_LSW6 still provides real-time overcurrent status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LSW56_REG07 – LSW56 Configuration Register

Address = 0x57h	Default = 0xD8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON LSW6	PBINEN	AUXEN	SLEEPEN	DPSLEEPEN	DBQL [2:0]		
Default	1	1	0	1	1	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON LSW6	0 – LSW6 is enabled through normal sequencing routing 1 – LSW6 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	
AUXEN	0 – Cannot be turned on/off using Auxiliary Input 1 – Can be turned on/off using Auxiliary Input	Allows the output to be turned on and off by a GPIO input.
SLEEPEN	0 – LSW6 stays on when the IC enters Sleep mode 1 – LSW6 turns off when the IC enters Sleep mode	
DPSLEEPEN	0 – LSW6 stays on when the IC enters DEEP SLEEP mode 1 – LSW6 turns off when the IC enters DEEP SLEEP mode	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LSW56_REG08 – LSW56 Configuration Register

Address = 0x58h	Default = 0x20h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	OFF DELAY [3:0]				RST	DBOK [2:0]		
Default	0010				0	000		
Access	R/W				R/W	R/W		

Name	Description	Notes
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.
RST	0 – LSW6 does not affect nRESET output 1 – LSW6 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LSW56_REG09 – LSW56 Configuration Register

Address = 0x59h	Default = 0x0Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				MODE	ON DELAY [2:0]		
Default	0000				1	110		
Access	R/W				R/W	R/W		

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.

LSW56_REG13 – LSW56 Configuration Register

Address = 0x5Dh	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	QLTCH LSW6	QLTCH LSW5	LSW6 ILIM SHUTDOWN DIS	LSW5 ILIM SHUTDOWN DIS	ILIM SET56 [1:0]		EN LOWVIN ILIM MODE	EN LSW ILIM COMPS
Default	0	0	0	0	00		0	0
Access	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Name	Description	Notes
QLTCH LSW6	0 – LS6 shuts down when its sequenced input shuts down 1 – LS6 stays on when its sequenced input shuts down	
QLTCH LSW5	0 – LS5 shuts down when its sequenced input shuts down 1 – LS5 stays on when its sequenced input shuts down	
LSW4 ILIM SHUTDOWN DIS	0 = Enables the LSW6 shutdown during current limit 1 = Disables the LSW6 shutdown during current limit	
LSW3 ILIM SHUTDOWN DIS	0 = Enables the LSW5 shutdown during current limit 1 = Disables the LSW5 shutdown during current limit	
ILIM SET56 [1:0]	Current limit settings for LSW56	
EN LOWVIN ILIM MODE	0 = Disabled low VIN mode when load switch input is the LSW5 shutdown during current limit 1 = Enable low VIN mode for using a low common mode voltage comparator.	
EN LSW ILIM COMPS	0 = Disabled LSW current limit comparator, lower quiescent current possible. 1 = Enable LSW current limit comparator.	

B1_REG00 – Buck1 Configuration Register

Address = 0x60h	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV_FLT	ILIM_FLT	ILIM_WARN	RFU[1:0]		ILIM_FLTMSK	RFU
Default	0	0	0	0	00		1	0
Access	RO	RO	RO	RO	RO		RO	RO

Name	Description	Notes
POK	0 = Buck1 voltage is below the power good threshold 1 – Buck1 voltage is above the power good threshold	Provides real-time power good status
OV_FLT	0 = Buck1 voltage is below the overvoltage threshold 1 – Buck1 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM_FLT	0 = Buck1 is below the ILIM threshold 1 – Buck1 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	0 = Buck1 is below the ILIM warn threshold 1 – Buck1 is above the ILIM warn threshold	Provides real-time current limit warning status
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ILIM_FLT_MSK	0 = Unmasks the Buck1 B1_ILIM register 1 = Masks the Buck1 B1_ILIM register	When 1, the B1_ILIM fault is masked from the master ILIM fault register. B1_ILIM still provides real-time current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG01 – Buck1 Configuration Register

Address = 0x61h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
RFU [7:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG02 – Buck1 Voltage Set0 Register

Address = 0x62h	Default = 0x98h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FSW [1:0]		VSET0 [5:0]					
Default	10		011000					
Access	R/W		R/W					

Name	Description	Notes
FSW [1:0]	Switching frequency settings 00 – 1.5 MHz 01 – 2.0 MHz 10 – 2.5 MHz 11 – 3.3 MHz	Check electrical tables for switching frequency values
VSET0 [5:0]	Buck1 output voltage setting in ACTIVE mode.	Controls the Buck1 output voltage in Active Mode. The output voltage is equal to 0.6V + VSET0 [5:0] *0.05V

B1_REG03 – Buck1 Voltage Set1 Register

Address = 0x63h	Default = 0xD8h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VFF RES SEL [1:0]		VSET1 [5:0]					
Default	11011000							
Access	R/W							

Name	Description	Notes
VFF RES SEL [1:0]	Resistor settings for ripple generator / compensation network. VFF RES SEL [2] in B1_REG07. 000 – 0.125 MΩ 001 – 0.25 MΩ 010 – 0.5 MΩ 011 – 0.75 MΩ 000 – 1.0 MΩ 001 – 1.25 MΩ 010 – 1.5 MΩ 011 – 2.0 MΩ	Tweaks response of the regulator by adjusting the ripple generation filter. See Active-Semi Design for operation. This typically should not change from CMI value.
VSET1 [5:0]	Buck1 output voltage setting in SLEEP, DPSLP, or DVS mode.	The output voltage is equal to 0.6V + VSET1 [5:0] *0.05V

B1_REG04 – Buck1 Configuration Register

Address = 0x64h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_STDN DIS	ILIM_SET
Default	1	1	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = Buck1 is enabled through normal sequencing routing 1 = Buck1 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	Do not change this bit
QLTCH	0 = Buck1 shuts down when its sequencing trigger input shuts down 1 = Buck1 stays on when its sequencing trigger input shuts down	
SLEEP EN	0 = Buck1 stays on when the IC enters Sleep mode 1 = Buck1 turns off when the IC enters Sleep mode	Provides real-time power good status
AUXIN EN	0 = Buck1 turn on/off cannot be controlled with auxiliary input. 1 = Buck1 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DP SLEEP EN	0 = Buck1 stays on when the IC enters DP SLEEP mode 1 = Buck1 turns off when the IC enters DP SLEEP mode	
ILIM_STDN_DIS	0 = Shut down is active 1 = Shut down is disabled	
ILIM_SET	0 = Low current limit setting ~0.6A peak 1 = High current limit setting ~1.2A peak	Check electrical tables for buck regulator for values

B1_REG05 – Buck1 Configuration Register

Address = 0x65h	Default = 0xC1h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	1	000			001		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	Do not change this bit
RST	0 – Buck 1 does not affect nRESET output 1 – Buck 1 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG06 – Buck1 Configuration Register

Address = 0x66h	Default = 0x04h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				DIS ILIM CBC	BURST SEL	DBSTBY [1:0]	
Default	0000				0	1	00	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit
DIS ILIM CBC	0 – Enable the cycle-by-cycle current limit. 1 – Disable the cycle-by-cycle current limit.	Option to disable the cycle-by-cycle current limit.
BURST SEL	0 – Select lower threshold for burst voltage comparator 1 – Select higher threshold for burst voltage comparator	Adjusts higher or lower voltage before detecting burst mode and skipping cycles for higher efficiency.
DBSTBY [1:0]	Determines startup sequencing from the CMI code	Do not change this bit

B1_REG07 – Buck1 Configuration Register

Address = 0x67h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VFF RES SEL [2]	ON DELAY [2:0]			OFF DELAY [3:0]			
Default	0	0			1000			
Access	R/W	R/W			R/W			

Name	Description	Notes
VFF RES SEL [2]	Resistor settings for ripple generator / compensation network. VFF RES SEL [1:0] in B1_REG03. 000 – 0.125 MΩ 001 – 0.25 MΩ 010 – 0.5 MΩ 011 – 0.75 MΩ 000 – 1.0 MΩ 001 – 1.25 MΩ 010 – 1.5 MΩ 011 – 2.0 MΩ	Tweaks response of the regulator by adjusting the ripple generation filter. See Active-Semi Design for operation. This typically should not change from CMI value.
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.

B2_REG00 – Buck2 Configuration Register

Address = 0x70h	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV_FLT	ILIM_FLT	ILIM_WARN	RFU[1:0]		ILIM_FLTMSK	RFU
Default	0	0	0	0	0		1	0
Access	RO	RO	RO	RO	RO		RO	RO

Name	Description	Notes
POK	0 = Buck2 voltage is below the power good threshold 1 – Buck2 voltage is above the power good threshold	Provides real-time power good status
OV_FLT	0 = Buck2 voltage is below the overvoltage threshold 1 – Buck2 voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM_FLT	0 = Buck2 is below the ILIM threshold 1 – Buck2 is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	0 = Buck2 is below the ILIM warn threshold 1 – Buck2 is above the ILIM warn threshold	Provides real-time current limit warning status
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ILIM_FLT_MSK	0 = Unmasks the Buck2 B2_ILIM register 1 = Masks the Buck2 B2_ILIM register	When 1, the B2_ILIM fault is masked from the master ILIM fault register. B2_ILIM still provides real-time current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG01 – Buck2 Configuration Register

Address = 0x71h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
RFU [7:0]	Reserved for future use	Not Used

B2_REG02 – Buck2 Voltage Set0 Register

Address = 0x72h	Default = 0x8Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FSW [1:0]		VSET0 [5:0]					
Default	10		001100					
Access	R/W		R/W					

Name	Description	Notes
FSW [1:0]	Switching frequency settings 00 – 1.5 MHz 01 – 2.0 MHz 10 – 2.5 MHz 11 – 3.3 MHz	Check electrical tables for switching frequency values
VSET0 [5:0]	Buck2 output voltage setting in ACTIVE mode.	Controls the Buck2 output voltage in Active Mode. The output voltage is equal to 0.6V + VSET0 [5:0] *0.05V

B2_REG03 – Buck2 Voltage Set1 Register

Address = 0x73h	Default = 0xCCh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VFF RES SEL [1:0]		VSET1 [5:0]					
Default	11001100							
Access	R/W							

Name	Description	Notes
VFF RES SEL [1:0]	Resistor settings for ripple generator / compensation network. VFF RES SEL [2] in B2_REG07. 000 – 0.125 MΩ 001 – 0.25 MΩ 010 – 0.5 MΩ 011 – 0.75 MΩ 000 – 1.0 MΩ 001 – 1.25 MΩ 010 – 1.5 MΩ 011 – 2.0 MΩ	Tweaks response of the regulator by adjusting the ripple generation filter. See Active-Semi Design for operation. This typically should not change from CMI value.
VSET2 [5:0]	Buck2 output voltage setting in SLEEP, DPSLP, or DVS mode.	Normal operation output voltage settings. VOUT = 0.6V + (VSET2 [5:0]*0.05V

B2_REG04 – Buck2 Configuration Register

Address = 0x74h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_STDN DIS	ILIM_SET
Default	1	1	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = Buck2 is enabled through normal sequencing routing 1 = Buck2 I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	Do not change this bit
QLTCH	0 = Buck2 shuts down when its sequencing trigger input shuts down 1 = Buck2 stays on when its sequencing trigger input shuts down	
SLEEP EN	0 = Buck2 stays on when the IC enters Sleep mode 1 = Buck2 turns off when the IC enters Sleep mode	Provides real-time power good status
AUXIN EN	0 = Buck2 turn on/off cannot be controlled with auxiliary input. 1 = Buck2 turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DP SLEEP EN	0 = Buck2 stays on when the IC enters DP SLEEP mode 1 = Buck2 turns off when the IC enters DP SLEEP mode	
ILIM_STDN_DIS	0 = Shut down is active 1 = Shut down is disabled	
ILIM_SET	0 = Low current limit setting ~0.6A peak 1 = High current limit setting ~1.2A peak	Check electrical tables for buck regulator for values

B2_REG05 – Buck2 Configuration Register

Address = 0x75h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	000			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	Do not change this bit
RST	0 – Buck 1 does not affect nRESET output 1 – Buck 1 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG06 – Buck2 Configuration Register

Address = 0x76h	Default = 0x05h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				DIS ILIM CBC	BURST SEL	DBSTBY [1:0]	
Default	0000				0	1	01	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit
DIS ILIM CBC	0 – Enable the cycle-by-cycle current limit. 1 – Disable the cycle-by-cycle current limit.	Option to disable the cycle-by-cycle current limit.
BURST SEL	0 – Select lower threshold for burst voltage comparator 1 – Select higher threshold for burst voltage comparator	Adjusts higher or lower voltage before detecting burst mode and skipping cycles for higher efficiency.
DBSTBY [1:0]	Determines startup sequencing from the CMI code	Do not change this bit

B2_REG07 – Buck2 Configuration Register

Address = 0x77h	Default = 0x17h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VFF RES SEL [2]	ON DELAY [2:0]			OFF DELAY [3:0]			
Default	0	001			0111			
Access	R/W	R/W			R/W			

Name	Description	Notes
VFF RES SEL [2]	Resistor settings for ripple generator / compensation network. VFF RES SEL [1:0] in B2_REG03. 000 – 0.125 MΩ 001 – 0.25 MΩ 010 – 0.5 MΩ 011 – 0.75 MΩ 000 – 1.0 MΩ 001 – 1.25 MΩ 010 – 1.5 MΩ 011 – 2.0 MΩ	Tweaks response of the regulator by adjusting the ripple generation filter. See Active-Semi Design for operation. This typically should not change from CMI value.
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.

BOOST_REG00 – Boost Configuration Register

Address = 0x80h	Default = 0x07h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_PD	BST_ILIM_WARN	BST_OV	BST_UV	RFU	BST_ILIM_WARN_MASK	BST_OV_MASK	BST_UV_MASK
Default	0	0	0	0	0	1	1	1
Access	R/W	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
EN_PD	0 – Disable pull down resistor from VBST. 1 – Enable pull down resistor from VBST.	This function active only when the Boost was turned off.
BST_ILIM_WARN	0 – Low side current of Boost is below the ILIM_WARNING Threshold. 1 - Low side current of Boost is above the ILIM_WARNING Threshold.	Provides real-time current limit status.
BST_OV	0 – Output voltage of Boost is below the Over Voltage Threshold. 1 - Output voltage of Boost is above the Over Voltage Threshold.	Provides real-time over voltage status.
BST_UV	0 – Output voltage of Boost is below the Power Good Voltage Threshold. 1 - Output voltage of Boost is above the Power Good Voltage Threshold.	Provides real-time power good voltage status.
RFU	Reserved for future use	Can write to this register, but it always returns a 0 when read.
BST_ILIM_WARN_MASK	0 – Unmasks the BST_ILIM_WARN register. 1 – Masks the BST_ILIM_WARN register.	When 1, the BST_ILIM_WARN_MASK fault bit is masked from the master ILIM warning register. BST_ILIM_WARN_MASK still provides real-time ILIM warning status.
BST_OV_MASK	0 – Unmasks the BST_OV register. 1 – Masks the BST_OV register	When 1, the BST_OV_MASK fault bit is masked from the master over voltage register. BST_OV_MASK still provides real-time over voltage status.
BST_UV_MASK	0 – Unmasks the BST_UV register. 1 – Masks the BST_UV register	When 1, the BST_UV_MASK fault bit is masked from the master under voltage register. BST_UV_MASK still provides real-time under voltage status.

BOOST_REG01 – Boost Configuration Register

Address = 0x81h	Default = 0x1Ch	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS_FAULTS	DISCC	LED BOOST REG VSET [5:0]					
Default	0	0	011100					
Access	R/W	R/W	R/W					

Name	Description	Notes
DIS_FAULTS	0 – Enable the Boost shutdown when meet faults. 1 – Disable the Boost shutdown when meet faults.	Do not change this bit.
DISCC	0 – Boost works as normal which include Constant current and Constant voltage mode. 1 – Boost works at constant voltage mode only, the ISNS pin works at sink current mode.	
LED BOOST REG VSET [5:0]	Boost output voltage setting in ACTIVE mode.	Controls the Boost output voltage in Active Mode. The output voltage is equal to VOUT = VOUT = 5V + VSET [5:0] *0.25V

BOOST_REG02 – Boost Configuration Register

Address = 0x82h	Default = 0x20h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS ILIM2 TURN OFF	CC_ADJ	LED_BOOST ISET [5:0]					
Default	0	0	100000					
Access	R/W	R/W	R/W					

Name	Description	Notes
DIS ILIM2 TURN OFF	0 – Enable the Boost shutdown during low side over current faults. 1 – Disable the Boost shutdown during low side over current faults	Do not change this bit.
CC_ADJ	0 – More stable when use more than 4LEDs. 1 – Faster response when use less than 3LEDs	Do not change this bit.
LED_BOOST ISET [5:0]	Normal operation output current settings. IOUT = (ISET [5:0] code in decimal) *0.625mA	Check Boost output current table.

BOOST_REG03 – Boost Configuration Register

Address = 0x83h	Default = 0x50h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP_EN	AUXIN_EN	ONDEL [2:0]		
Default	0	1	0	1	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
ON	0 = Boost is enabled through normal sequencing routing 1 = Boost I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	Do not change this bit
QLTCH	0 = Boost shuts down when its sequencing trigger input shuts down 1 = Boost stays on when its sequencing trigger input shuts down	
SLEEP_EN	0 = Boost stays on when the IC enters Sleep mode 1 = Boost turns off when the IC enters Sleep mode	Provides real-time power good status
AUXIN_EN	0 = Boost turn on/off cannot be controlled with auxiliary input. 1 = Boost turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
ONDEL [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.

BOOST_REG04 – Boost Configuration Register

Address = 0x84h	Default = 0xC0h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	DP SLEEP EN	DBQL [2:0]			DBOK [2:0]		
Default	1	1	000			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DP SLEEP EN	0 = Buck1 stays on when the IC enters DP SLEEP mode 1 = Buck1 turns off when the IC enters DP SLEEP mode	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

BOOST_REG05 – Boost Configuration Register

Address = 0x85h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				OFF DELAY [3:0]			
Default	0000				0000			
Access	R/W				R/W			

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	Do not change this bit
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.

BB_REG00 – Buck-Boost Configuration Register

Address = 0x90h	Default = 0x02h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV_FLT	ILIM_FLT	ILIM_WARN	RFU[1:0]		ILIM_FLTMSK	RFU
Default	0	0	0	0	0		1	0
Access	RO	RO	RO	RO	RO		RO	RO

Name	Description	Notes
POK	0 = Buck-Boost voltage is below the power good threshold 1 – Buck-Boost voltage is above the power good threshold	Provides real-time power good status
OV_FLT	0 = Buck-Boost voltage is below the overvoltage threshold 1 – Buck-Boost voltage is over the overvoltage threshold	Provides real-time overvoltage status
ILIM_FLT	0 = Buck-Boost is below the ILIM threshold 1 – Buck-Boost is above the ILIM threshold	Provides real-time current limit status
ILIM_WARN	0 = Buck-Boost is below the ILIM warn threshold 1 – Buck-Boost is above the ILIM warn threshold	Provides real-time current limit warning status
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ILIM_FLT_MSK	0 = Unmasks the Buck-Boost BB_ILIM register 1 = Masks the Buck-Boost BB_ILIM register	When 1, the BB_ILIM fault is masked from the master ILIM fault register. BB_ILIM still provides real-time current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

BB_REG01 – Buck-Boost Configuration Register

Address = 0x91h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
RFU [7:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

BB_REG02 – Buck-Boost Voltage Set0 Register

Address = 0x92h	Default = 0x64h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FSW [1:0]		VSET0 [5:0]					
Default	01		100100					
Access	R/W		R/W					

Name	Description	Notes
FSW [1:0]	Switching frequency settings 00 – 1.5 MHz 01 – 2.0 MHz 10 – 2.5 MHz 11 – 3.3 MHz	Check electrical tables for switching frequency values
VSET0 [5:0]	Buck-boost output voltage setting in ACTIVE mode.	Controls the Buck-boost output voltage in Active Mode. The output voltage is equal to VOUT = 3.2V + VSET0 [5:0] *0.05V, up to a max of 5.55V

BB_REG04 – Buck-Boost Configuration Register

Address = 0x94h	Default = 0xC4h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBINEN	QLTCH	SLEEP EN	AUXIN EN	DP SLEEP EN	ILIM_STDN DIS	ILIM_SET
Default	1	1	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 = Buck-Boost is enabled through normal sequencing routing 1 = Buck-Boost I2C enable bit that bypasses normal sequencing	
PBINEN	0 – Does not respond to push button mode 1 – Responds to turn on automatically with push button input.	Do not change this bit
QLTCH	0 = Buck-Boost shuts down when its sequencing trigger input shuts down 1 = Buck-Boost stays on when its sequencing trigger input shuts down	
SLEEP EN	0 = Buck-Boost stays on when the IC enters Sleep mode 1 = Buck-Boost turns off when the IC enters Sleep mode	Provides real-time power good status
AUXIN EN	0 = Buck-Boost turn on/off cannot be controlled with auxiliary input. 1 = Buck-Boost turn on/off can be controlled with auxiliary input.	Control bit to use internal gb_aux line as control input for turn on/off.
DP SLEEP EN	0 = Buck-Boost stays on when the IC enters DP SLEEP mode 1 = Buck-Boost turns off when the IC enters DP SLEEP mode	
ILIM_STDN_DIS	0 = Shut down is active 1 = Shut down is disabled	
ILIM_SET	Not used in BB	Check electrical tables for BB regulator for values

BB_REG05 – Buck-Boost Configuration Register

Address = 0x95h	Default = 0x80h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	000			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck 1 does not affect nRESET output 1 – Buck 1 POK affects nRESET output	RST bit determines if the regulator power okay (POK) signal is required to go high before the nRESET output from the PMIC can assert.
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

BB_REG06 – Buck-Boost Configuration Register

Address = 0x96h	Default = 0x0Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				RFU[1:0]		DBSTBY [1:0]	
Default	0000				11		00	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
Dis_toff_extended	Should be set to 1, this is an internal Active-Semi evaluation option	
DBSTBY [1:0]	Determines startup sequencing from the CMI code	Do not change this bit

BB_REG07 – Buck-Boost Configuration Register

Address = 0x97h	Default = 0xA6h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VFF RES SEL [2]	ON DELAY [2:0]			OFF DELAY [3:0]			
Default	1	010			0110			
Access	R/W	R/W			R/W			

Name	Description	Notes
VFF RES SEL [2]	Resistor settings for ripple generator / compensation network. VFF RES SEL [1:0] in BB_REG03. 000 – 0.125 MΩ 001 – 0.25 MΩ 010 – 0.5 MΩ 011 – 0.75 MΩ 000 – 1.0 MΩ 001 – 1.25 MΩ 010 – 1.5 MΩ 011 – 2.0 MΩ	Tweaks response of the regulator by adjusting the ripple generation filter. Note this is used for Buck Type 1 mode only. A separate control is typically used for the BB. Consult the Active Design team for additional information
ON DELAY [2:0]	Sets the delay time during power on sequence following the trigger to turn on the regulator.	Programs the delay time between the regulators trigger and the actual regulator startup.
OFF DELAY [3:0]	Controls OFF Delay during power off	See off delay settings in data sheet.

APLC_REG00 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC0h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	VIN_OV	VIN_UV	VINOK	VBAT LOW	No use	Q2ILIM PROT	Q1ILIM	SUSPEND
Default	0	0	1	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
VIN_OV	0: Not OV, 1: OV	
VIN_UV	0: not UV; 1: UV	
VINOK	VINOK =! (VIN_UV+VIN_OV+ (IN<BAT+200mV))	
VBAT LOW	0: VBAT is higher than VBAT short threshold 1: VBAT is lower than VBAT short threshold	
Not used		
Q2ILIM_PROT	0: current below Q2 ILIM 1: Q2 ILIM regulation loop is active. There are some things wrong with external RISET.	
Q1ILIM	0: current below ILIM 1: ILIM regulation loop is active	
SUSPEND	0: Charger Status as APLC_REG01<2:0> 1: Charger routine is suspended because battery temperature run out of safety range (& charge current = 0).	

APLC_REG01 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC1h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	BAT_TEMP [2:0]			BAT SUP MODE	BAT DETECTED	BAT CHG STATUS [2:0]		
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
BAT_TEMP [2:0]	0: Below 0 1: 0 to 10 2: 10 to 45 3: 45 to 50 4: 50 to 60 5: Over 60 6: Not used 7: Not used	
BAT_SUP_MODE	0 = Battery is not in supplement mode 1 = Battery is in supplement mode	
BAT_DETECTED	0 = Battery is not detected 1 = Battery is detected	
BAT CHG STATUS [2:0]	000 = Exit Charge 001 = Reset Mode 010 = VBAT SHORT Mode 011 = VBAT PRECOND Mode 100 = Fast Charge CC loop on 101 = Fast Charge CC loop off & CV loop on 110 = End of Charge Mode 111 = Fault Mode	

APLC_REG02 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC2h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	VCHGINx STAT	BAT STAT	CHG STAT CHANGE	VBAT LOW STAT	BAT TEMP STAT	THERMAL LOOP ACTIVE	FAULT STAT	SFTY TIMER EXPIRED
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
VCHGINx_STAT	0 = The charging status has not changed since last read 1 = The charging status has changed since last read	
BAT_STAT	0 = The battery detection status has not changed since the last read 1 = The battery detection status has changed since the last read	
CHG_STAT_CHANGE	0 = The changer status has not changed since the last read 1 = The charger status has changed since the last read	
VBAT LOW STAT	0 = VBAT is higher than VBAT short threshold 1 = VBAT is lower than VBAT short threshold.	
BAT_TEMP_STAT	0 = Battery temperature has not changed from IN RANGE to OUT RANGE or from OUT RANGE to IN RANGE 1 = Battery temperature has changed either from IN RANGE to OUT RANGE or from OUT RANGE to IN RANGE Notes: BAT_TEMP_STAT flag only be set when charging has started	
THERMAL_LOOP_ACTIVE	0 = The battery charger thermal loop is not active 1 = The battery charger thermal loop is active	
FAULT_STAT	0 = No faults since last read 1 = A fault has occurred since the last read	
SFTY_TIMER_EXPIRED	0 = The safety charger timer has not expired 1 = The safety charger timer has expired	

APLC_REG03 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC3h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INT CHG STAT INRG MASK	INT BAT DETECT MASK	INT CHG STAT MASK	VBAT LOW MASK	INT BAT TEMP INRG MASK	INT THERMAL LOOP MASK	INT FAULT MASK	PRECOND SFTY TIMER MASK
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
INT_CHGSTAT_INRG_MASK	0 = UNMASK 1 = MASK the flag status when Charger Input is jump into OK Range (VINOK from 0 -> 1)	
INT_BAT_DETECT_MASK	0 = UNMASK 1 = MASK	
INT_CHG_STAT_MASK	0 = UNMASK 1 = MASK	
VBAT LOW MASK	0 = UNMASK 1 = MASK	For MASK: need set both APLC_REG03[4] and APLC_REG04[4] to 1. If any of these bit is 0, then not MASK
INT_BATTEMP_INRG_MASK	0 = UNMASK 1 = MASK the interrupt when Battery jump into temperature range which allow charging	
INT_THERMAL_LOOP_MASK	0 = UNMASK 1 = MASK the thermal loop interrupt (Thermal loop active whenever dice temperature > 120oC)	
INT_FAULT_MASK	Use to mask fault interrupt 0 = UNMASK 1 = MASK	Fault interrupt including: BAT_OV, Over-Temperature Fault, Safety Timer Expired OR Charge current reach to internal limit level (1.2A for fast-charge & 240mA when BAT_LOW)
PRECOND_SFTY_TIMER_MASK	0 = UNMASK 1 = MASK	Use to mask Precondition OR trickle charge safety time-out interrupt

APLC_REG04 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC4h	Default = 0x9Dh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INT CHG STAT OUTRG MASK	RFU[1:0]		VBAT LOW MASK	INT BAT TEMP OUTRG MASK	INT JEITA THRM FLDBLOOP MASK	RFU	FSTCHG SFTY TIMER MASK
Default	1	00		1	1	1	0	1
Access	R/W	R/W		R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
INT_CHGSTAT_OUTRG_MASK	0 = UNMASK 1 = MASK the flag status when Charger Input is out of OK Range (VINOK from 1 -> 0)	
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VBAT LOW MASK	0 = UNMASK 1 = MASK	For MASK: need set both APLC_REG03[4] and APLC_REG04[4] to 1. If any of these bit is 0, then not MASK
INT_BATTEMP_OUTRG_MASK	0 = UNMASK 1 = MASK the interrupt when Battery jump out of temperature range which disable charging	
INT_JEITA_THRM_FLDBLOOP_MASK	0: allow JEITA FOLDBACK current function calling interrupt (If bit JEITA COOL FOLDBACK EN = 1). 1: MASK the interrupt	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
FSTCHG_SFTY_TIMER_MASK	Use to mask fast-charge safety time-out interrupt 0 = UNMASK 1 = MASK	

APLC_REG05 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC5h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	RFU	RFU	CLR FLT TIMER	FLT TIMER PAUSE
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
CLR_FLT_TIMER	Write 1 to the register bit to clear any time out faults. This bit is automatic reset to 0	
FLT_TIMER_PAUSE	0 = Charger fault timer operates normally 1 = Pauses the fault timer counter	

APLC_REG06 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC6h	Default = 0x89h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VPRE [3:0]				IPRE [1:0]		EN_AUXIN	CHG_EN
Default	1	0	0	0	1	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
VPRE [3:0]	Precondition voltage setting: VPRE_CHG_VOLTAGE = 2.7V + 50mV* VPRE [3:0]	BAT_LOW threshold
IPRE [1:0]	Use to set precondition charge current. It is scale of fast charge current (0 = 20%, 1=15%, 2=10%, 3=5%).	
EN_AUXIN	0 = Disable VINOK control gb_auxin 1 = Enable VINOK control gb_auxin	
CHG_EN	0 = Disable charger 1 = Enable charger when VIN_OK	

APLC_REG07 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC7h	Default = 0x37h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DIS THERM REG	VDCCC [1:0]		VTERM [4:0]				
Default	0	0	1	1	0	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
DIS_THERM_REG	0 = Die Thermal regulation enabled 1 = Die Thermal regulation disabled	
VDCCC [1:0]	“Input voltage low” regulation setting. 0= Disable, 1=4.25V, 2=4.5V, 3 = 4.75V	
VTERM [4:0]	Charge termination voltage setting: VBAT_TERM_VOLTAGE = 3.9V + 20mV*VTERM [4:0]	

APLC_REG08 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC8h	Default = 0x52h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VSYS [1:0]		IN_ILIM [1:0]		VIN_STRT_DLY [1:0]		ITERM [1:0]	
Default	0	1	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
VSYS [1:0]	Output system voltage regulation from VIN: 0= BYPASS, 1=4.8V, 2=5.0V, 3=5.4V	
IN_ILIM [1:0]	VIN current limit setting 0=0.5A, 1=1A, 2=1.5A, 3=2A	
VIN_STRT_DLY [1:0]	Start Delay to start charging after enabled (Dig will give a signal become high this period to do the automation offset adjust): 00: 64ms 01: 220msec 10: 500msec 11: 1.3sec	
ITERM [1:0]	CHG ITERM CURRENT (0 = 20% of IFCHG, 1 = 15% of IFCHG, 2=10% of IFCHG, 3=5% of IFCHG)	Charge routine will finish after (VBAT > 96.5% && Ichg < ITERM && 750ms qualification time-out)

APLC_REG09 – Active Path Linear Charger (APLC) Configuration Register

Address = 0xC9h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	CORD COMP SETTING [2:0]			BAT_RECHG THRESHOLD		I_TRICKLE SET	V_TRICKLE [1:0]	
Default	0	0	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
CORD COMP SETTING [2:0] (default 000 = off)	Cord Compensation Level Setting: 000 = OFF; 001= 100mV/A; 010=150mV/A; 011=200mV/A; 100=250mV/A; 101=300mV/A; 110=350mV/A; 111=400mV/A	
BAT_RECHG_THRESHOLD	Battery re-charge threshold 00 = VTERM<4:0> - 80mV 01 = VTERM<4:0> - 120mV 10 = VTERM<4:0> - 160mV 11 = VTERM<4:0> - 200mV	
I_TRICKLE_SET	Trickle charge current setting 0 = 10mA 1 = 25mA	
V_TRICKLE [1:0]	Trickle charge voltage setting 0 = 2.0V, 1 = 2.2V, 2=2.4V, 3=2.5V	BAT_SHORT threshold

Referenced Documents

The reference documents below take precedence over the contents of this application note and should always be consulted for the latest information.

ACT81460 Data Sheet

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice

The information contained in this Data Sheet and any associated documents ("Data Sheet Information") is believed to be reliable; however, Qorvo makes no warranties regarding the Data Sheet Information and assumes no responsibility or liability whatsoever for the use of said information. All Data Sheet Information is subject to change without notice. Customers should obtain and verify the latest relevant Data Sheet Information before placing orders for Qorvo® products. Data Sheet Information or the use thereof does not grant, explicitly, implicitly or otherwise any rights or licenses to any third party with respect to patents or any other intellectual property whether with regard to such Data Sheet Information itself or anything described by such information.

DATA SHEET INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Without limiting the generality of the foregoing, Qorvo® products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death. Applications described in the Data Sheet Information are for illustrative purposes only. Customers are responsible for validating that a particular product described in the Data Sheet Information is suitable for use in a particular application.