QPA1314D

13.75 – 14.5 GHz 55 Watt GaN Power Amplifier

Product Overview

Qorvo's QPA1314D is a high power MMIC amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). QPA1314D is targeted to the 13.75-14.5 GHz Satcom band. Linear power is 20 W with 25 dBc third order intermodulation distortion products. It provides 55 W of saturated output power with 22.5 dB of large signal gain while achieving 37% power-added efficiency. Operating frequency can extend to 12.75 – 15.35 GHz if desired.

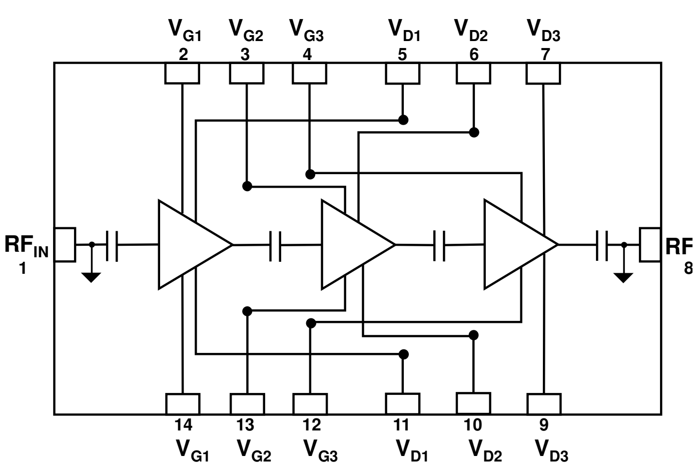
To simplify system integration, the QPA1314D is fully matched to 50 ohms with DC grounded I/O ports for optimum ESD performance. Also, there are on-chip blocking capacitors following the DC grounds on the input and output ports.

The QPA1314D is ideal for supporting communications and radar applications in both commercial and military markets.

The QPA1314D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant

Functional Block Diagram



Key Features

- Frequency Range: 13.75 – 14.5 GHz
- Extended Frequency Range: 12.75 – 15.35 GHz
- P_{SAT} (P_{IN} = 25 dBm): 47.5 dBm
- PAE (P_{IN} = 25 dBm): 37 %
- IM3 (P_{OUT}/Tone = 40 dBm): -25 dBc
- Small Signal Gain: 29 dB
- Bias: V_D = +24 V, I_{D12} = 168 mA, I_{D3} = 512 mA
  V_G = -2.3 V typ range.
- Die Dimensions: 4.78 x 6.71 x 0.10 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Applications

- Satellite Communications
- Datalinks

Ordering Information

Part No.	Description
QPA1314D	55 Watt GaN PA
QPA1314DEVB	Evaluation Board for QPA1314D

Absolute Maximum Ratings

Parameter	Value / Ra
Drain Voltage (V_D)	29.5 V
Gate Voltage Range (V_G)	-6 V to 0 V
Drain Current (I_{D1})	0.96 A
Drain Current (I_{D2})	1.96 A
Drain Current (I_{D3})	7.56 A
Drain Current (I_{D_TOTAL})	10.48 A
Gate Current (I_G)	See p. 25
Power Dissipation (P_{DISS}), 85 °C	130 W
Input Power (P_{IN}), 50 Ω, CW, V_D = 24 V, I_{D12} = 228 mA, I_{D3} = 512 mA, T_{BASE} = 85 °C	31 dBm
Input Power (P_{IN}), 3:1 VSWR, CW, V_D = 24 V, I_{D12} = 228 mA, I_{D3} = 512 mA, T_{BASE} = 85 °C	31 dBm
Mounting Temperature (30 seconds)	320 ºC
Storage Temperature	-55 to +150

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)		24	24	V
Drain Current, Quiescent (I_{D12})		168		mA
Drain Current, Quiescent (I_{D3})		512		mA
Drain Current, RF (I_{D_Drive} Total)	See plot page 4,6,9,12			mA
Gate Voltage Typ. Range (V_G)	–1.7 to -2.9			V
Gate Current, RF (I_{G_Drive})	See plot page 5,6			mA
Input Power @ Saturation, (P_{IN})*	T_{BASE} -40°C: 25			dBm
	T_{BASE} +25°C: 25			
	T_{BASE} +85 °C: 29			
Operating Temp. Range (T_{BASE}*)	–40		+85	ºC

* See plots page 7
T_{BASE} is back side of 20 mil CuMo carrier plate with AuSn solder

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

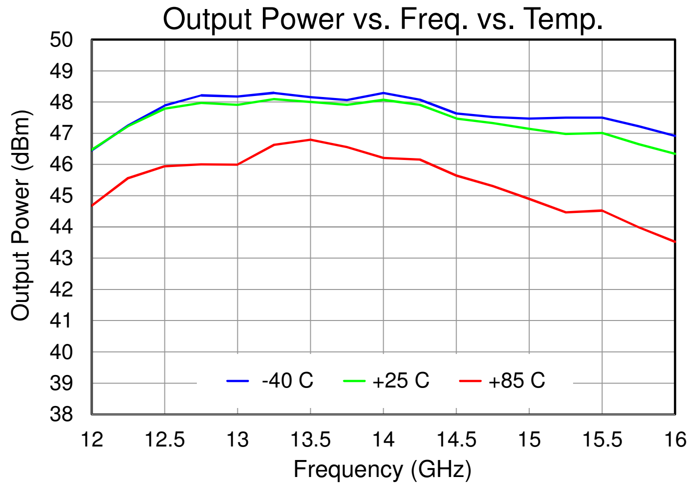
Parameter	Conditions (1) (2)	Min	Typ.	Max	Units
Operational Frequency Range		13.75		14.5	GHz
Output Power at Saturation, P_{SAT}	P_{IN} = 25 dBm, Frequency = 12.75 – 13.75 GHz (3)	47	48		dBm
	P_{IN} = 25 dBm, Frequency = 13.75 – 14.5 GHz	46.7	47.5		
	P_{IN} = 25 dBm, Frequency = 14.5 – 15.35 GHz (3)	45	47		
Power Added Efficiency, PAE	P_{IN} = 25 dBm		37		%
Large Signal Gain	P_{IN} = 25 dBm		22.5		dB
3RD Intermodulation Products, IM3	P_{OUT}/Tone = 40 dBm		-25		dBc
5RD Intermodulation Products, IM5			-40		
Small Signal Gain, S21	P_{IN} = -30 dBm		29		dB
Input Return Loss, IRL			20		
Output Return Loss, ORL			7		
P_{SAT} Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC; P_{IN} = 25 dBm		-0.04		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = 25 ºC to 85 ºC		-0.10		dB/ºC

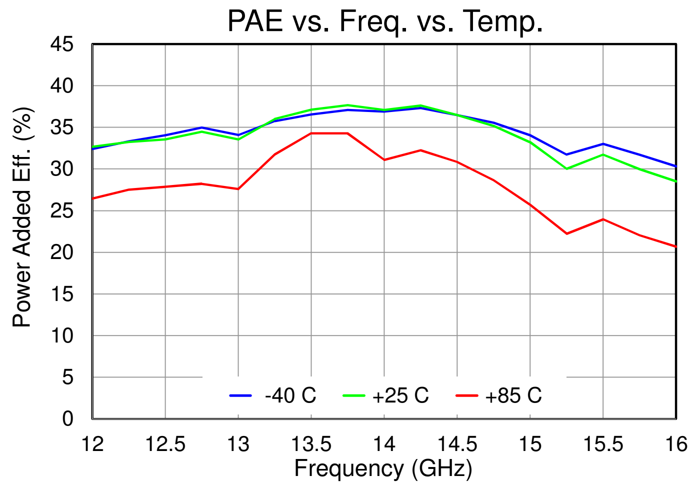
Notes:

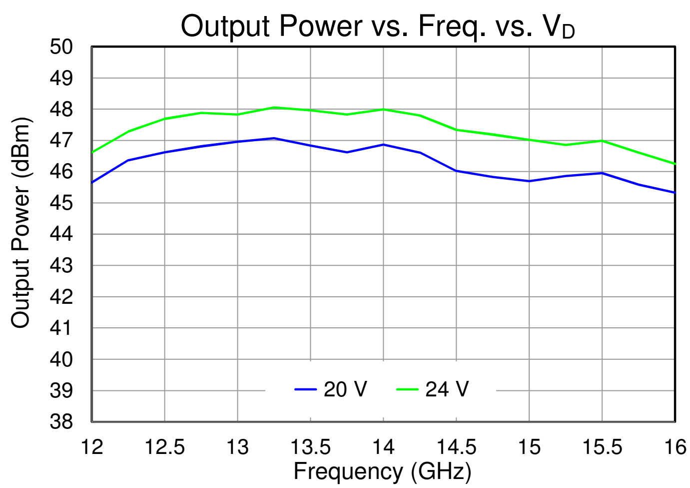
1. Test conditions unless otherwise noted: CW, V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA, V_G = -2.3 V +/- 0.6V typical, T_{BASE} = +25ºC, Z_0 = 50 Ω
2. T_{BASE} is back side of 20 mil CuMo carrier plate with AuSn die attached
3. Extended frequency range

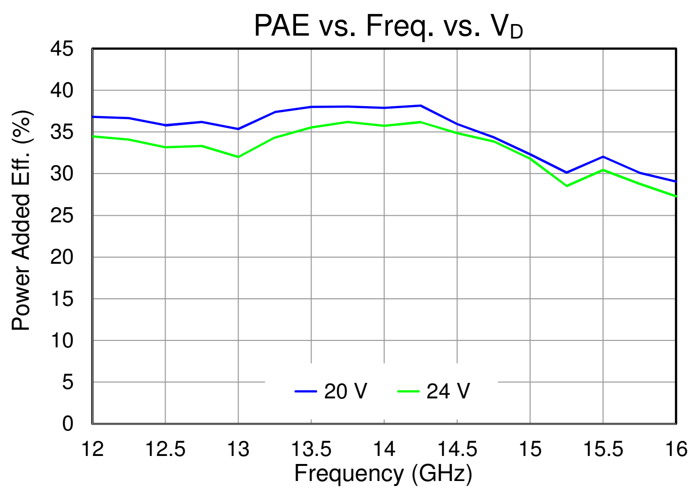
Performance Plots – Large Signal

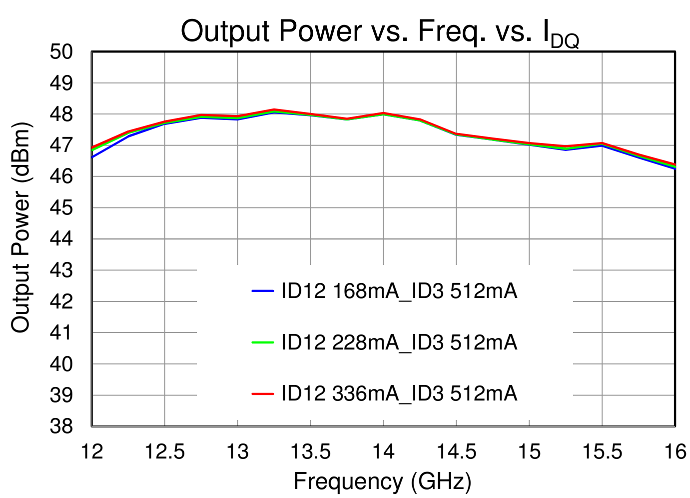
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA, P_{IN} = 25 dBm, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)

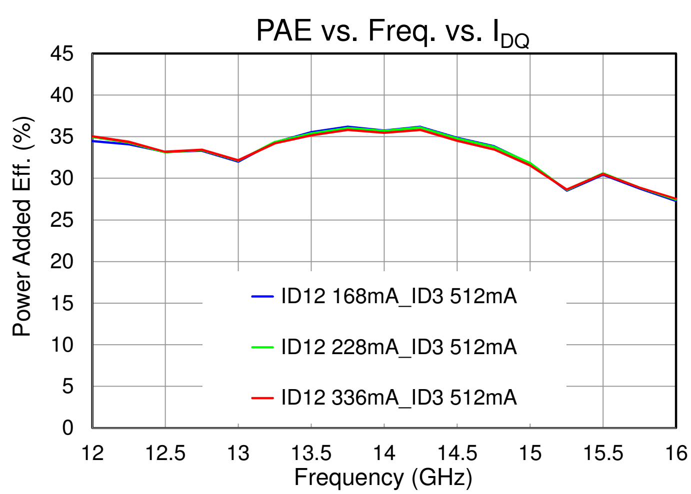






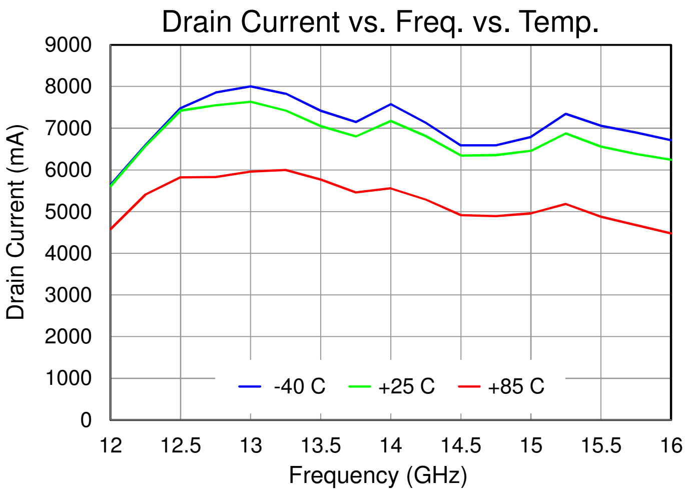


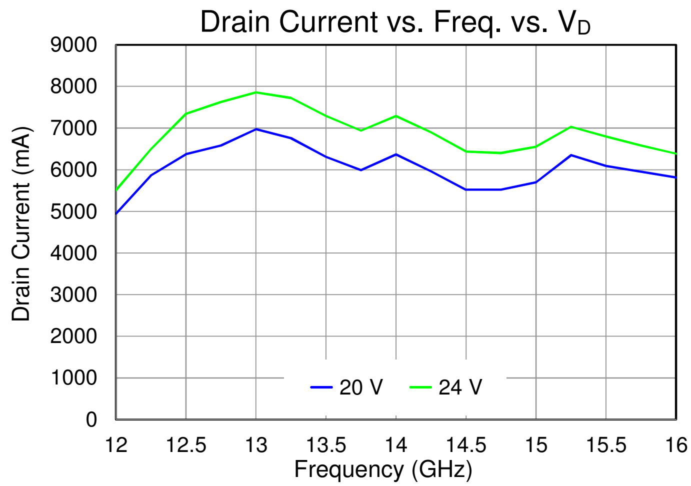


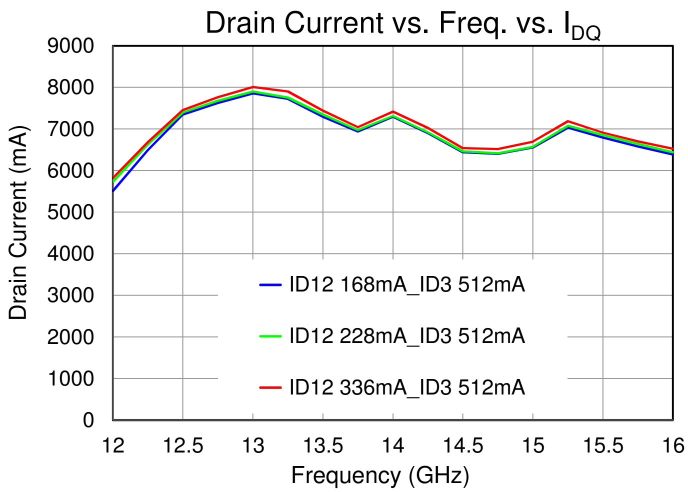


Performance Plots – Large Signal

Test conditions, unless otherwise noted: **CW,** V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA, P_{IN} = 25 dBm, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)







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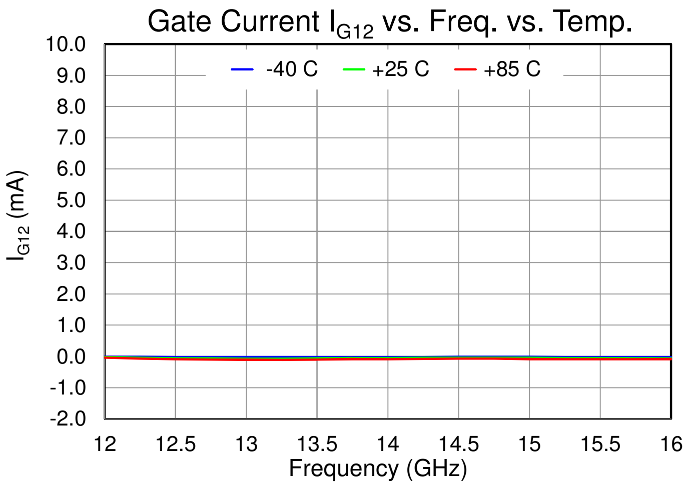

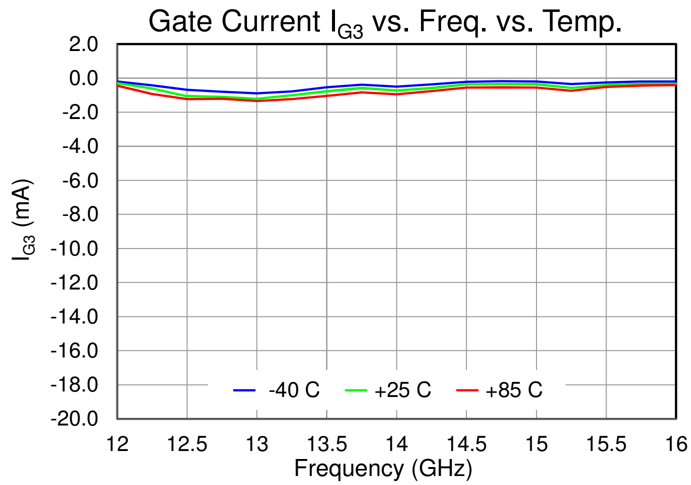

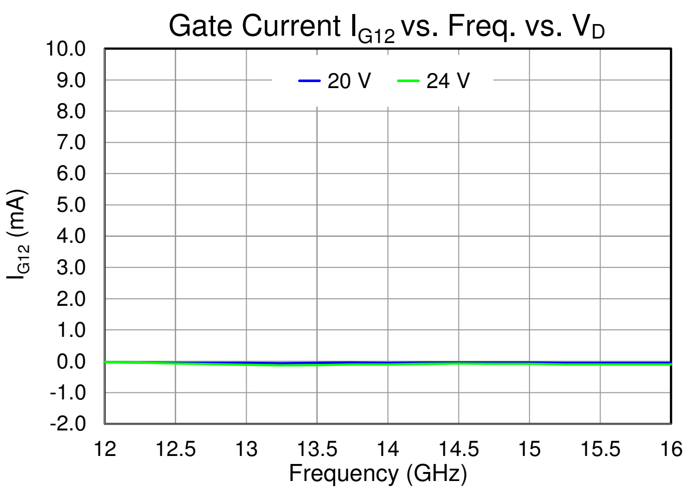

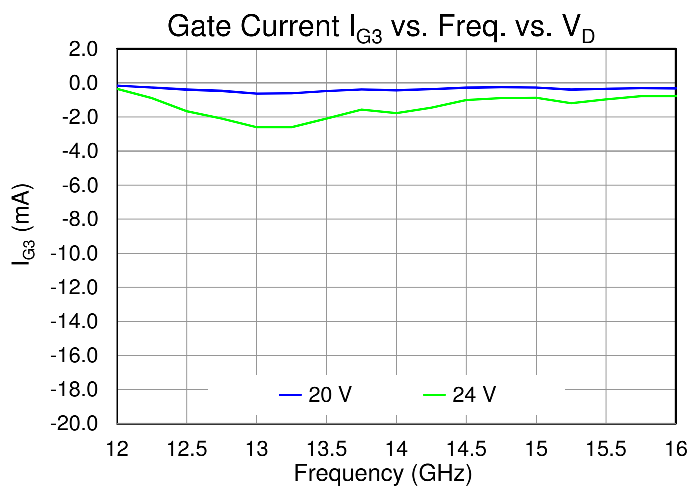

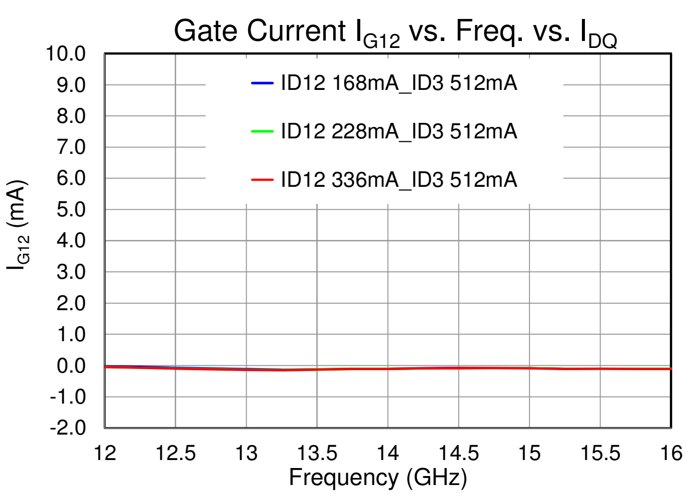

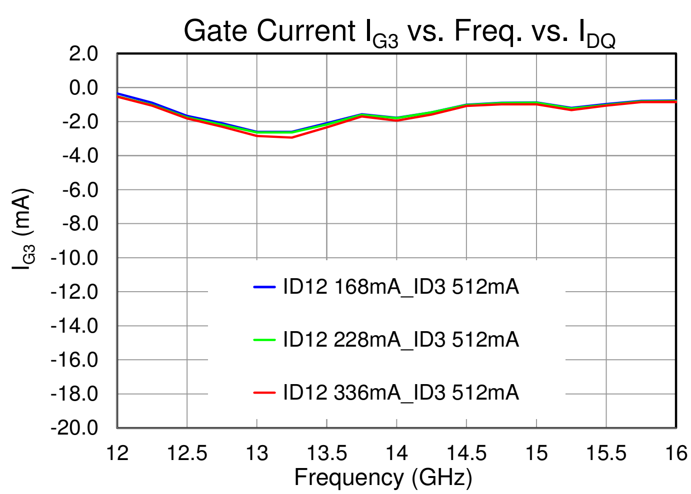

Performance Plots – Large Signal

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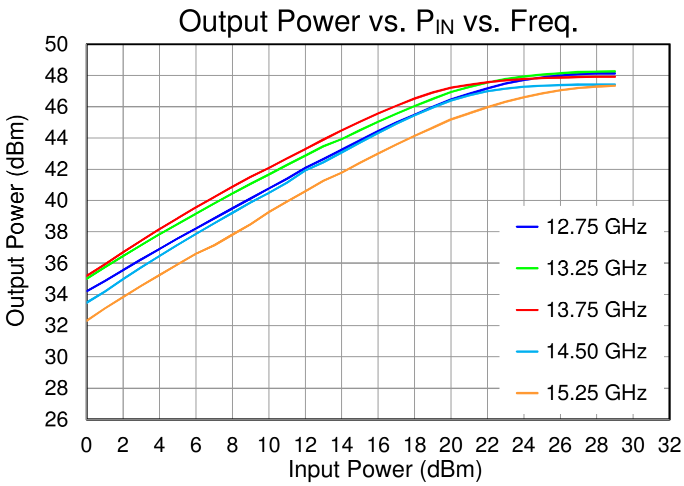

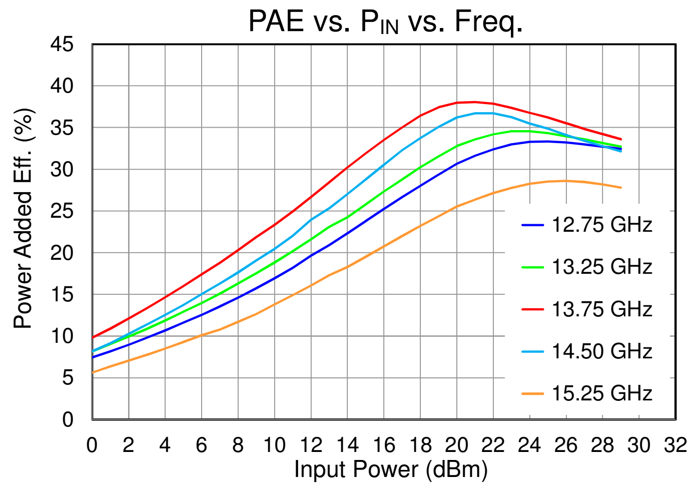

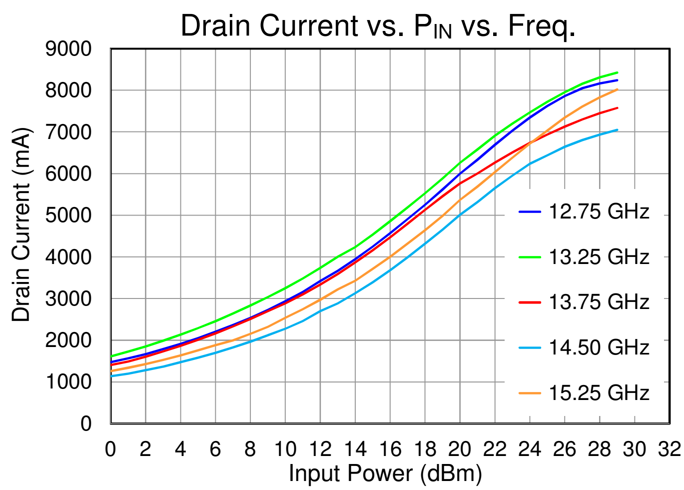

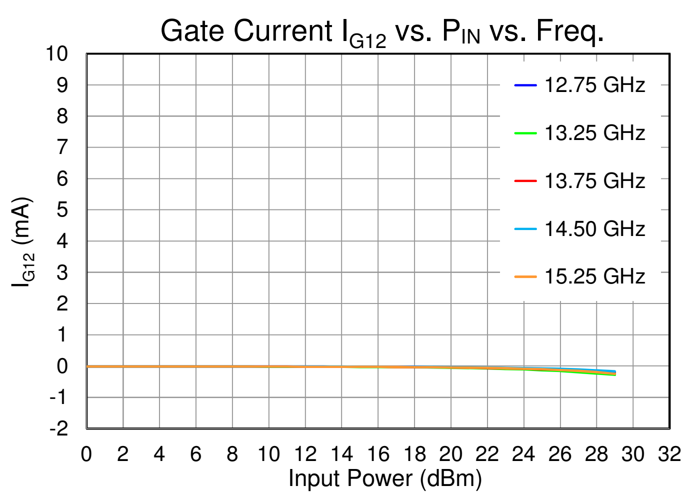

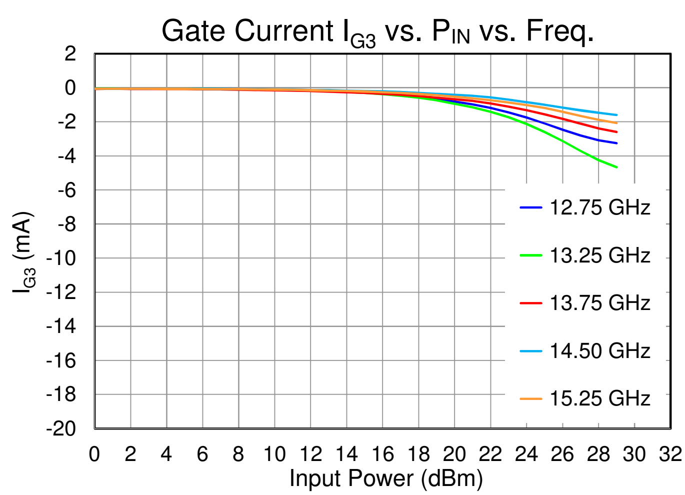

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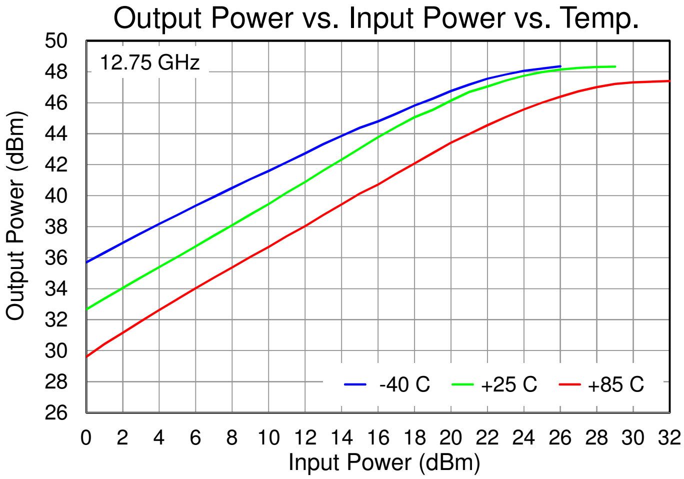

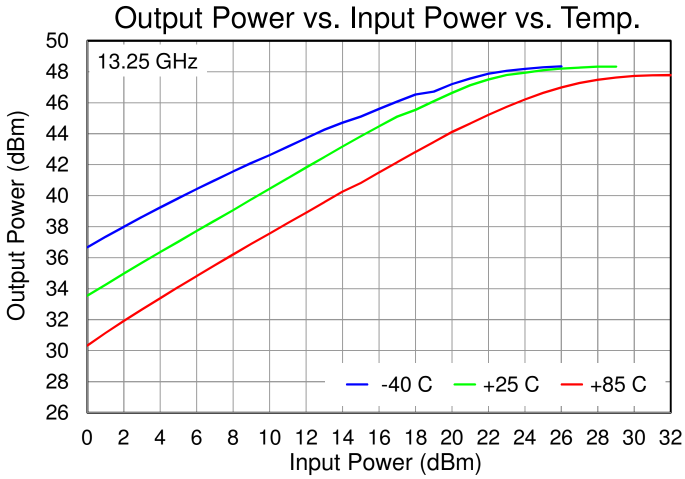

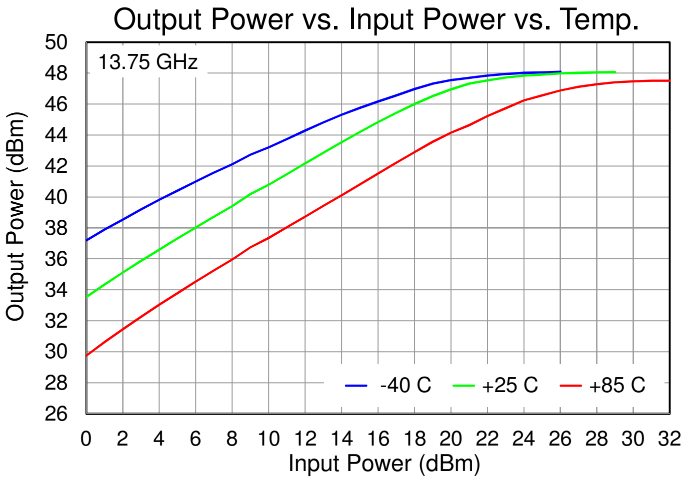

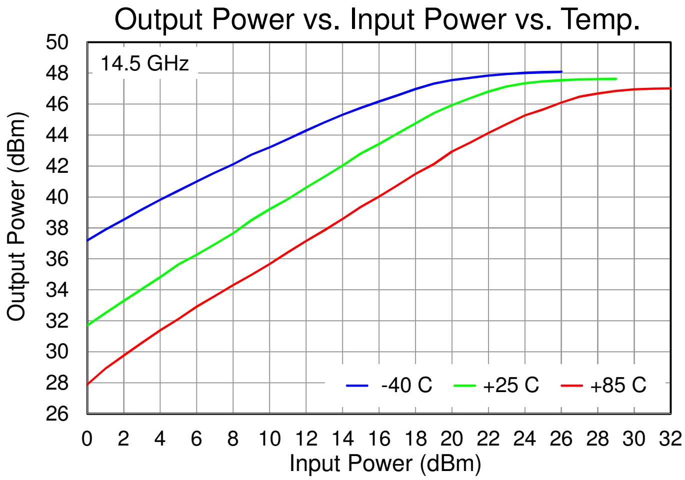

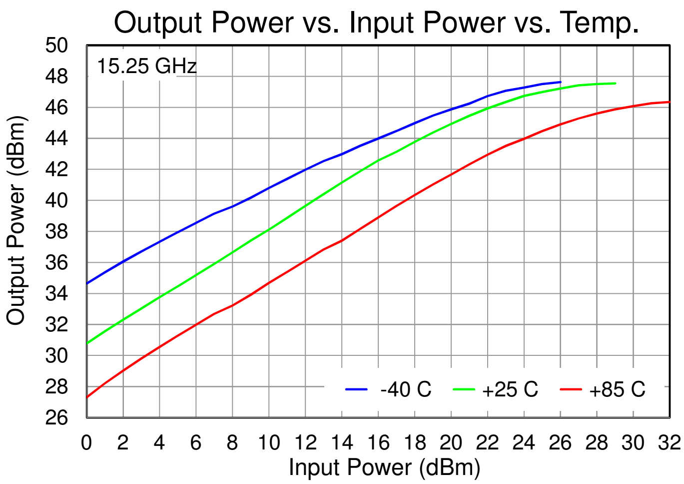

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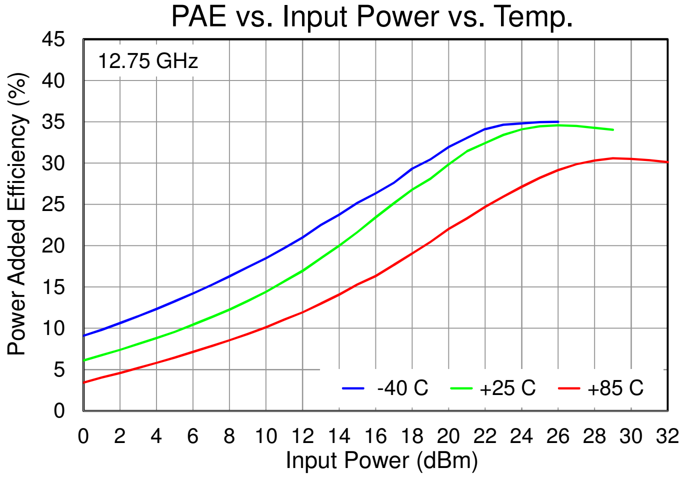

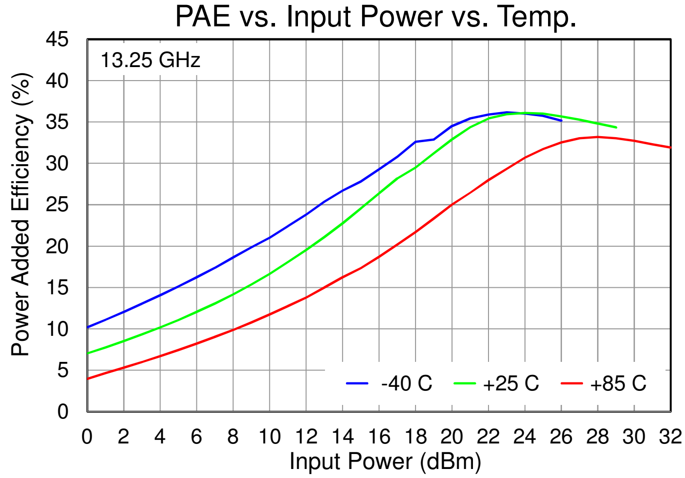

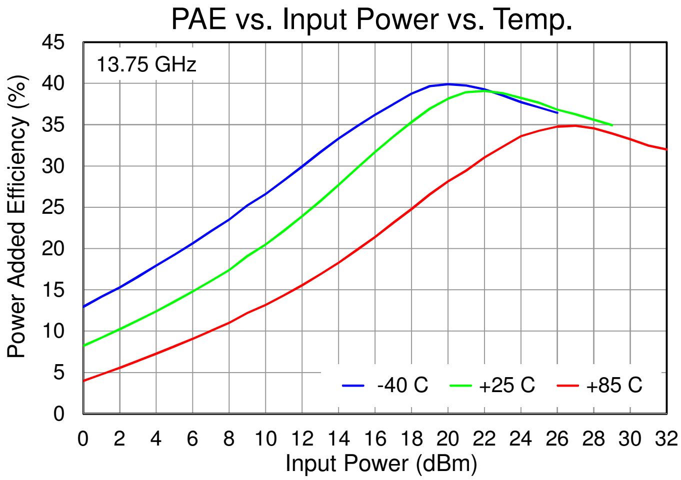

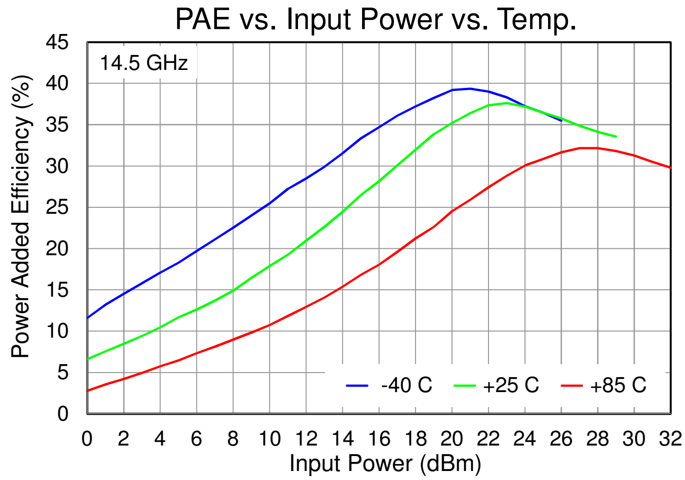

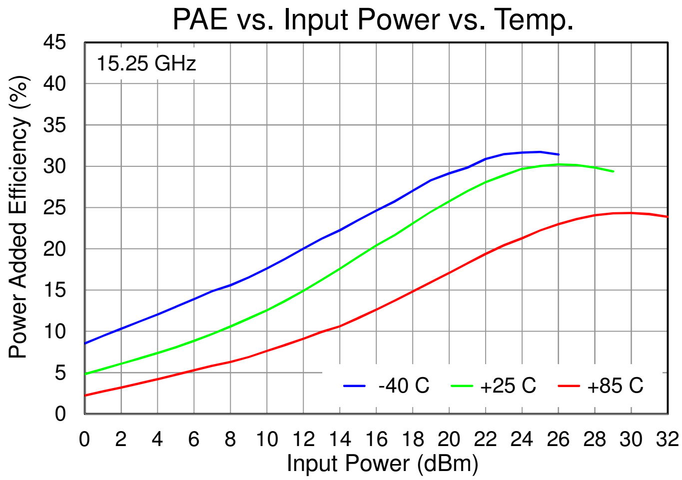

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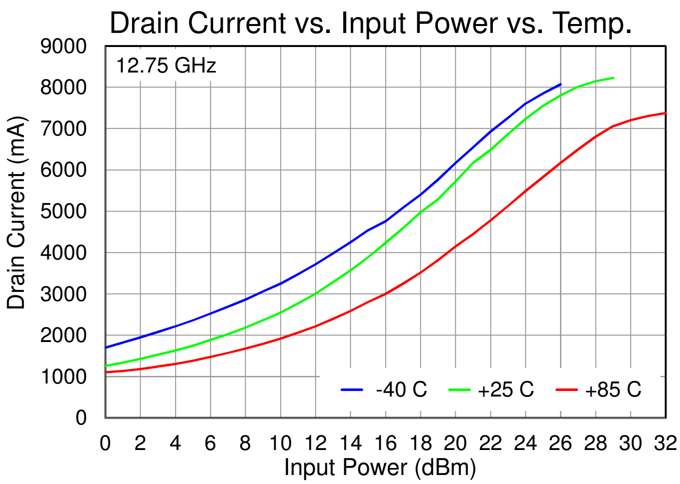

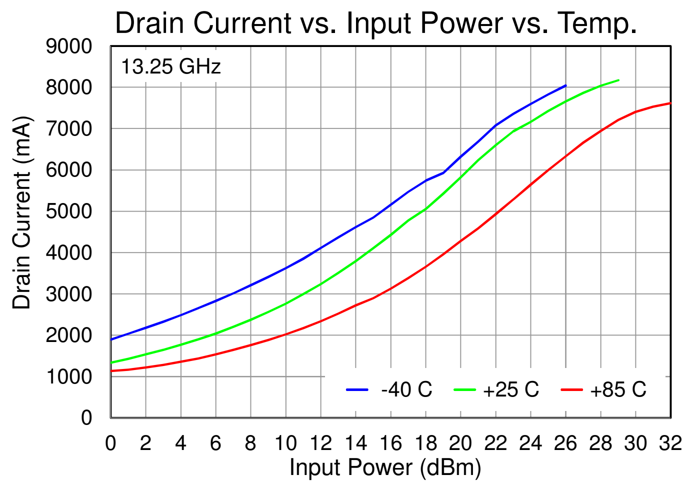

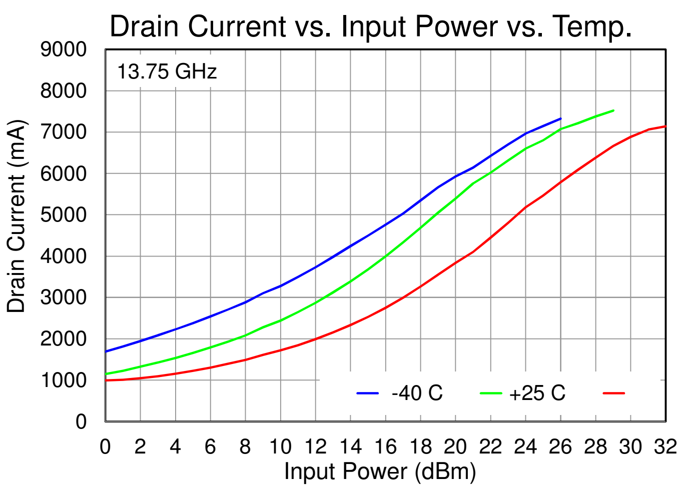

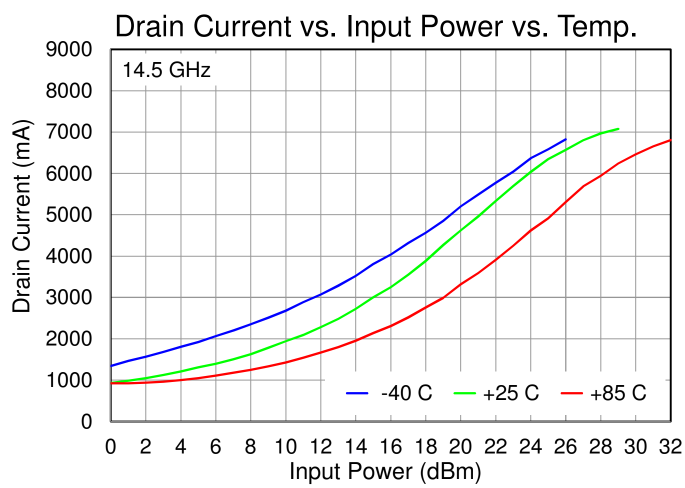

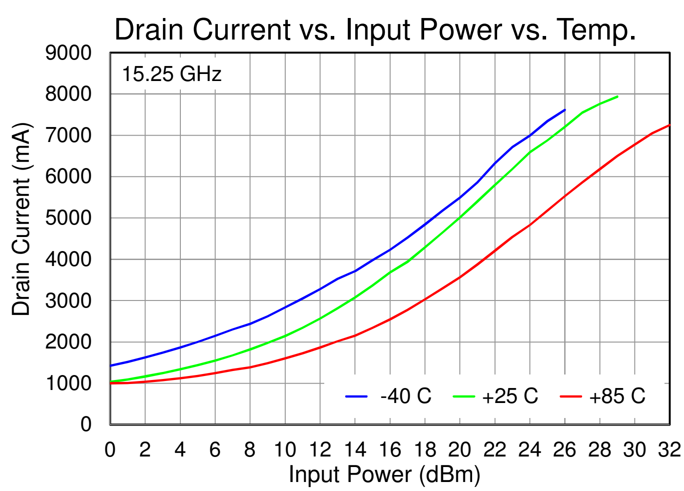

Performance Plots – Large Signal

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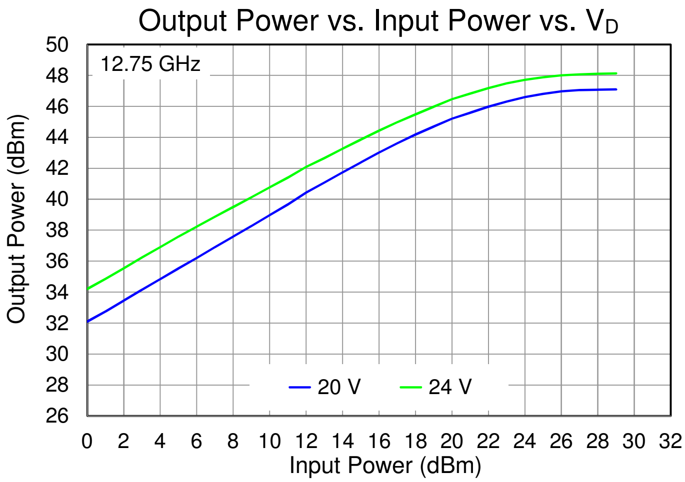

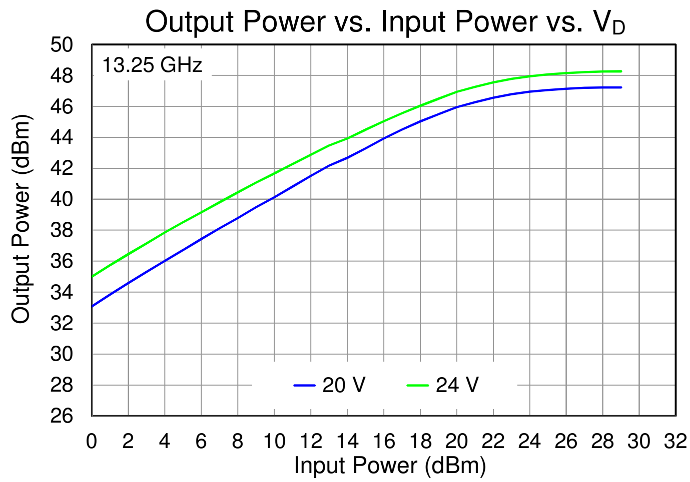

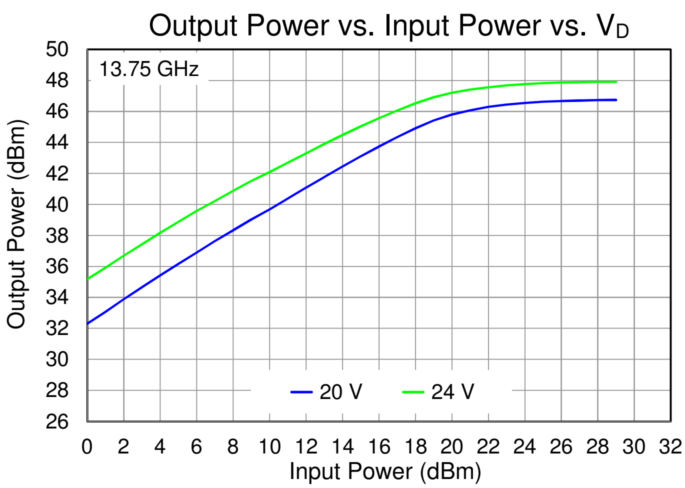

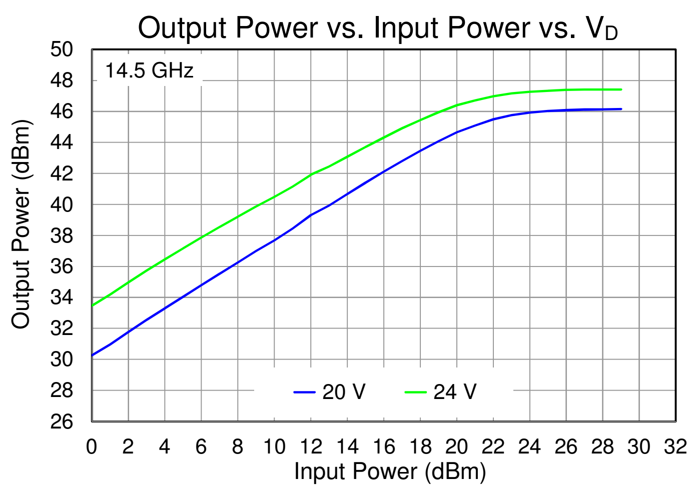

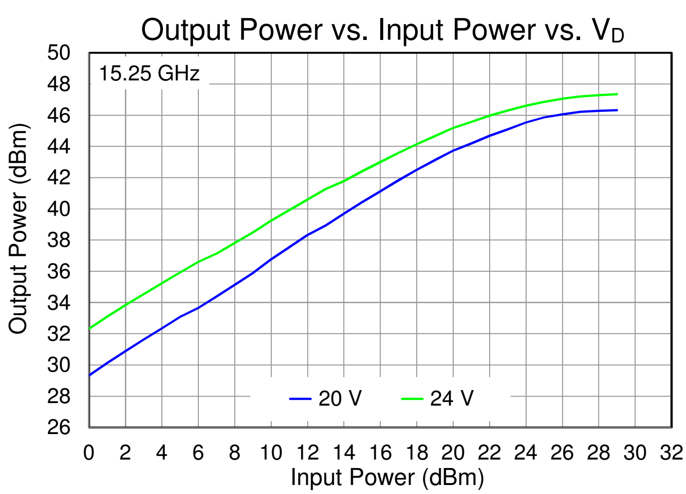

Performance Plots – Large Signal

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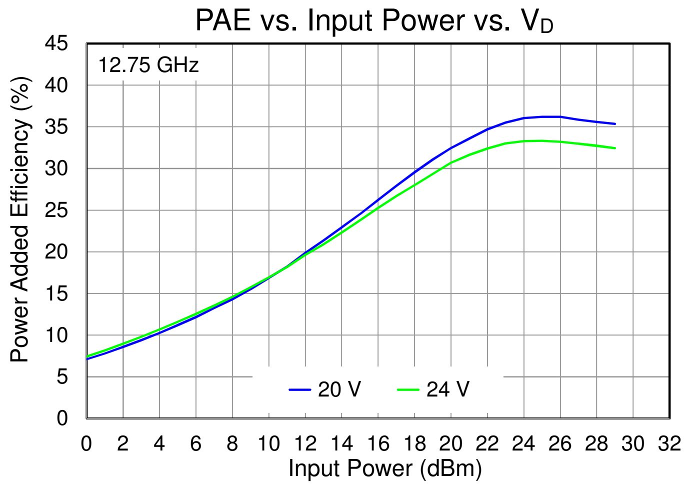

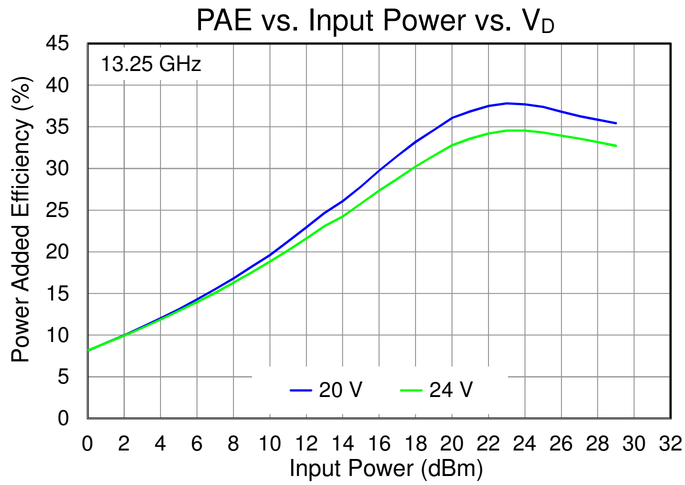

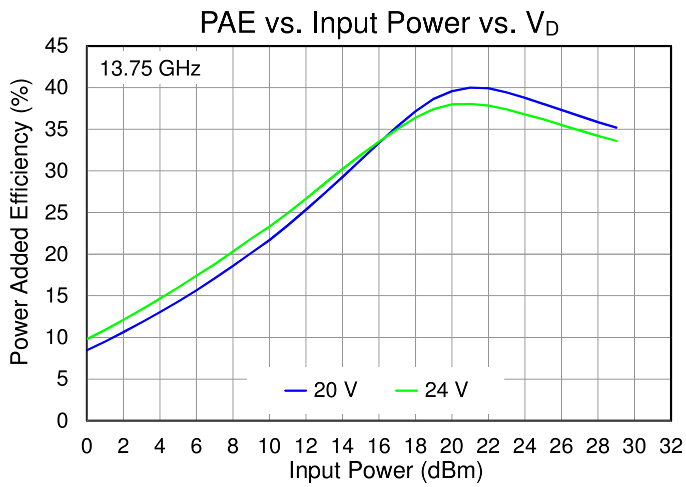

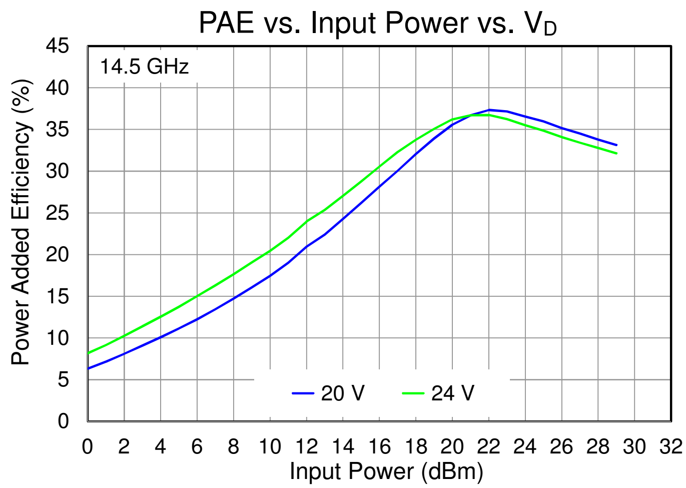

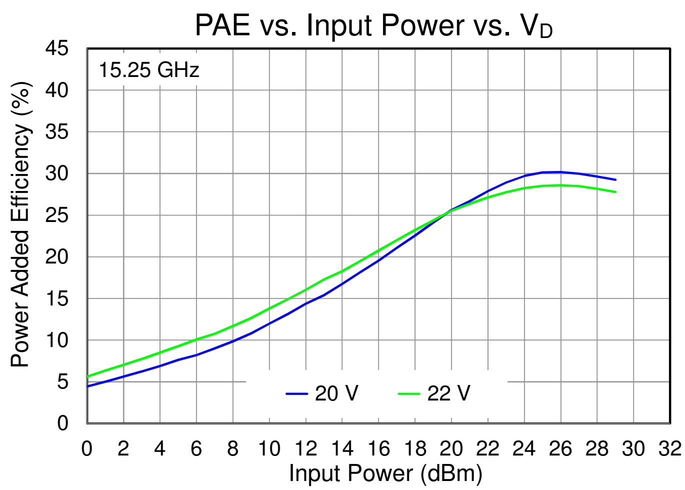

Performance Plots – Large Signal

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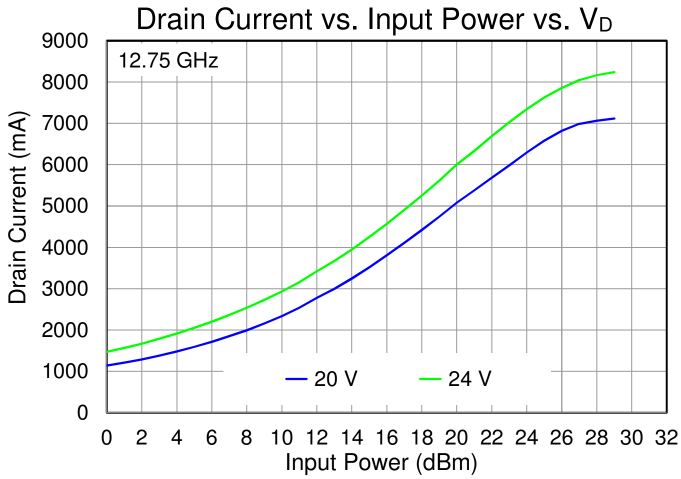

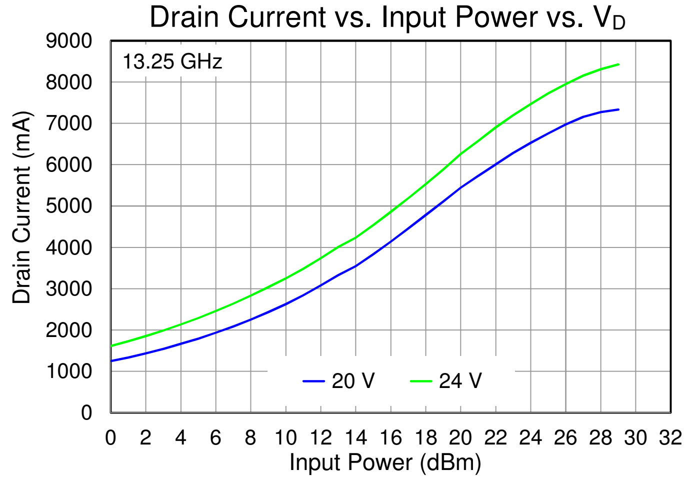

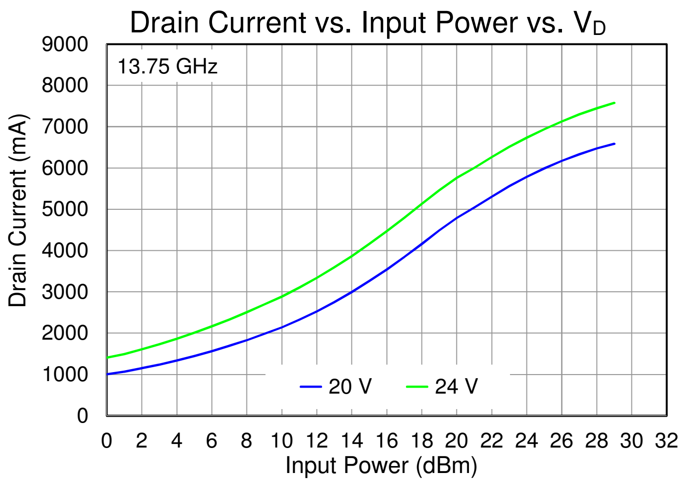

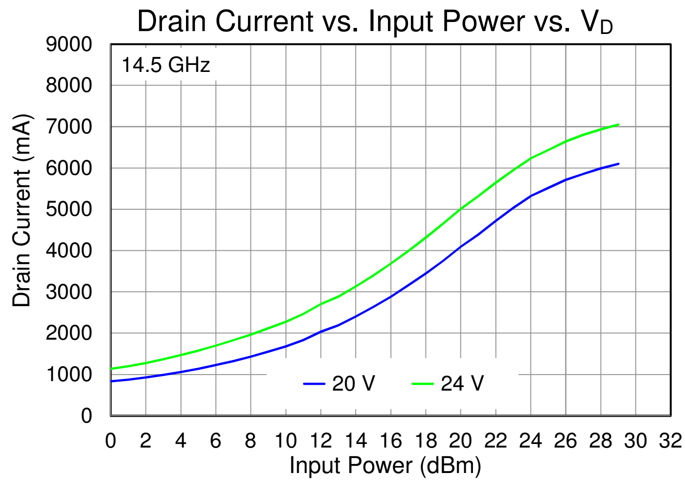

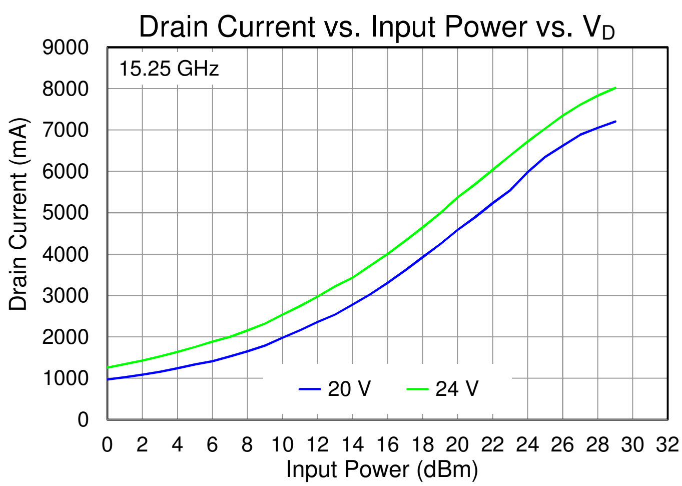

Performance Plots – Large Signal

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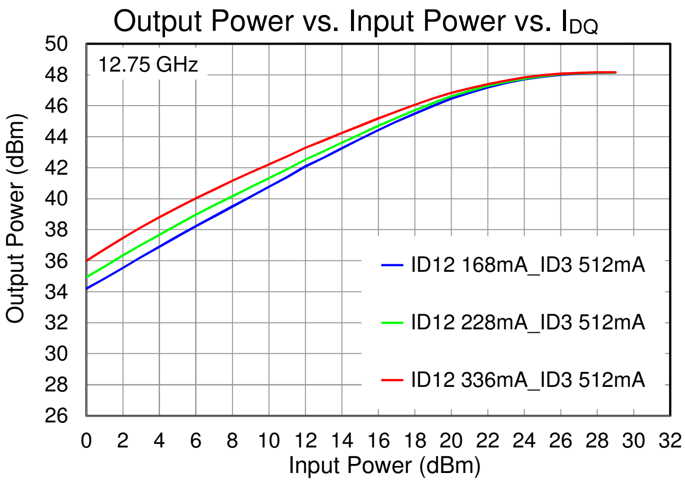
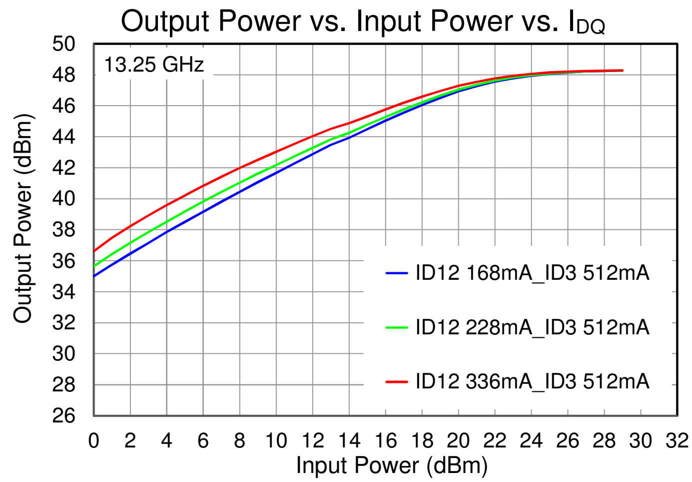
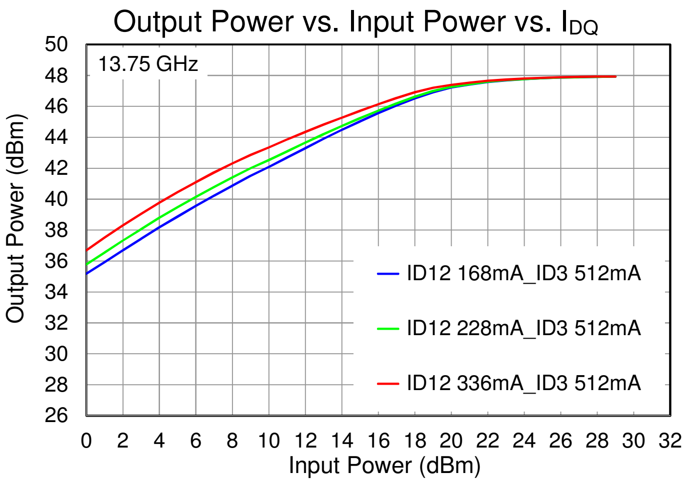
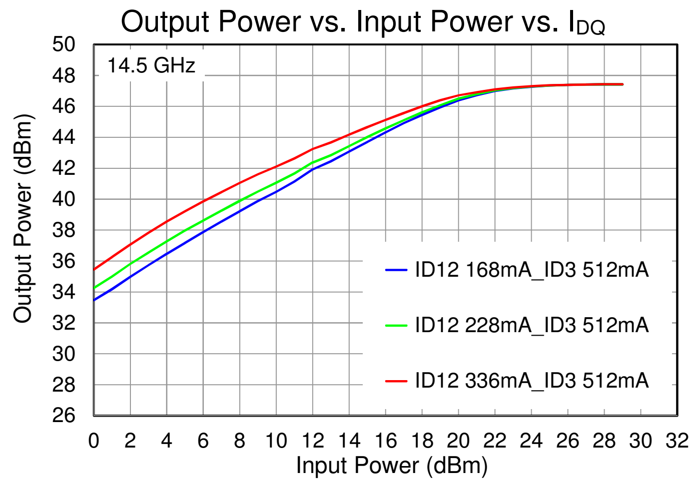
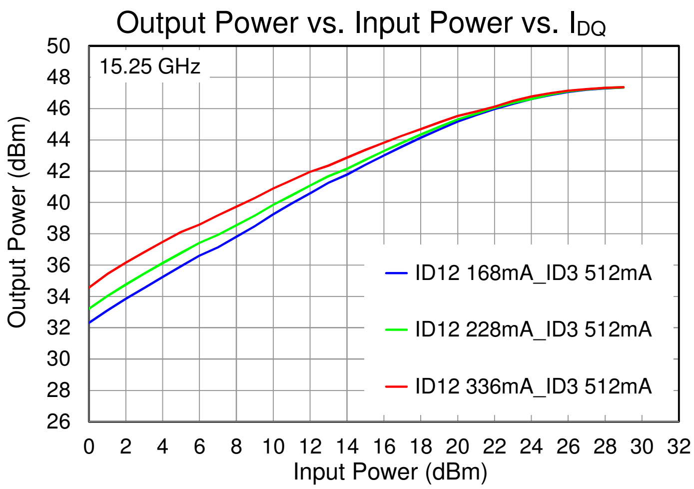




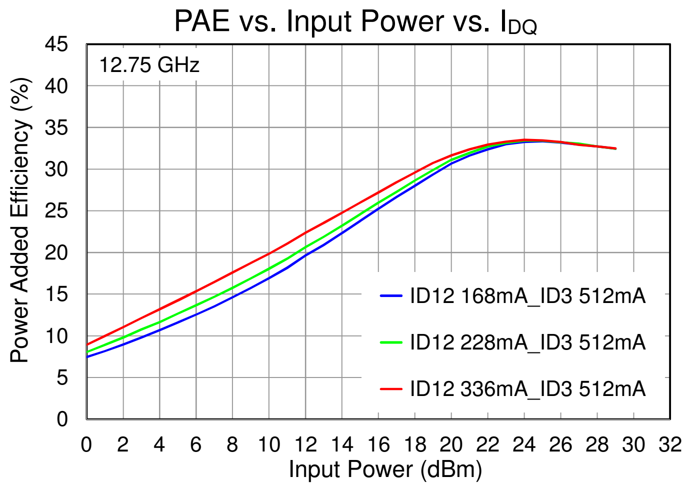


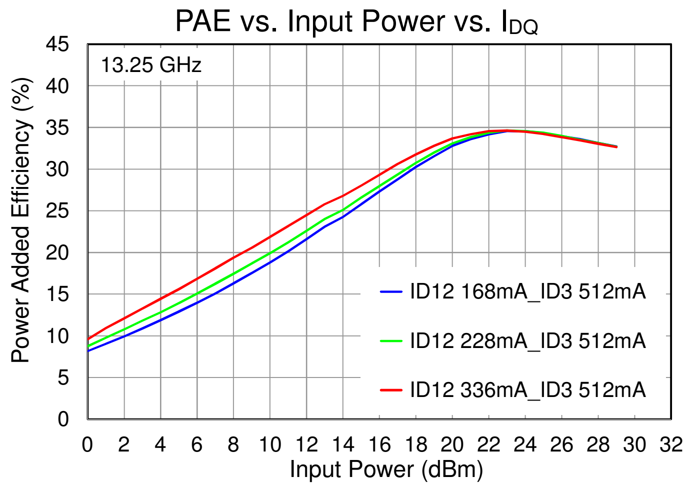


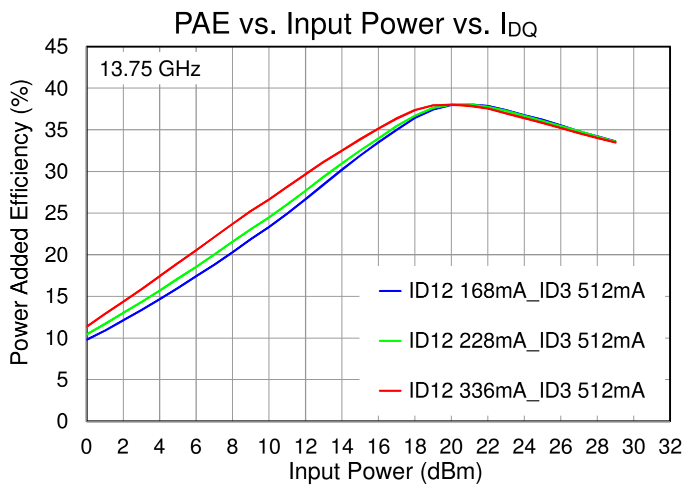


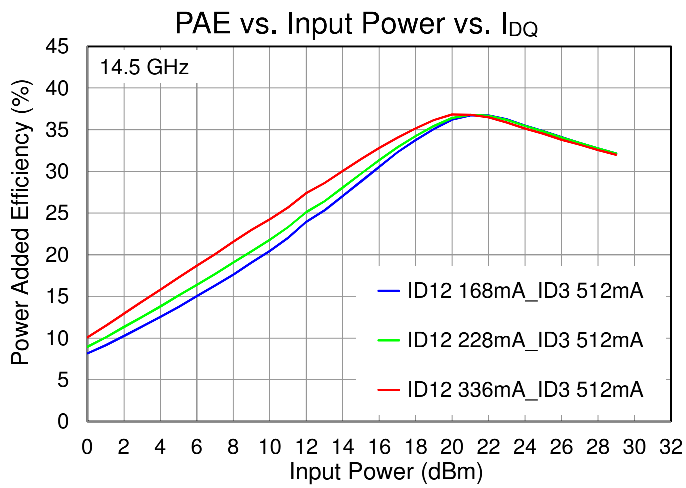
Performance Plots – Large Signal

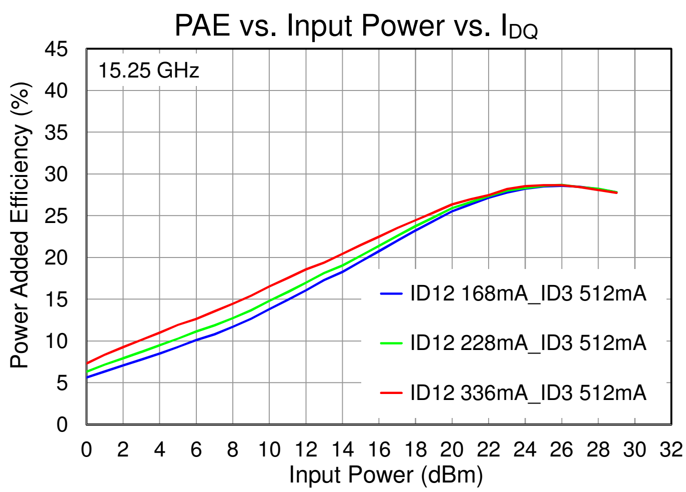
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA, P_{IN} = 25 dBm, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)





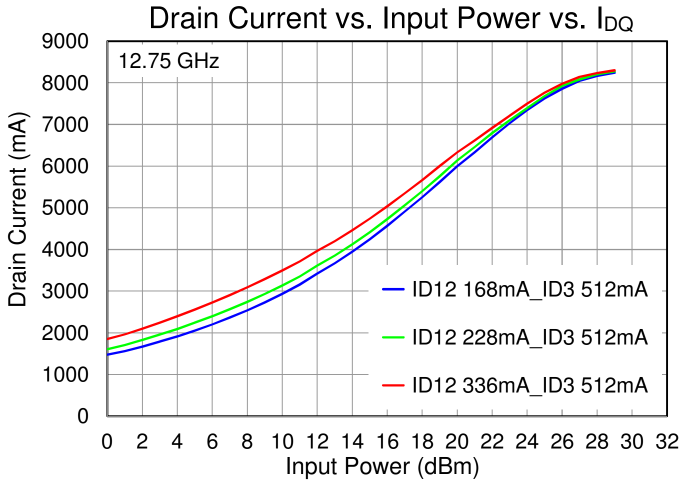


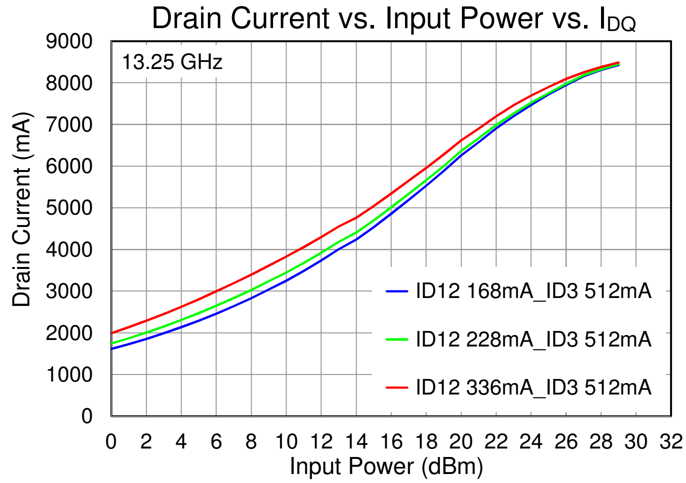


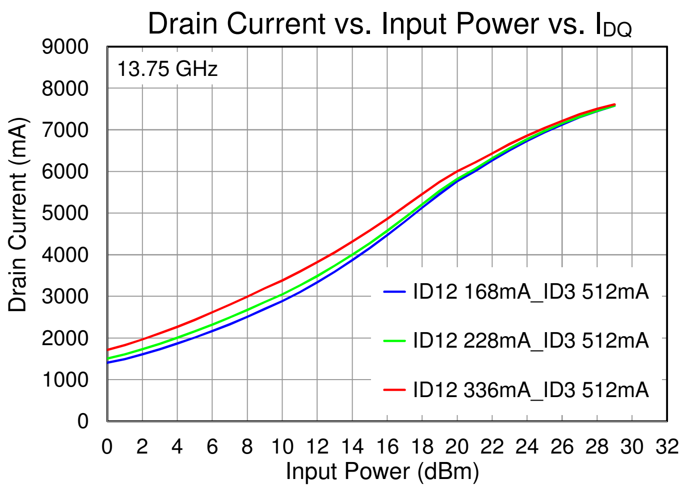


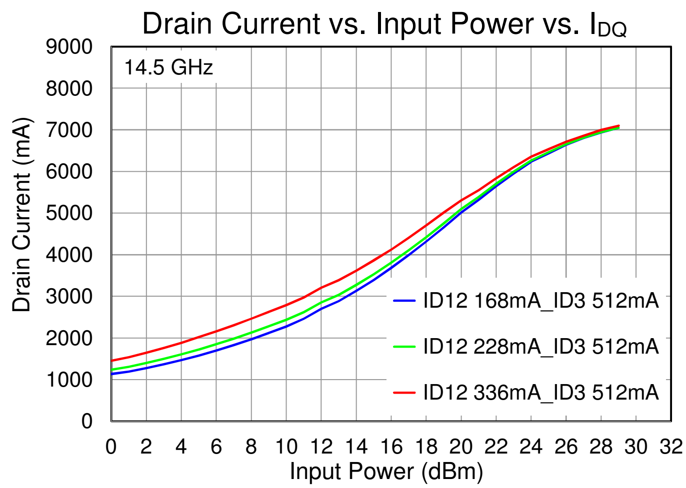
Performance Plots – Large Signal

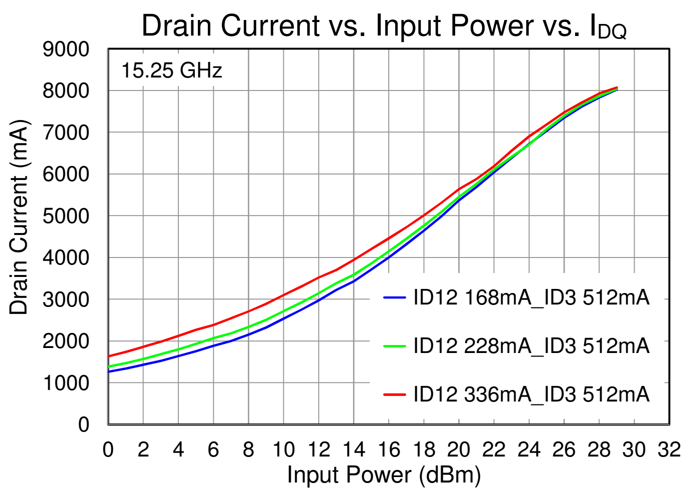
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA, P_{IN} = 25 dBm, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)







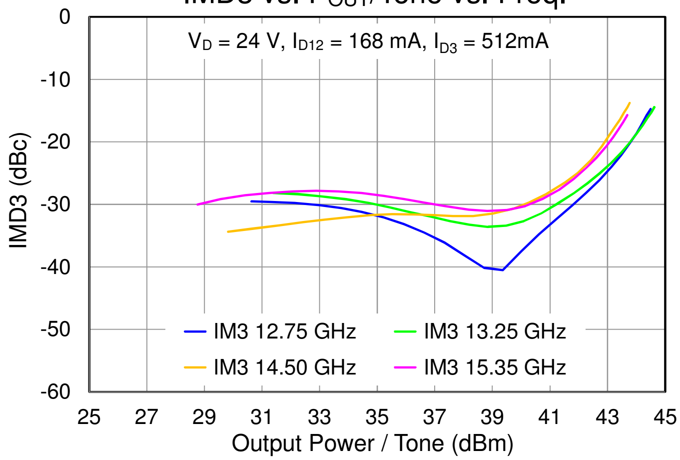




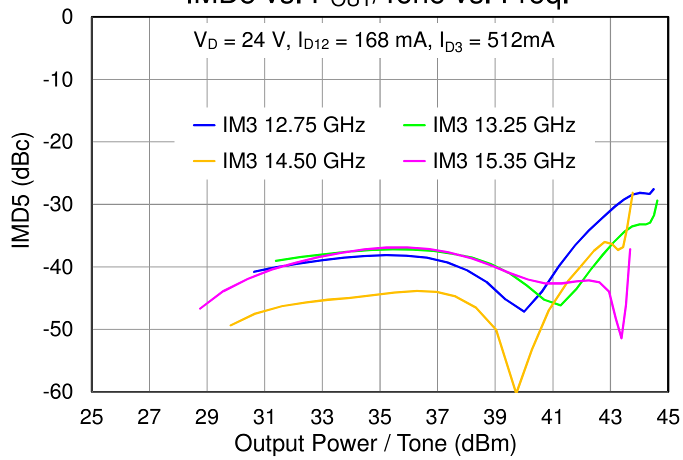
Performance Plots – Linearity

Test conditions, unless otherwise noted: **CW,** V_D = 24 V, Δf = 10 MHz, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)

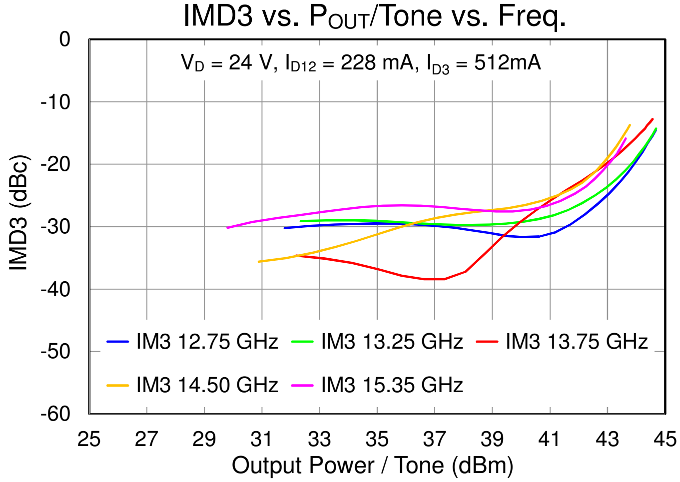
IMD3 vs. P_{OUT}/Tone vs. Freq.



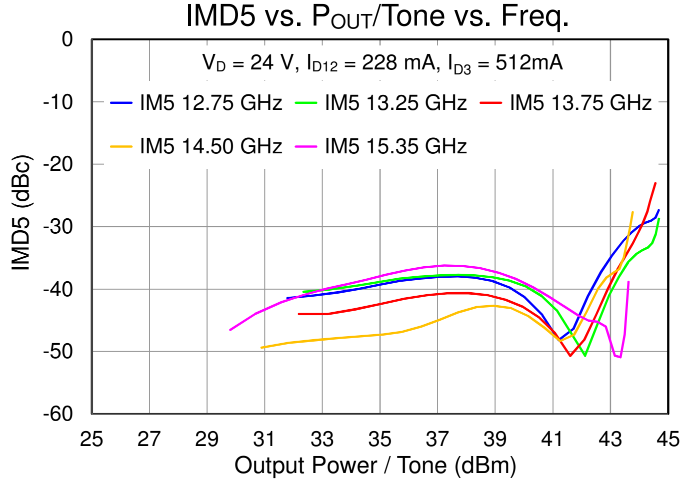
IMD5 vs. P_{OUT}/Tone vs. Freq.



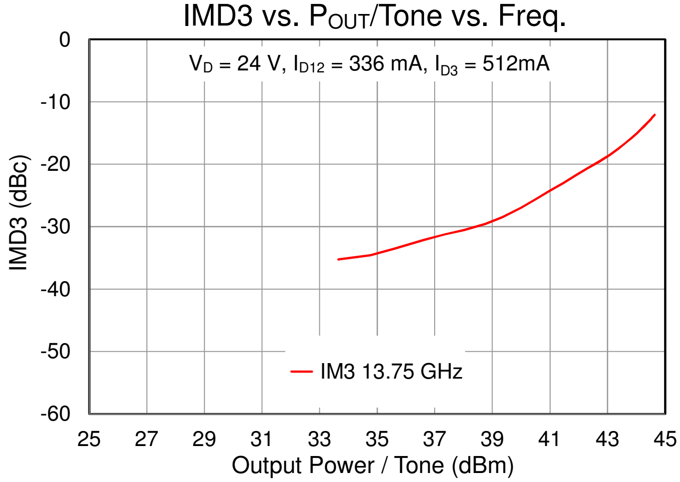
IMD3 vs. P_{OUT}/Tone vs. Freq.



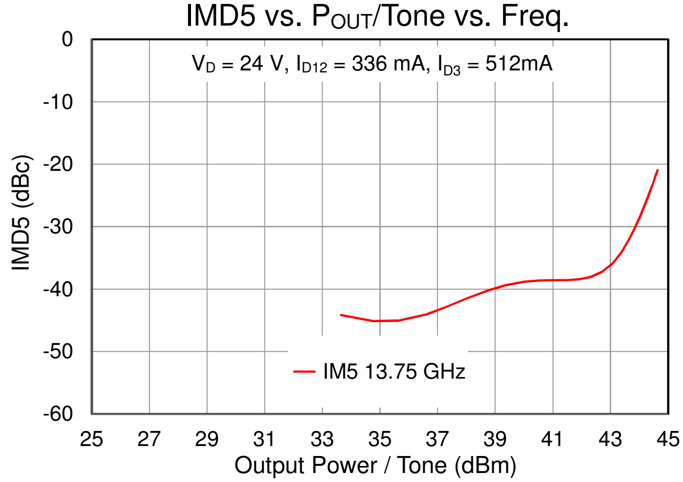
IMD5 vs. P_{OUT}/Tone vs. Freq.



IMD3 vs. P_{OUT}/Tone vs. Freq.

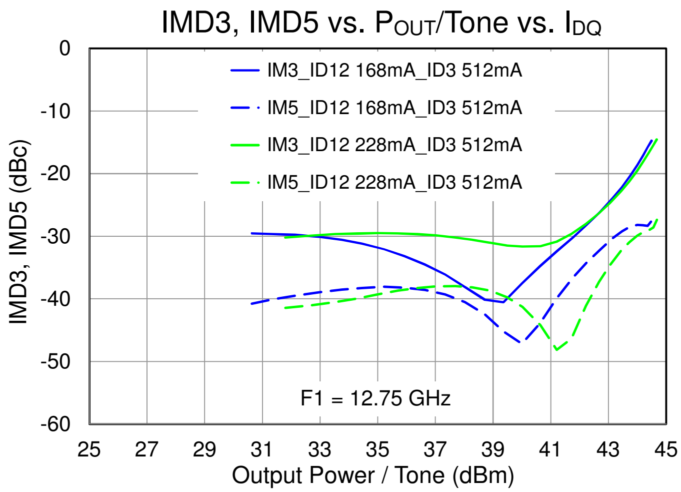


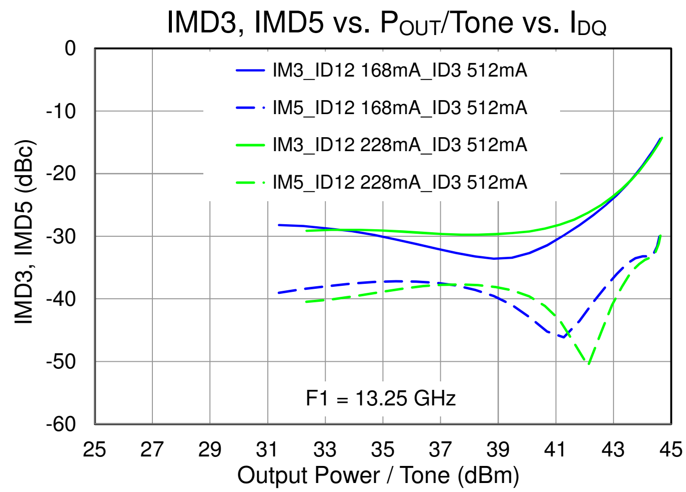
IMD5 vs. P_{OUT}/Tone vs. Freq.

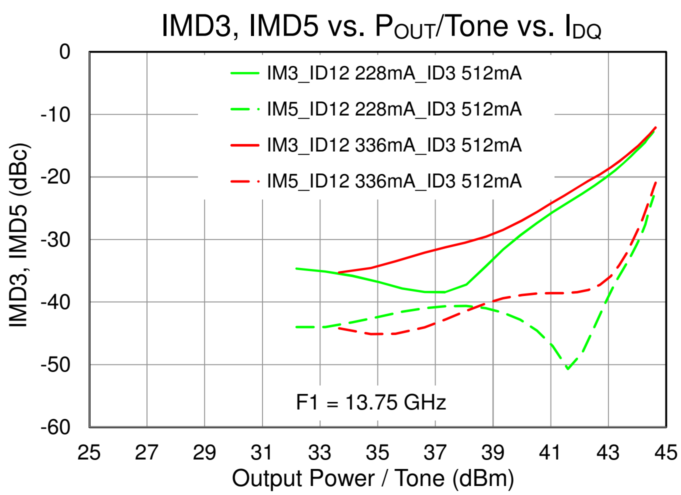


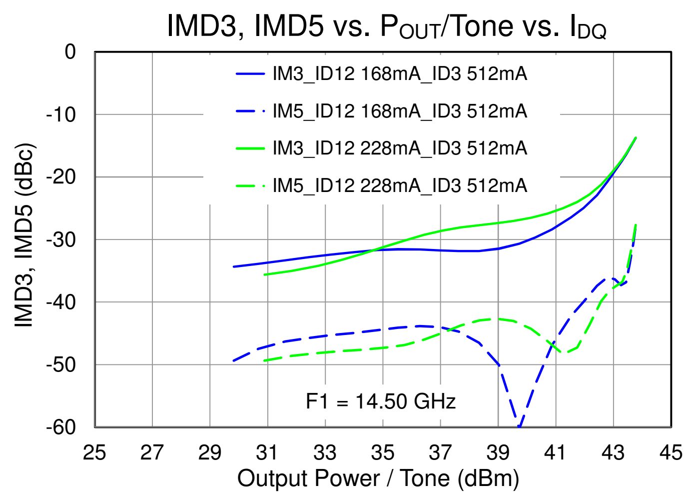
Performance Plots – Linearity

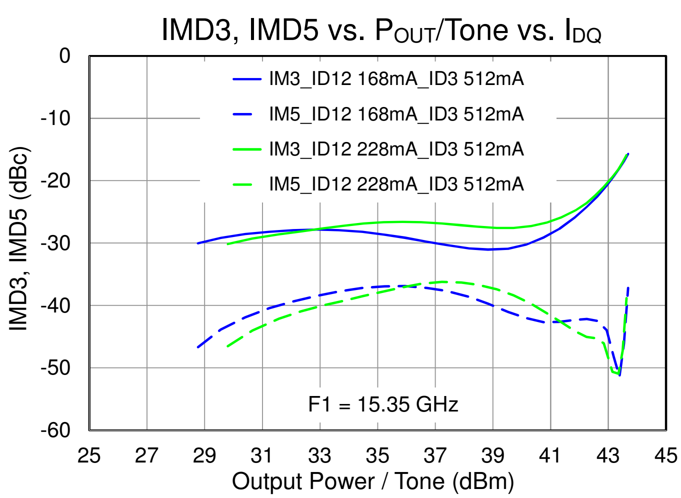
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, Δf = 10 MHz, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)





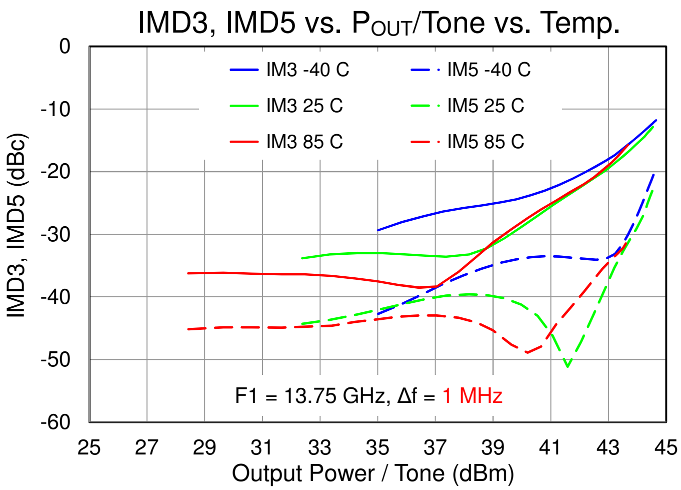


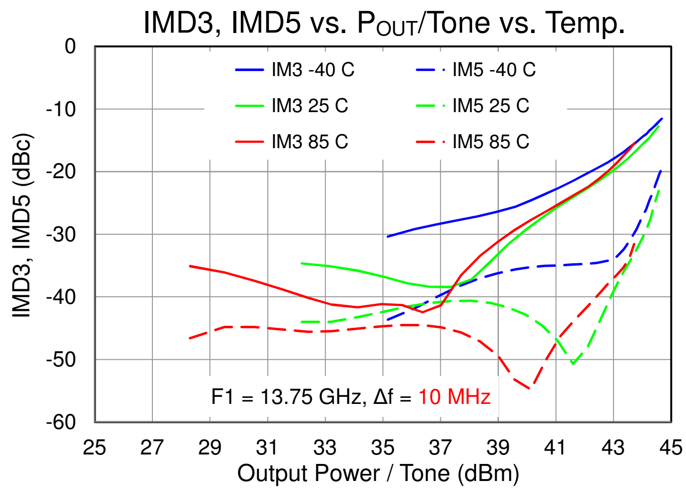


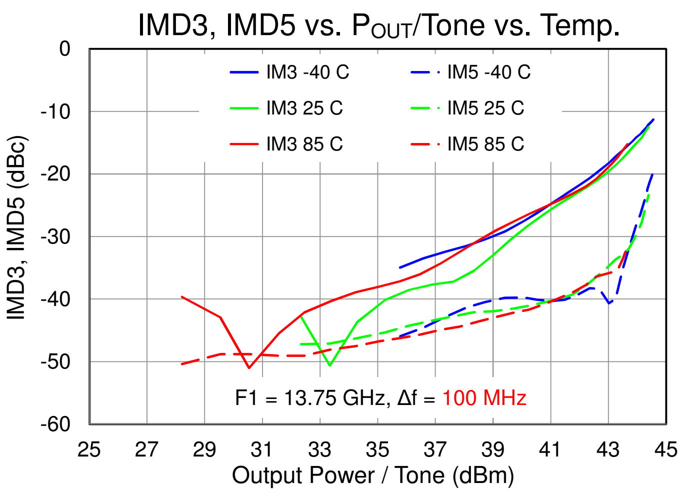


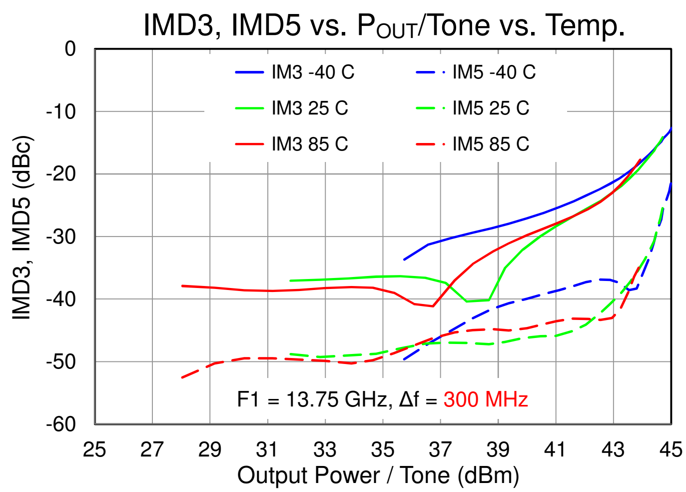
Performance Plots – Linearity

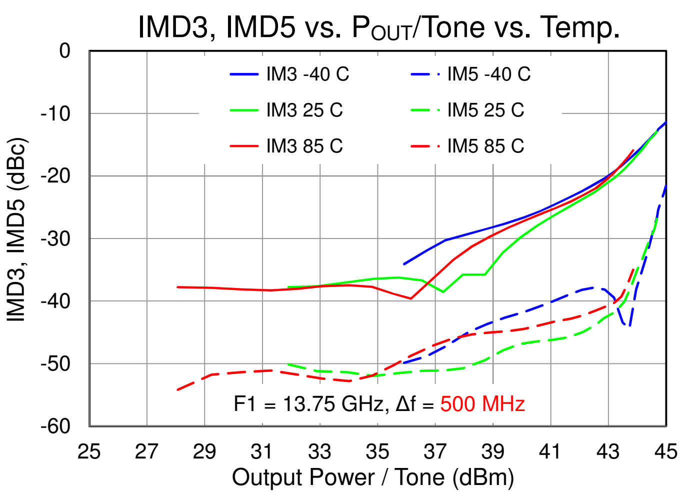
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, I_{D12} = 238 mA, I_{D3} = 512 mA, T_{BASE} is backside of 20 mil CuMo carrier plate

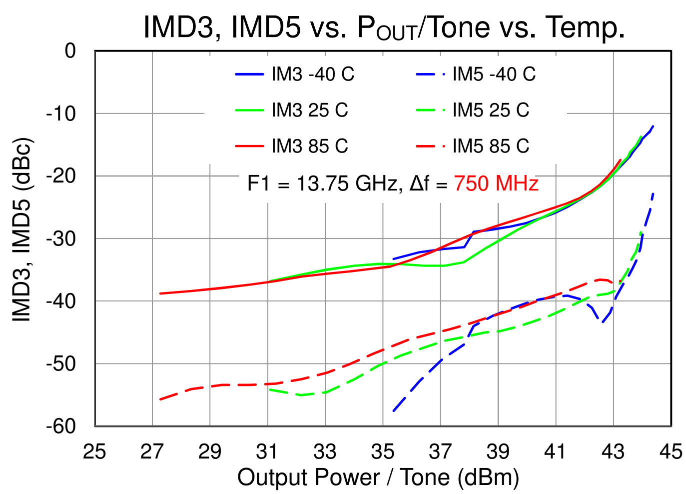






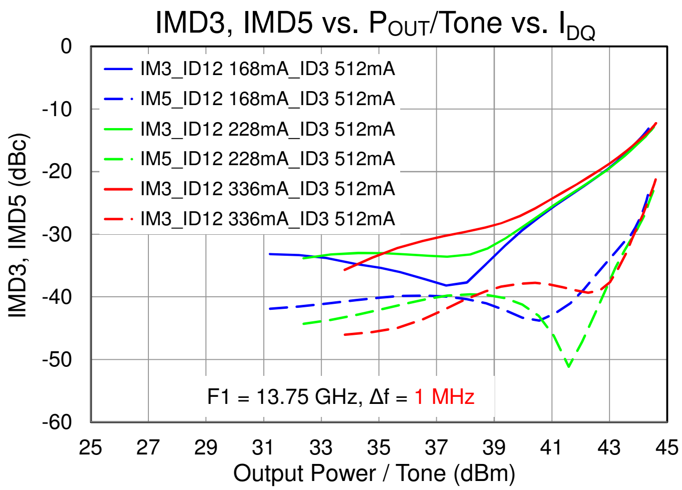


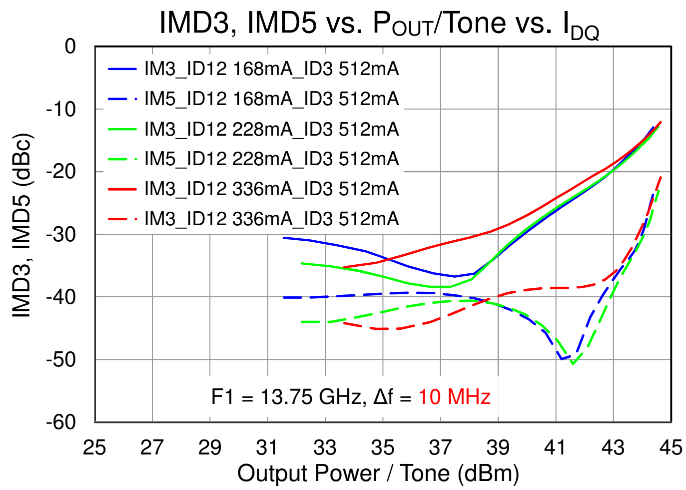


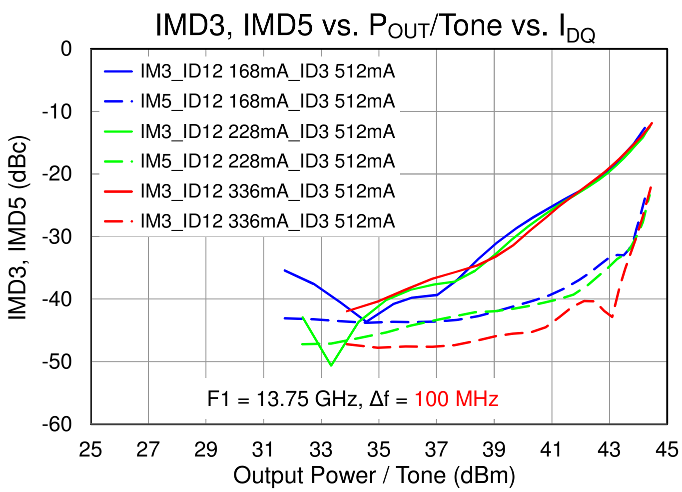


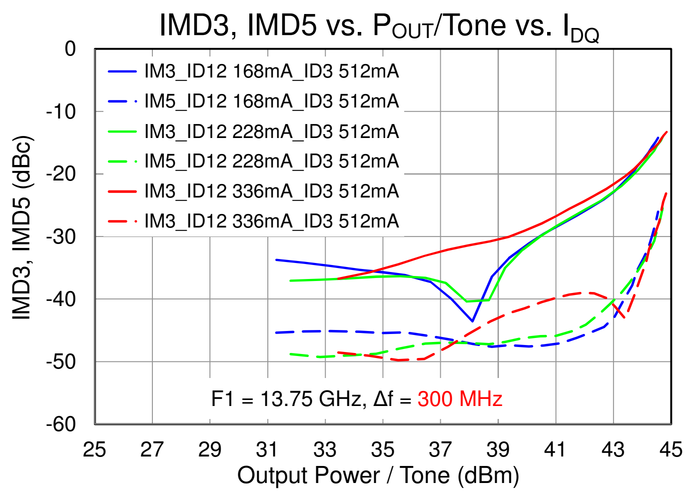
Performance Plots – Linearity

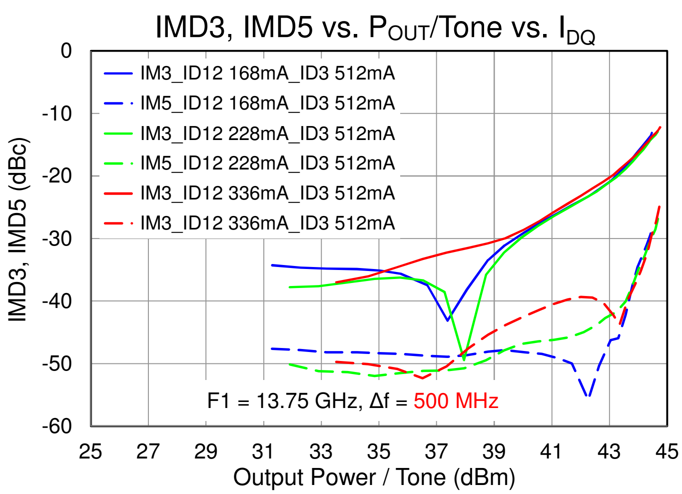
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)

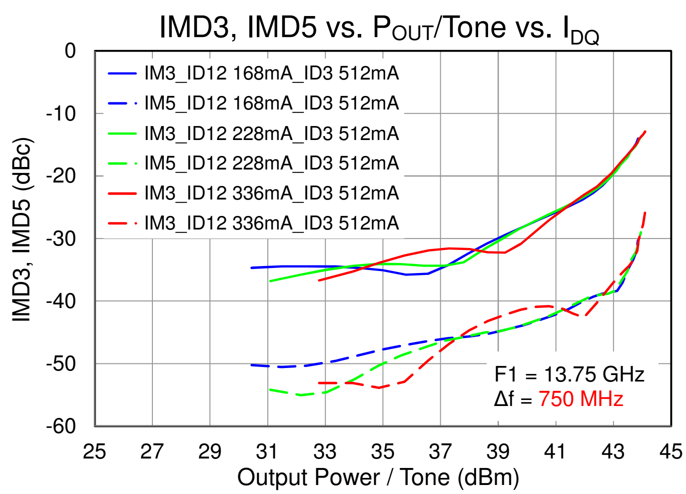






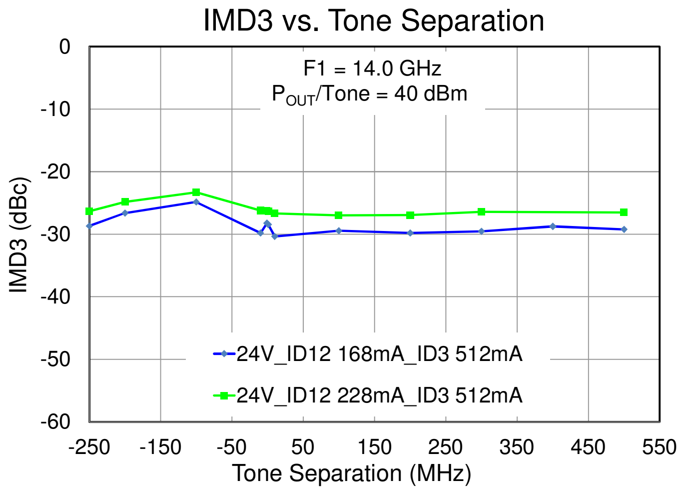


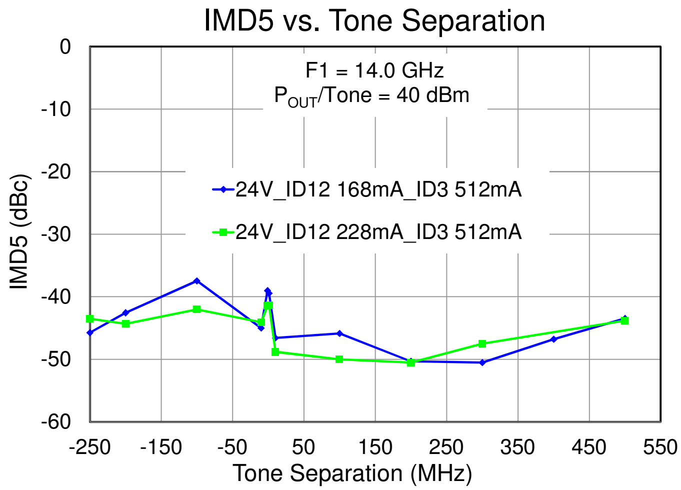


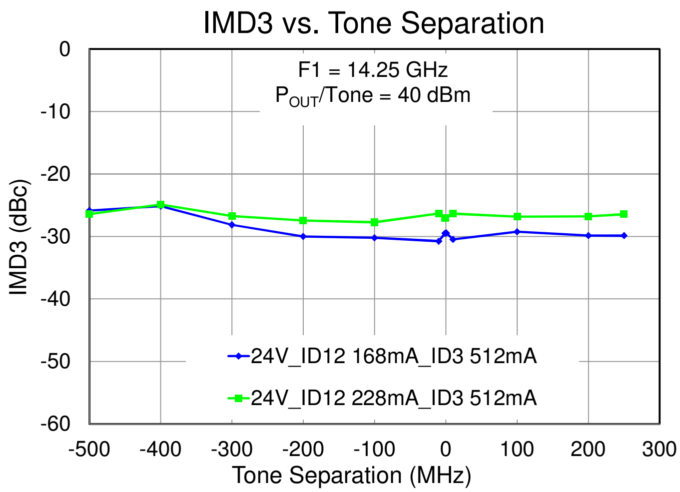


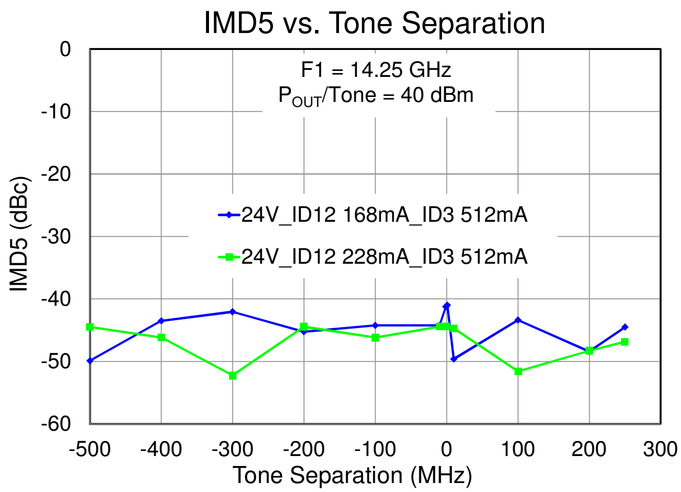
Performance Plots – Large Signal

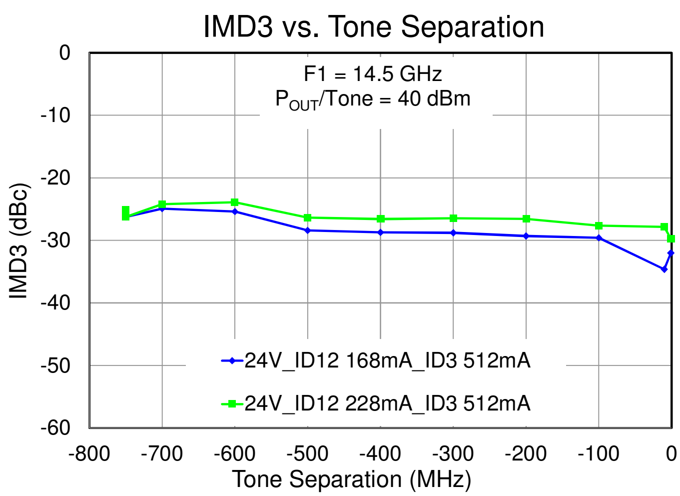
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)

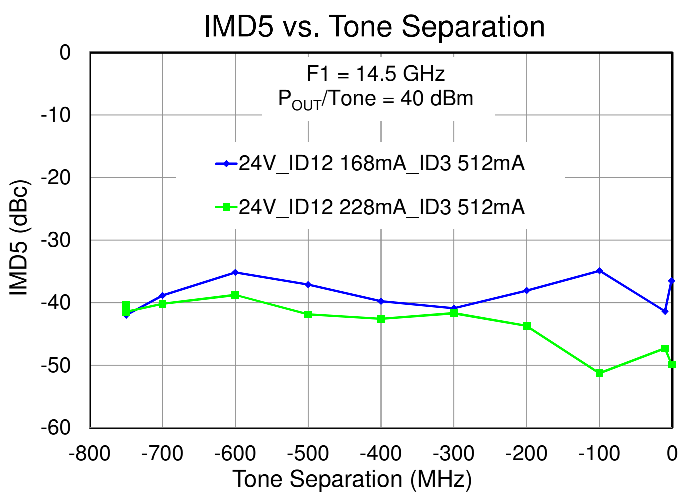






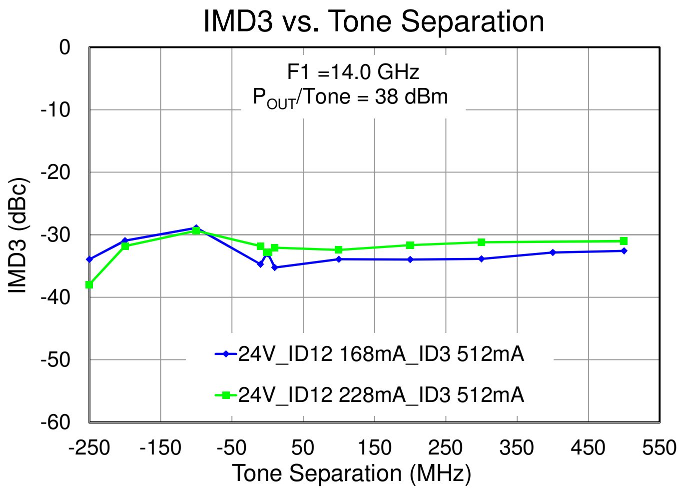


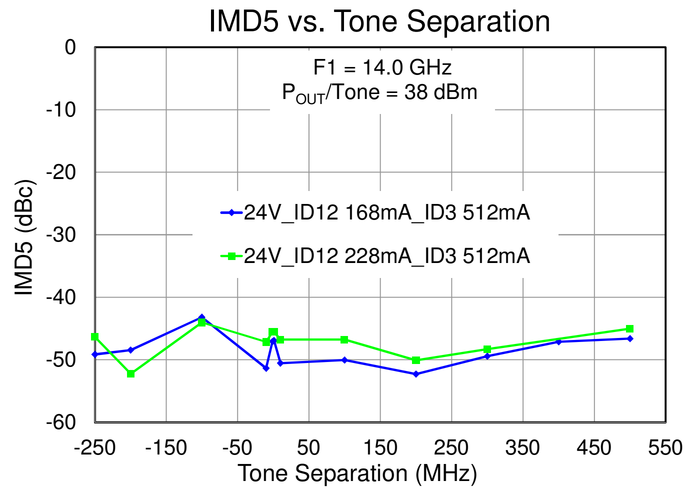


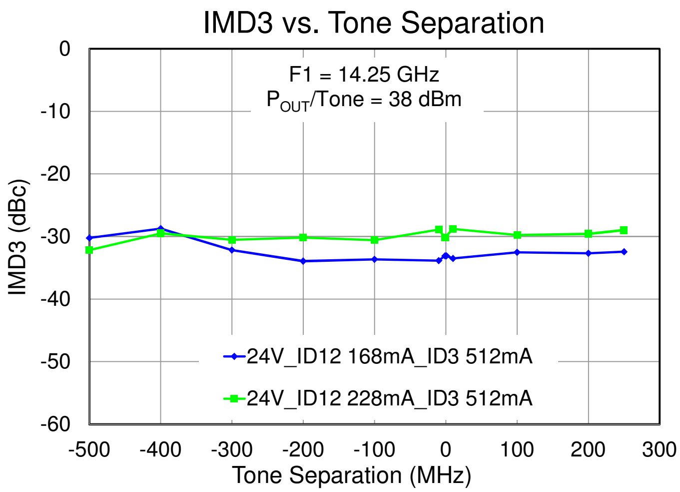


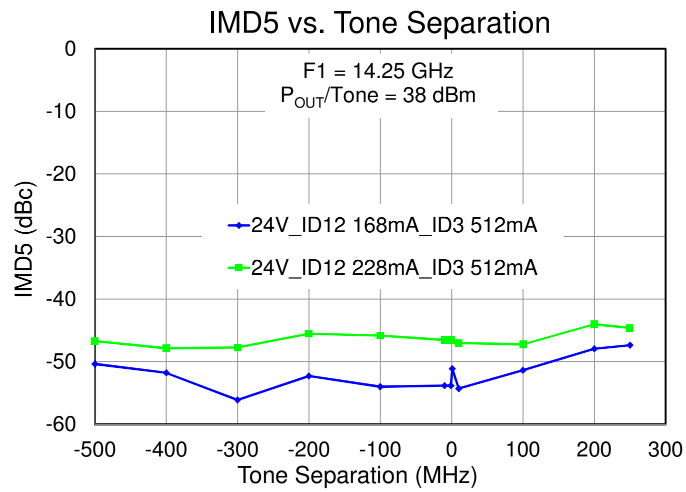
Performance Plots – Linearity

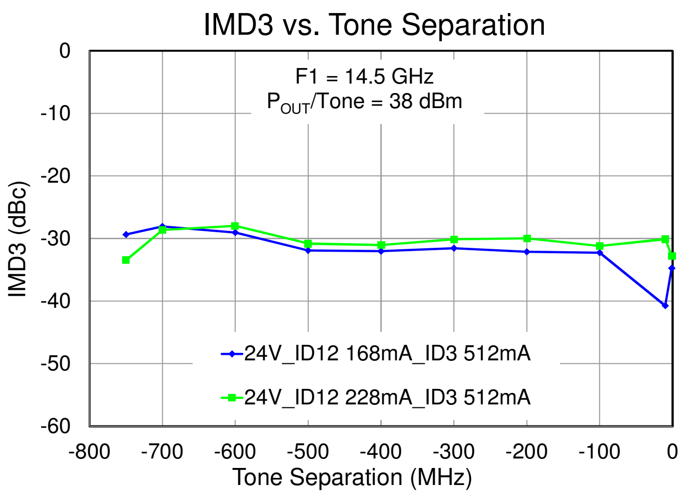
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)

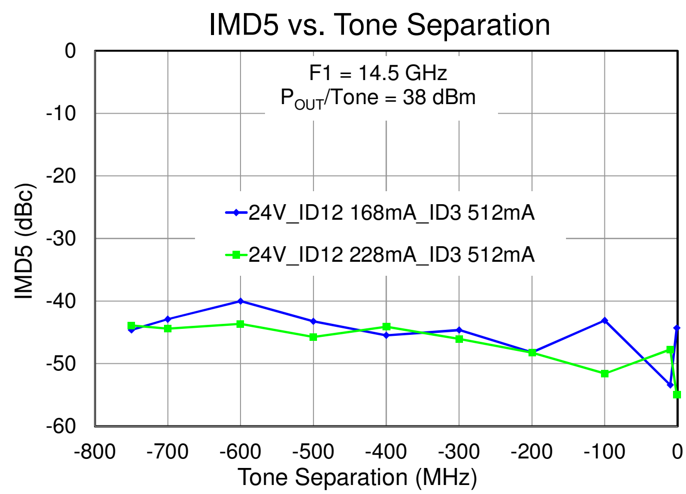






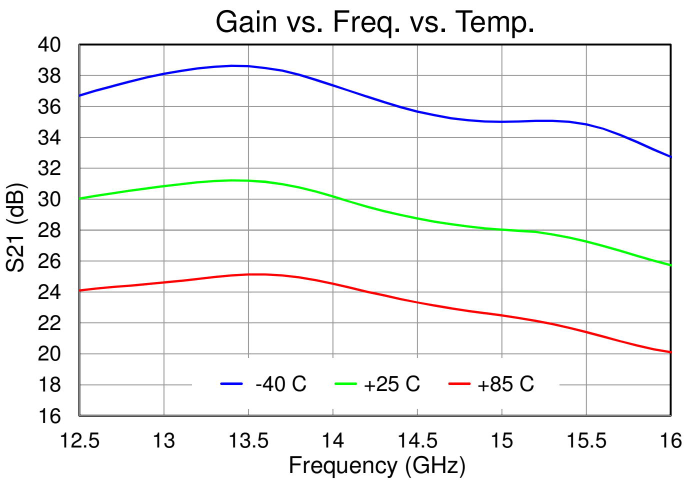


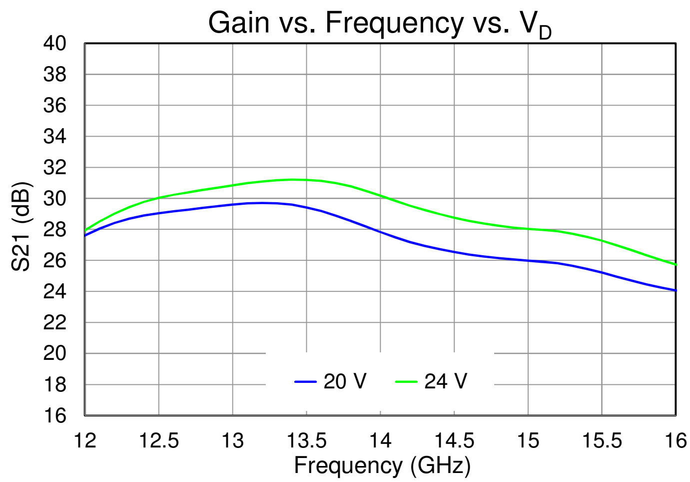


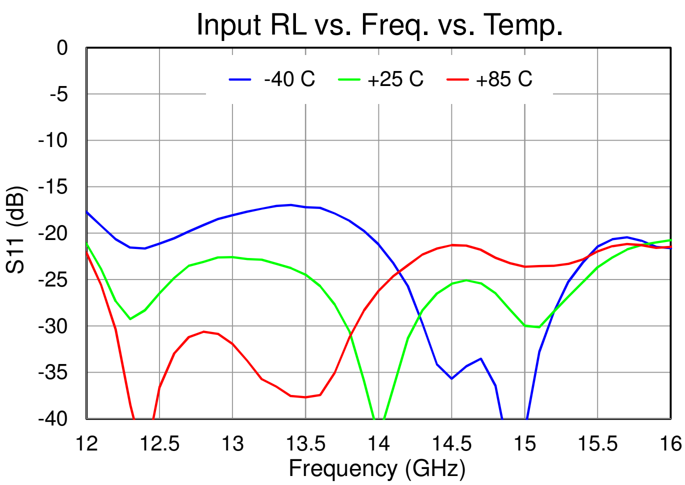


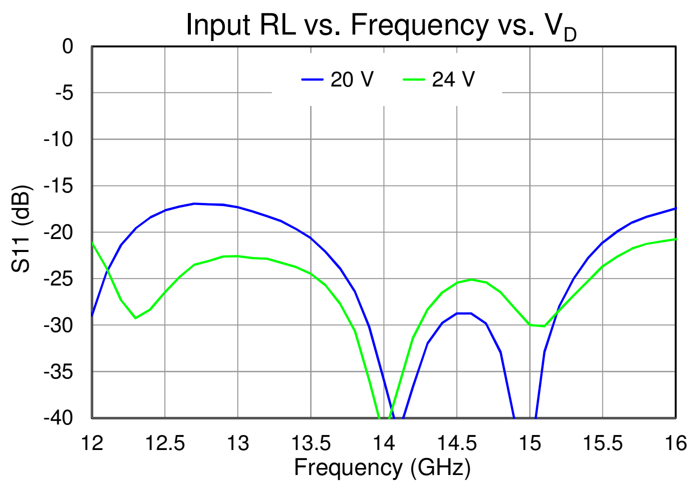
Performance Plots – Small Signal

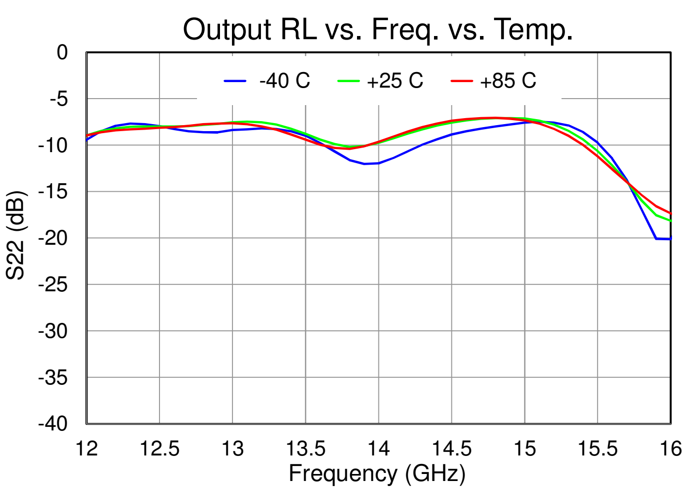
Test conditions, unless otherwise noted: **CW,** V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)

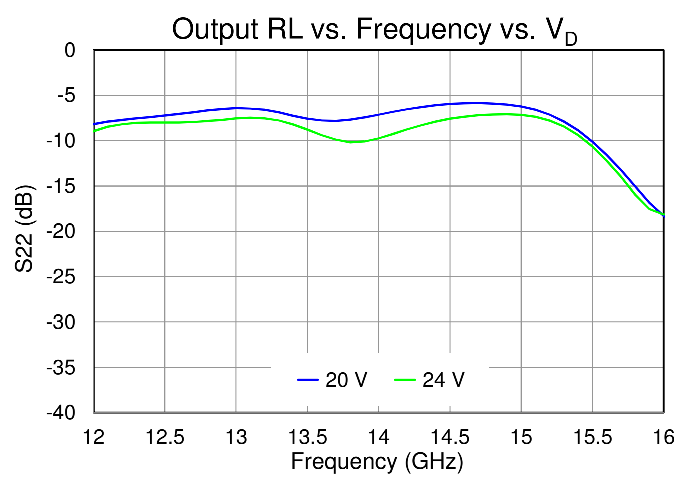






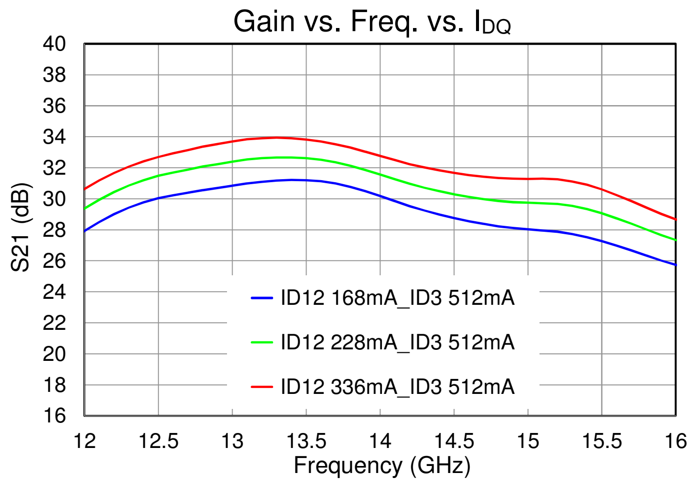


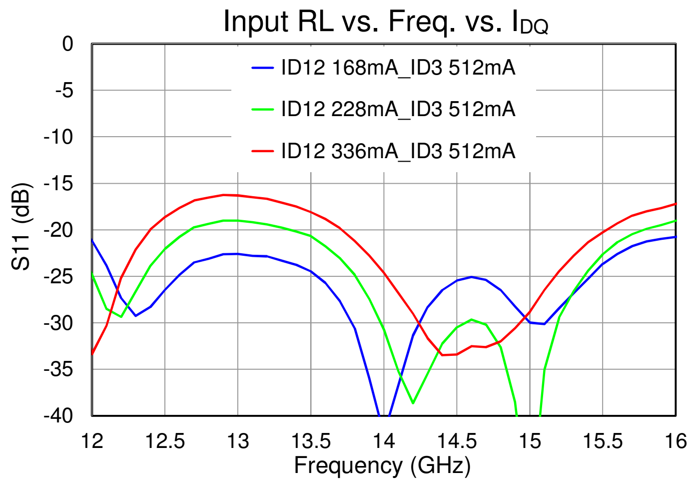


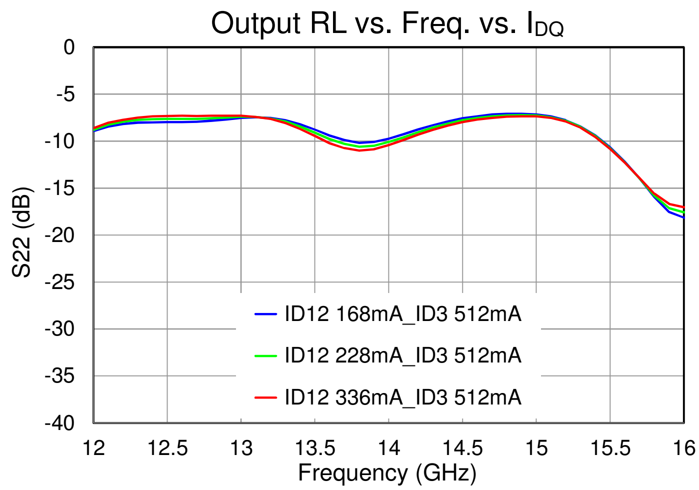


Performance Plots – Small Signal

Test conditions, unless otherwise noted: **CW,** V_D = 24 V, P_{IN} = -30 dBm, T_{BASE} = +25 ºC (backside of 20 mil CuMo carrier plate)







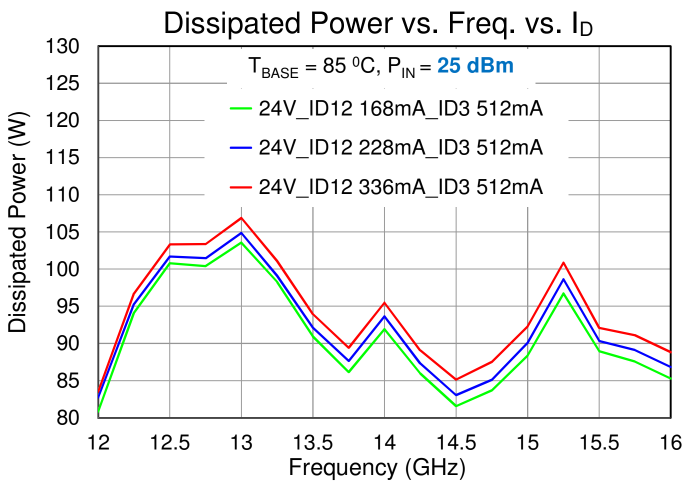
Thermal and Reliability Information

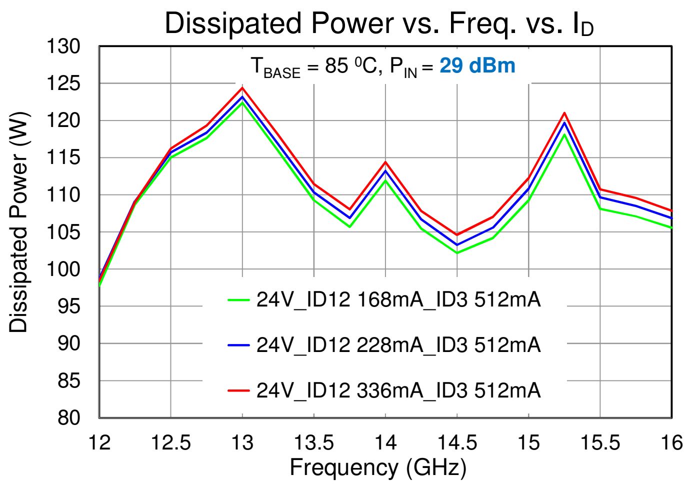
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent, no RF T_{BASE} = 85 °C, V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA P_{DISS} = 16.3 W	0.70	ºC/W
Channel Temperature, T_{CH} (2)		96	°C
Thermal Resistance, θ_{JC} (1)	For 13.75 – 14.5 GHz: P_{IN} = 25 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA , Freq = 14 GHz, I_{D_DRIVE} Total = 5560 mA, P_{OUT} = 46.2 dBm P_{DISS} = 91.9 W	0.73	ºC/W
Channel Temperature, T_{CH} (2)		152	°C
Thermal Resistance, θ_{JC} (1)	For 13.75 – 14.5 GHz P_{IN} = 25 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{D12} = 228 mA, I_{D3} = 512 mA , Freq = 14 GHz, I_{D_DRIVE} Total = 5680 mA, P_{OUT} = 46.3 dBm P_{DISS} = 93.7 W	0.73	ºC/W
Channel Temperature, T_{CH} (2)		153	°C
Thermal Resistance, θ_{JC} (1)	For extended 12.75 – 15.35 GHz: P_{IN} = 25 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA , Freq = 13 GHz, I_{D_DRIVE} Total = 5960 mA, P_{OUT} = 46 dBm P_{DISS} = 104 W	0.74	ºC/W
Channel Temperature, T_{CH} (2)		162	°C
Thermal Resistance, θ_{JC} (1)	For extended 12.75 – 15.35 GHz: P_{IN} = 25 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{D12} = 228 mA, I_{D3} = 512 mA , Freq = 13 GHz, I_{D_DRIVE} Total = 6028 mA, P_{OUT} = 46.dBm P_{DISS} = 105 W	0.74	ºC/W
Channel Temperature, T_{CH} (2)		163	°C
Thermal Resistance, θ_{JC} (1)	For 13.75 – 14.5 GHz: P_{IN} = 29 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA , Freq = 14 GHz, I_{D_DRIVE} Total = 6925 mA, P_{OUT} = 47.4 dBm P_{DISS} = 112 W	0.75	ºC/W
Channel Temperature, T_{CH} (2)		169	°C
Thermal Resistance, θ_{JC} (1)	For extended 12.75 – 15.35 GHz: P_{IN} = 29 dBm, T_{BASE} = 85 °C, CW, V_D = 24 V, I_{D12} = 168 mA, I_{D3} = 512 mA , Freq = 13 GHz, I_{D_DRIVE} Total = 7275 mA, P_{OUT} = 47.2 dBm P_{DISS} = 123 W	0.76	ºC/W
Channel Temperature, T_{CH} (2)		179	°C

Notes:

1. Thermal resistance determined to the back of 20 mil carrier plate CuMo with AuSn die attached
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note “GaN Device TCHMAX Theta-JC and Reliability Estimates,” located here https://www.qorvo.com/products/d/da006480

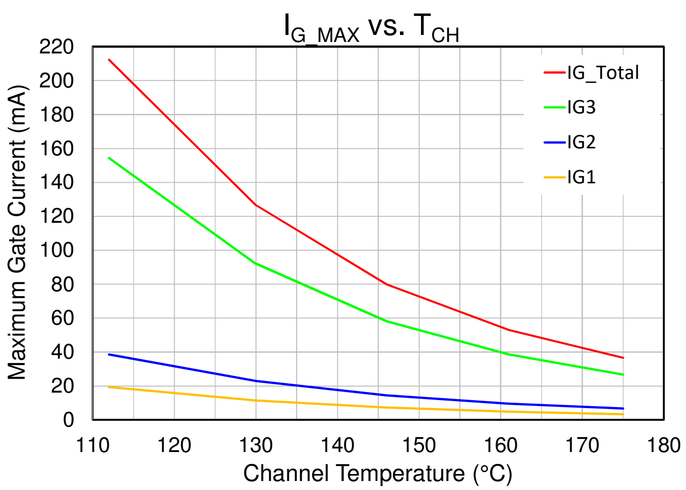
Dissipated Power and Maximum Gate Current





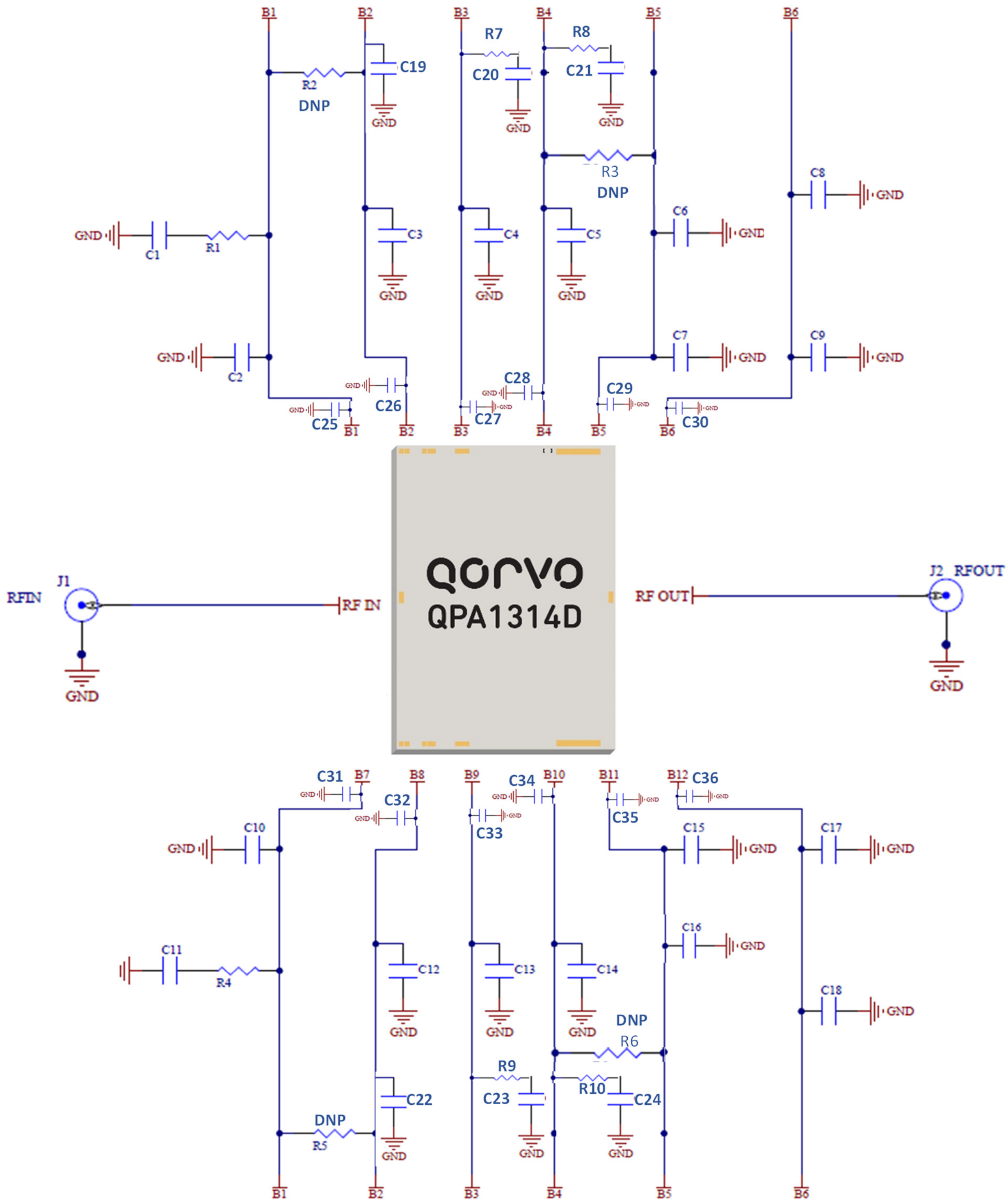
Test conditions, unless otherwise noted: CW, V_D = 24 V, I_{D12} = 168, 228 mA, I_{D3} = 512 mA, P_{IN} = 25, 29 dBm, T_{BASE} = +85 ºC, T_{BASE} is back side of 20 mil CuMo carrier plate with AuSn die attached

Maximum Gate Current



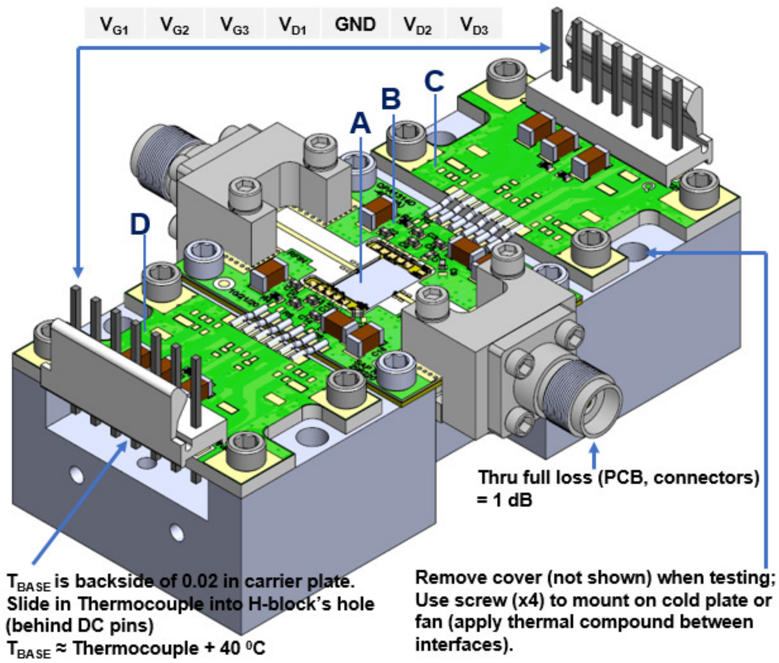
Channel Temperature is an IR scan equivalent

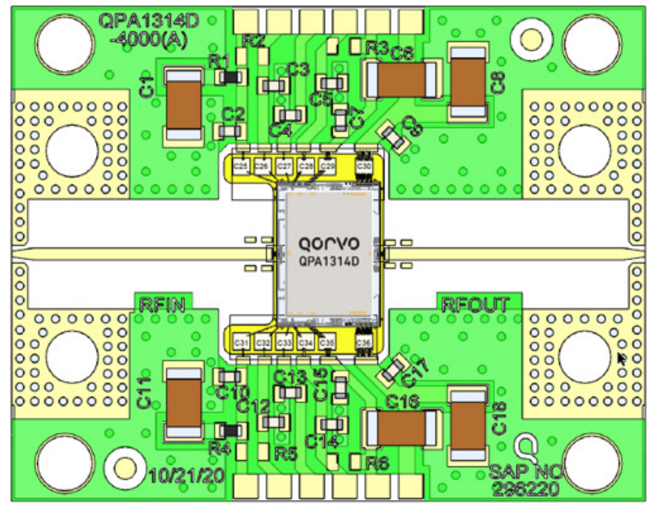
Applications Information



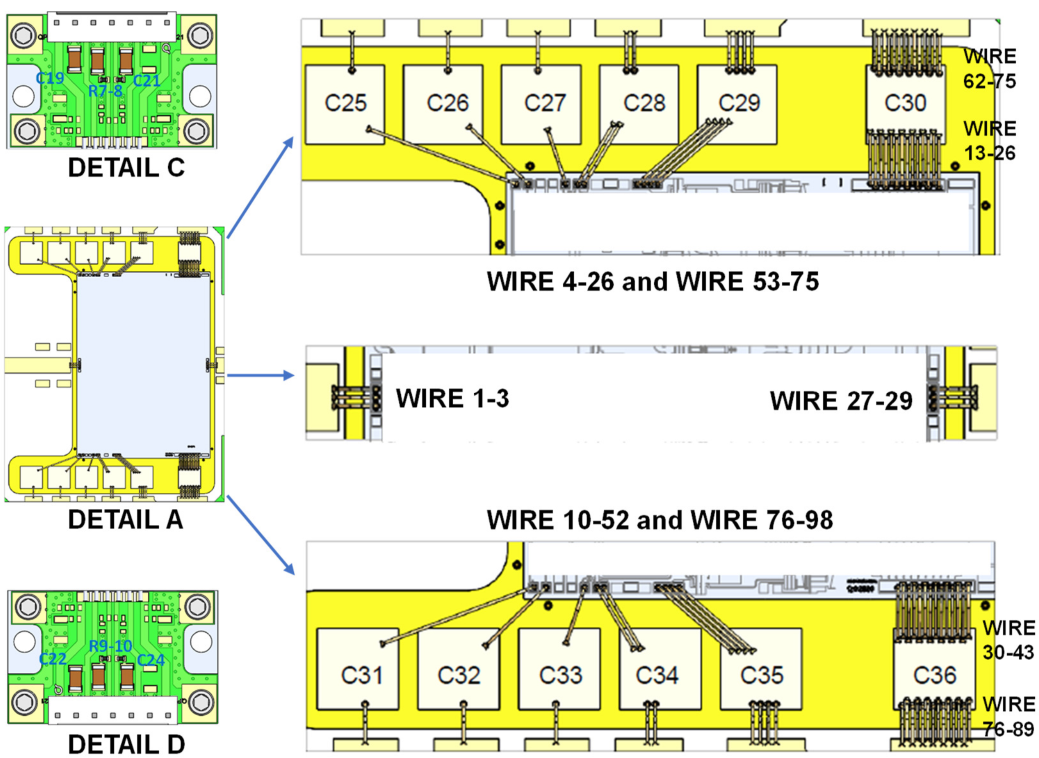
DC can be applied from top, or bottom, or both sides of the dies;
External bypassing required on both sides

Evaluation Board (EVB) Layout





DETAIL B



Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C6, C8, C11, C16, C18 – C24	12	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	
C2 – C5, C7, C9 – 10, C12 – C15, C17	12	0.01 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	
C25 – C36	12	10 nF	CAP, 10nF, ±15%, 30V, SLC, 0303	
R1, R4, R7 – R10	6	0 Ω	RES, 0 Ohm, JMPR, 0402	
PCB_MMIC	1		PCB for MMIC, Taconics RF-35HTC 0.01”, 0.5oz Ni/Pd/Au plating both sides, total thickness 0.14”	Qorvo, Custom
PCB,_Bias	2		PCB for DC Bias	Qorvo, Custom
H1, H2	2		CONN, HDR, Male-vert, 7 PIN, 1 RAW, MTA	
J1, J2	2		Connector, RF 2.9mm, F, Pin 0.005, Diel 0.029	Southwest Microwave 1092-01A-5
CP	1		Carrier Plate, CuMo, 0.9 x 1.15 x 0.02T	Qorvo, Custom
H-Block	1		H-Block, Copper C110, 1.14 x 2.49 x 0.59T	Qorvo, Custom
S1 – S4	4		Screw, Cap, Socket Head, 2-56X1/8”	
S5 – S12	8		Screw, Cap, Socket Head, 2-56X3/16”	
AuSn			AuSn Solder preform	
Epoxy			Epoxy preform	
Ablebond			Epoxy, Ablebond 84-1LMI	
Solder			Paste, solder, Syntech, Sn63/Pb37	
TC			Thermal Compound, Silver 5GR	Artic Silver 5 AS5-5G

.

Bias-Up Procedure

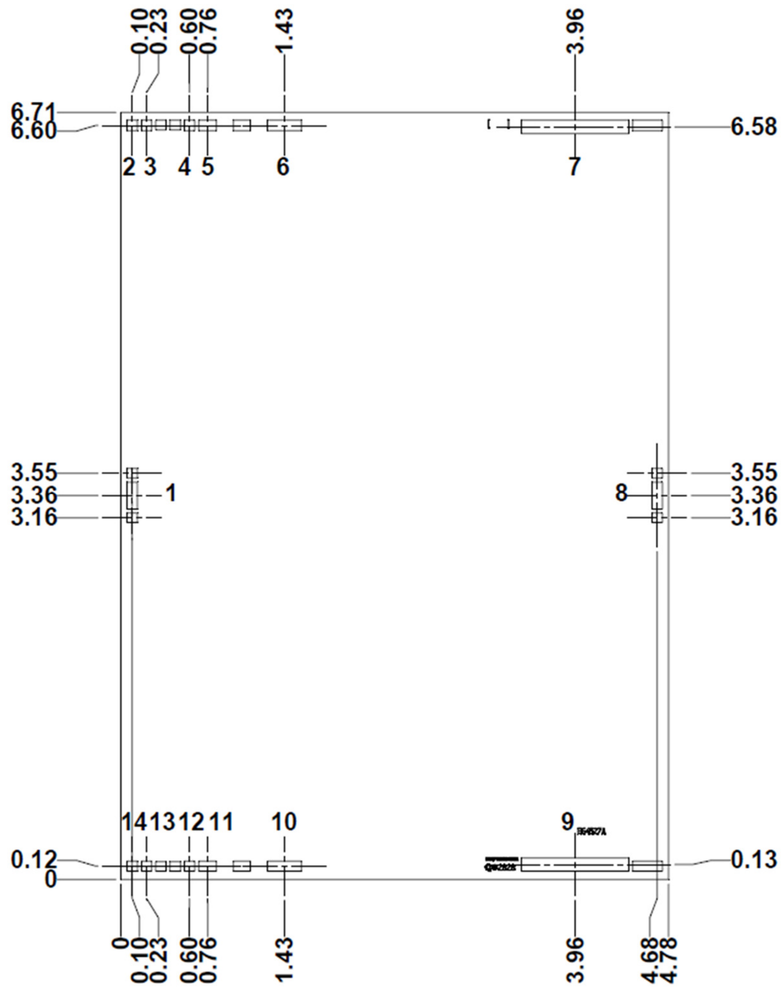
1. Set I_D limit to 9.5 A, I_G limit to 15 mA
2. Set V_{G12} to –5.0 V; V_{G3} to –5.0 V
3. Set V_D +24 V. Ensure I_{DQ} ~ 0 mA
4. Adjust V_{G12} more positive until I_{D12} = 168 mA; Adjust V_{G3} more positive until I_{D3} = 512 mA; $V_G \approx$ -2.3 V +/- 0.6V typical range
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to –5.0 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

If using three (3) bias supplies for V_D, V_{G12}, V_{G3}: combining all three V_D together, combining V_{G1} and V_{G2} as V_{G12}, adjusting V_{G12} to achieve $I_D = I_{D12}$, then adjusting V_{G3} to achieve I_{D3} where $I_D = I_{D12} + I_{D3}$

Mechanical Information



Dimensions: mm; Thickness: 0.10 mm; Die x, y size tolerance: ± 0.050; Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF_{IN}	0.09 x 0.24	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
2, 14	V_{G1}	0.09 x 0.09	Gate voltage for stage 1*
3, 13	V_{G2}	0.09 x 0.09	Gate voltage for stage 2*
4, 12	V_{G3}	0.09 x 0.09	Gate voltage for stage 3*
5, 11	V_{D1}	0.15 x 0.09	Drain voltage for stage 1*
6, 10	V_{D2}	0.30 x 0.09	Drain voltage for stage 2*
7, 9	V_{D4}	0.94 x 0.12	Drain voltage for stage 3*
8	RF_{OUT}	0.09 x 0.24	RF Output. Matched to 50 Ω, DC blocked, DC shorted to ground

* External bypassing required; refer to page 26 for recommendation

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001

Caution!

ESD-Sensitive Device

Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3 – 4 minutes, maximum.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- SVHC Free
- PFOS Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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