



APPLICATION NOTE

QPF4591

Wi-Fi 6 Dual Path Front End Module

Product Overview

This purpose of this application note is to help customers translate the layout and design guidelines for the Qorvo® QPF4591 dual path front end module.

The Qorvo® QPF4591 is an integrated front-end module (FEM) designed for Wi-Fi 6 (802.11ax) systems. The compact form factor and integrated matching minimizes layout area in the application.

Performance is focused on optimizing a multi-mode, multi-path PA for a 3.85V supply voltage that that allows for optimal throughput based on user conditions.

The QPF4591 dual path front end module features chipset-specific compatible control voltages to facilitate ease of use.

The QPF4591 integrates multiple 5 GHz power amplifiers (PA) with RF power detector, transmit-receive switches and bypassable low noise amplifiers (LNA) into a single device.

Product Details



Figure 1a. Device Packaging Detail

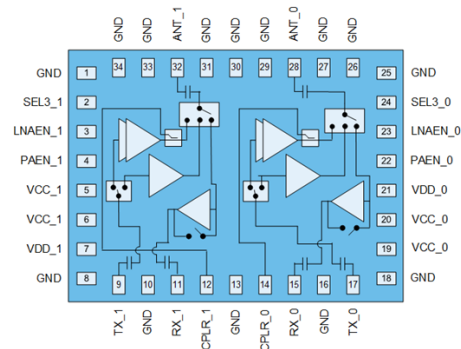


Figure 1b. Functional Block Diagram & Pin-Out Detail

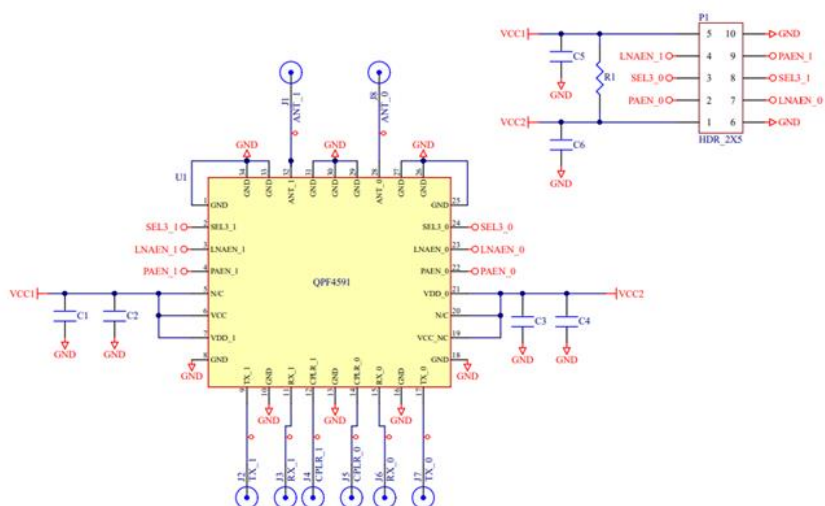
Table 1. QPF4591 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1	GND	No connection. This pin is not connected internally.
2	SEL3_1	Control pin.
3	LNAEN_1	Control pin.
4	PAEN_1	Control pin.
5	VCC_1	No connection. This pin is not connected internally.
6	VCC_1	Supply voltage.
7	VDD_1	Supply voltage.
8	GND	No connection. This pin is not connected internally.
9	TX_1	Chain 1 RF input. Internally matched to 50 Ω and DC blocked.

PIN NUMBER	LABEL	DESCRIPTION
10	GND	Ground connection.
11	RX_1	Chain 1 RF output from the low noise amplifier. Internally matched to 50 Ω and DC blocked.
12	CPLR_1	Chain 1 RF power detector. Provides an output proportional to the RF output power level.
13	GND	Ground connection.
14	CPLR_0	Chain 0 RF power detector. Provides an output proportional to the RF output power level.
15	RX_0	Chain 0 RF output from the low noise amplifier. Internally matched to 50 Ω and DC blocked.
16	GND	Ground connection.
17	TX_0	Chain 0 RF input. Internally matched to 50 Ω and DC blocked.
18	GND	No connection. This pin is not connected internally.
19	VCC_0	Supply voltage.
20	VCC_0	No connection. This pin is not connected internally.
21	VDD_0	Supply voltage.
22	PAEN_0	Control pin.
23	LNAEN_0	Control pin.
24	SEL3_0	Control pin.
25	GND	No connection. This pin is not connected internally.
26	GND	Ground connection.
27	GND	Ground connection.
28	ANT_0	Chain 0 RF bi-directional antenna port. Internally matched to 50 Ω and DC blocked Supply voltage
29	GND	Ground connection.
30	GND	Ground connection.
31	GND	Ground connection.
32	ANT_1	Chain 1 RF bi-directional antenna port. Internally matched to 50 Ω and DC blocked
33	GND	Ground connection.
34	GND	Ground connection.
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.
PIN NUMBER	LABEL	DESCRIPTION

Notes:

- Pin is DC blocked internally. There is no DC present on these ports. If connected to an external component with DC present, Qorvo® recommends using a 10 pF blocking capacitor.



Material	Layer	Thickness	Dielectric Material	Type	Comment
	Top Overlay			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
	Top Solder	0.0004in	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
Copper	Top Layer	0.0014in		Signal	
<i>Prepreg</i>		<i>0.0066in</i>	<i>RO4350B</i>	<i>Dielectric</i>	
Copper	Midlayer 2	0.0014in		Signal	
<i>Core</i>		<i>0.016in</i>	<i>FR-4</i>	<i>Dielectric</i>	
Copper	Midlayer 3	0.0014in		Signal	
<i>Prepreg</i>		<i>0.008in</i>	<i>FR-4</i>	<i>Dielectric</i>	
Copper	Bottom Layer	0.0014in		Signal	
	Bottom Solder	0.0004in	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
	Bottom Overlay			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.

Finished board thickness: 0.036in

REF. DES.	VALUE	DESCRIPTION	MANUF.	PART NUMBER
-	-	Printed Circuit Board		
U1	-	5GHz Wi-Fi Dual Path Front End Module	Qorvo	QPF4591
C5, C6	4.7 μ F	Capacitor, Chip, 20%, 16V, X7R, 0603	Murata	GRM188Z71C475ME21D
C1, C4	1 μ F	Capacitor, Chip, 20%, 16V, X7R, 0402	Murata	GRM155C81E105KE11D
C2, C3	1000 pF	Capacitor, Chip, 10%, 50V, X7R, 0402	Taiyo Yuden	UMK105B7102KV-F
R1	-	Do Not Install		

Recommended Biasing Sequence

Table 3. QPF4591 Logic Truth Table

MODE	PAEN	LNAEN	SEL3
Transmit High Power	High	Low	Low
Transmit Mid Power	High	Low	High
Transmit Low Power	High	High	High
LNA On Mode	Low	High	Low
Bypass Mode	High	High	Low
High Isolation Mode	Low	Low	Low
Not Supported	All Other States		

Notes:

1. The QPF4591 logic control and RF input is required to ensure optimal performance and reliable operation. See turn on/off procedure below.

Transmit High Power Mode Power-On Procedure:

1. Connect Power Supplies in OFF mode (0V) to VCC, VDD, and PA_EN pins.
2. Apply +3.85V to VCC, VDD pins.
3. Apply control voltages (0V to LNA_EN and SEL3 and apply +1.8V to PA_EN pin).
4. Apply RF input signal to TX, transmit RF; measure RF output on ANT.
5. RF Coupler Power detector can be monitored on CPLR.

Transmit Power-Off Procedure:

1. Remove RF input signal.
2. Set all control signals (PA_EN) to 0V.
3. Set the Power Supply Voltages on VCC, VDD to 0V.

Transmit High Power Mode Timing Diagram Power ON/OFF Sequence

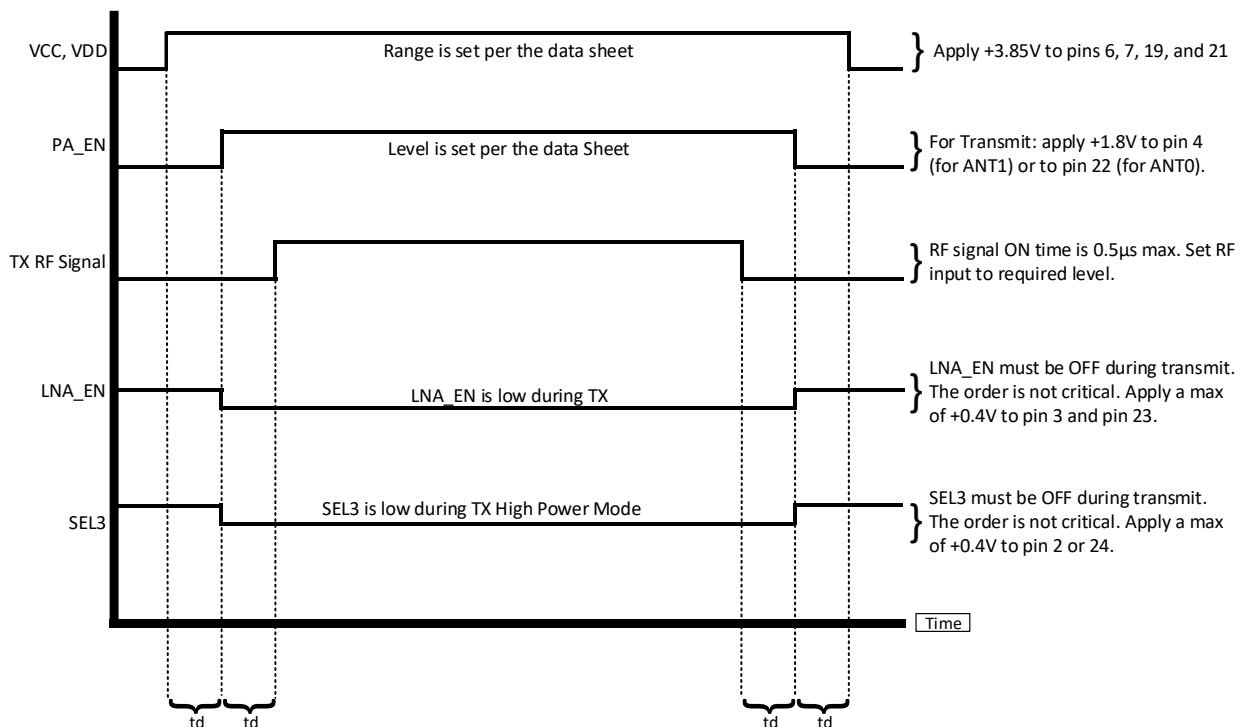


Figure 3a. QPF4591 Transmit Timing Diagram

Notes:

1. RF Signal for each specific mode is applied after the DC bias is applied.
2. Total ON/OFF time includes from 10% of control switching to 90% of RF power.
3. For "td" value, please refer to the turn ON/OFF time shown in the QPF4591 datasheet specification table. The maximum is 0.5 μs for each mode.

System Architecture Application Circuit Recommendations

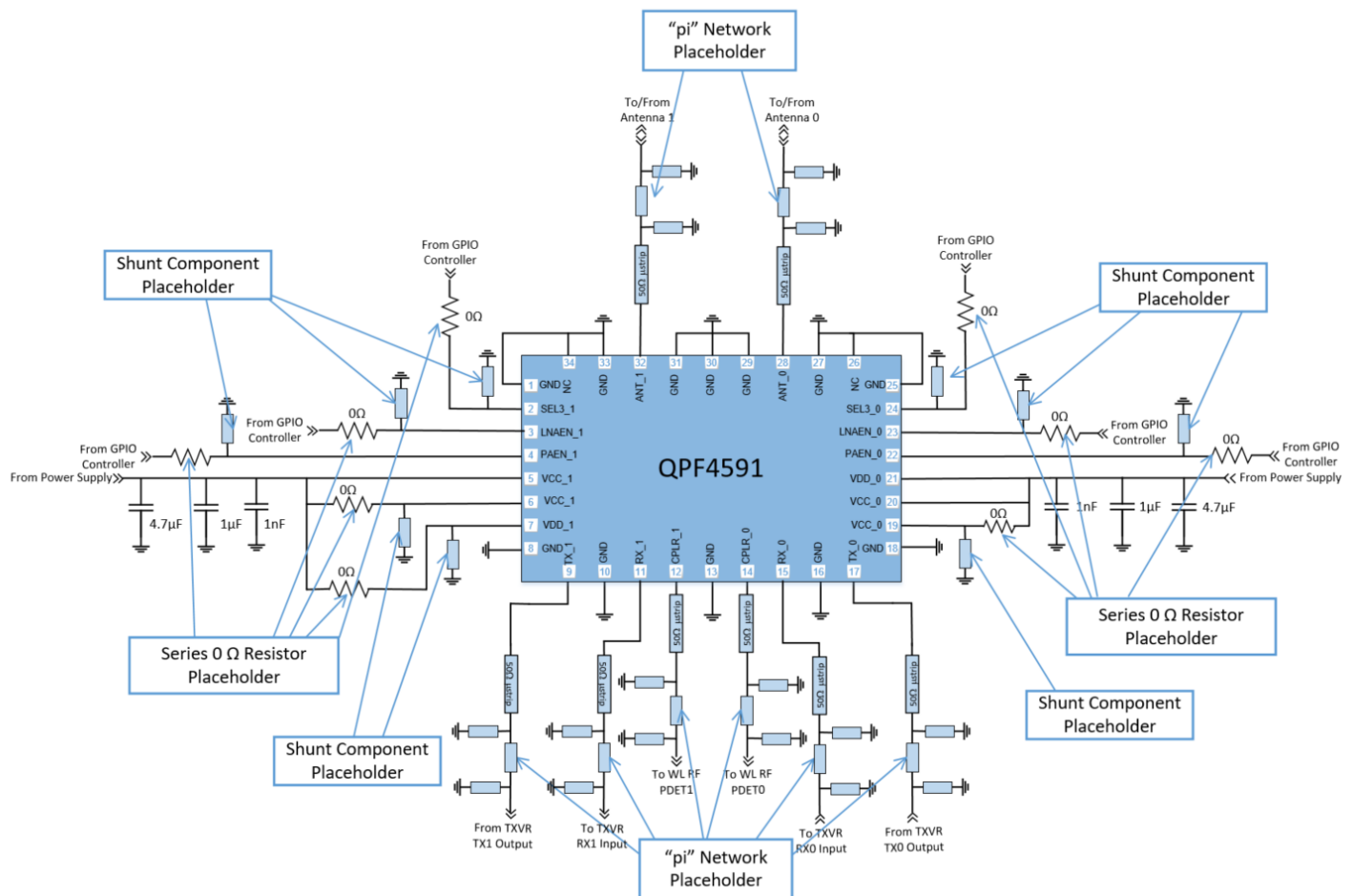


Figure 4a. Recommended Application Circuit in a System

1. The above schematic shows recommended bypassing values based on the QPF4591 evaluation board. The customer should ensure that sufficient bypassing is provided based on their PCB layout. In addition, one should ensure all bypass capacitors are placed as close as possible to respective FEM pins, with the lowest values placed closest to the part pin. It is also recommended that at least one ground via be placed right next to each bypass capacitor ground pad to minimize ground return inductance between the capacitor and the FEM ground. Qorvo® recommends using 150 pF bypass capacitor value on pin 9 (PA_EN) to avoid any ESD latch-up issue due to fast switching response from transceiver GPIOs.
2. In case there is DC present on the lines connecting RF paths on the board, we recommend using DC block per the recommended values in the schematic. There is no DC present on RF ports of FEM internally. Low value external DC blocking capacitors, however, can be beneficial for improving ESD immunity and overall ruggedness in the presence of transients. The capacitor values should be chosen to be series resonant at approximately mid band per the component manufacturer datasheet.
3. RF Power Detectors (pins 12 and 14) should not be left floating if not being used and instead terminated into 50 Ω.
4. Qorvo® suggests including a series element on customer's layout at the output of RF_PDET (pins 12 and 14) to have a flexibility of low pass filter, if required.

5. Qorvo® recommends using a “pi” network placeholder for tuning flexibility at TX, RX, and ANT ports. In addition, try to place tuning placeholder close to FEM. Transceiver (TXVR) matching components should be placed closer to TXVR with 50 Ω trace connecting to “pi” network placeholder near to FEM Input.
6. NC is no connect and can be left floating or grounded on the board. Grounding this pin can add better mounting integrity. If grounding, we suggest to GND it close to FEM pin.
7. Route control lines on a separate layer, other than the signal layer, whenever possible and isolate control line traces from RF and VCC traces. Keep a minimum distance of 150 μm between TX and RX control lines to minimize coupling.
8. Having a placeholder for a series component on PA_EN, LNA_EN, and SEL3 control lines provides a way to improve isolation.
9. Qorvo® recommends to fully populate the ground slug with as many thermal vias as possible and to add ground vias around RF traces.
10. Qorvo® recommends following the evaluation board layout guidelines as close as possible. QPF4591 evaluation board uses 16 mil diameter vias with 8 mil hole size under the FEM. Gerber files are available upon request.
11. When in operating mode, ensure ANT port on system board is always terminated and Wi-Fi chipset drive going into FEM input does not exceed FEM recommended operating range to avoid any damage.

PCB Layout Considerations

Board layout must be carefully considered to achieve optimal performance from any FEM, including the QPF4591. In addition to providing connectivity between the FEM and external components, the PCB layout is a part of the overall circuit. The RF and DC parasitic of the traces, along with coupling between traces, must be evaluated. The QPF4591 Evaluation Board PCB layout guidelines provides a good starting point for designing the layout in the actual application.

RF Traces

All the PCB traces between the RF pins and matching networks (where applicable) should be 50 Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. The RF traces should be routed on the top layer to minimize coupling with other RF, control input, and DC traces. If it is not possible for some reasons to route RF traces on top layer, we suggest making sure there is proper isolation between traces on the layout to avoid any coupling issues. RF lines should be isolated from other RF and DC signals by adding solid ground planes (with vias) between them to minimize coupling or cross-talking. In addition, we also recommend reducing RF trace lengths, wherever possible.

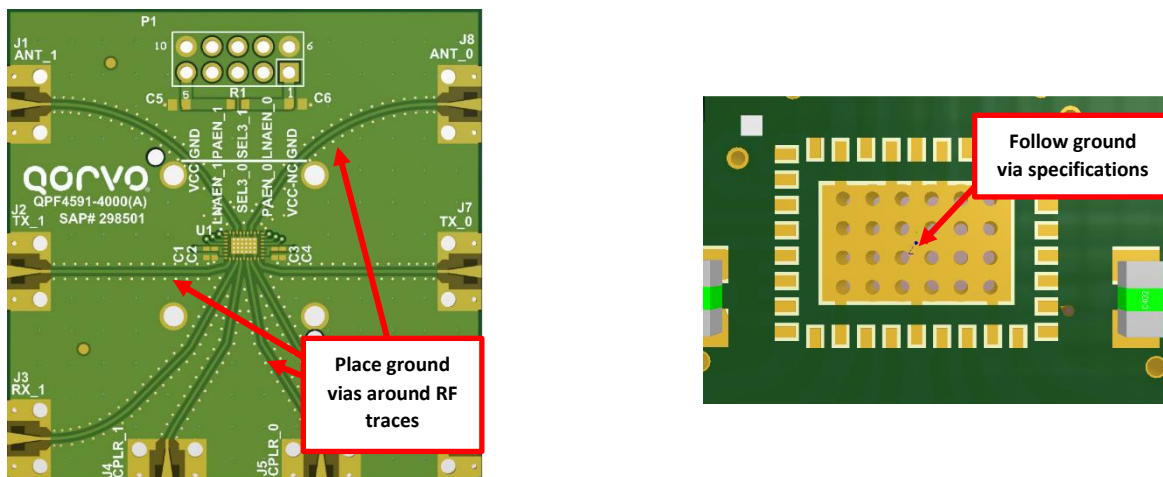


Figure 5a. Recommended PCB layout Considerations – Ground vias

Grounding Considerations

Connect the module center ground pad directly to main ground plane layer using as many vias as possible. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible. This ground layer also provides the reference layer for microstrip lines.

Particular attention should be paid to the grounding of the PA ground slug, the solid metalized area on the bottom side of the package. This serves as the primary RF and DC ground return for the entire PA, as well as the primary path for heat removal. A larger number of via holes should be distributed over the entire ground area below the PA to provide good RF and DC ground returns, as shown in **Figure 5b** below. Additionally, the vias will serve as a low resistance thermal path between the PA and the PCB. Vias passing through multiple copper layers provide the best overall RF, DC, and thermal performance.

Ensure proper vias on ground slug / paddle for better thermal consideration. QPF4591 ground slug / paddle has special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduct path for heat dissipation. The GND pad and vias pattern and size used on the Qorvo® evaluation board should be replicated. The Qorvo® layout files in Gerber format can be provided upon request.

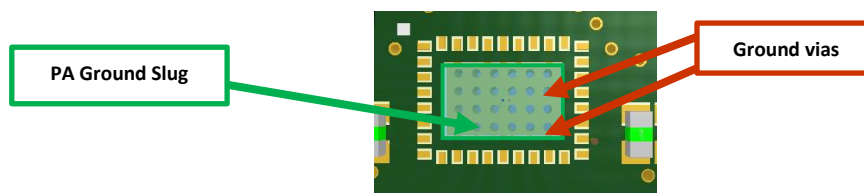


Figure 5b. Recommended PCB layout Considerations – Via Placement on Module Ground Slug

DC Layout Considerations

The most important layout consideration for the VCC DC traces is that they provide low impedances back to their main supply rail. Where possible, power planes should be used to route these traces. Where this is not possible due to space constraints, the traces should be made as wide as possible, using multiple copper layers if necessary, to achieve an equivalent width of 2 mm or more.

There should be at least one ground layer between these traces and any RF traces even though both are running diagonal to each other on different layers to minimize coupling.

When connecting all VCC pins on the board together, we recommend connecting VCC and VDD pins (pin 5, 6, 7, 19, 20, and 21) before bypass capacitors as shown in **Figure 5c**. In addition, we suggest running a longer trace for better isolation.

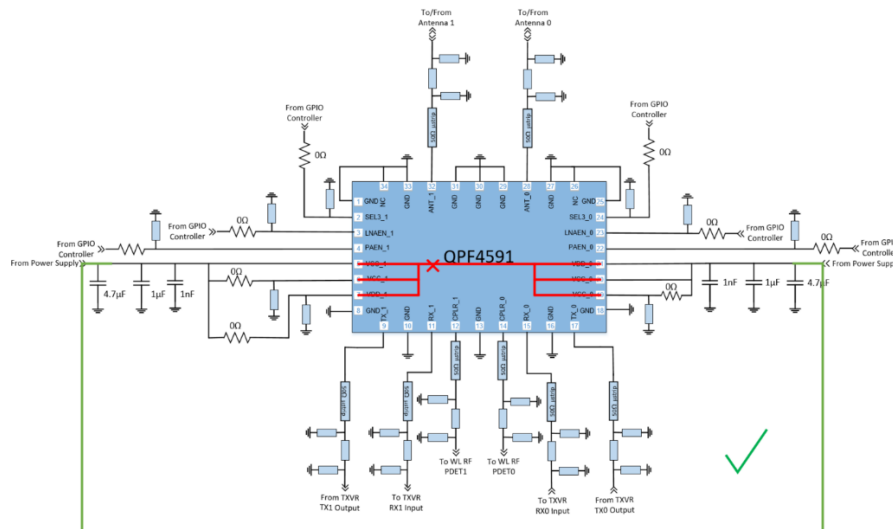


Figure 5c. Recommended PCB layout Considerations – Connecting VCC and VDD Pins

PCB Footprint Recommendations

See **Figures 6a and 6b** below for the Qorvo® recommended package outline drawing and solder mask patterns.

Land Pattern Recommendation

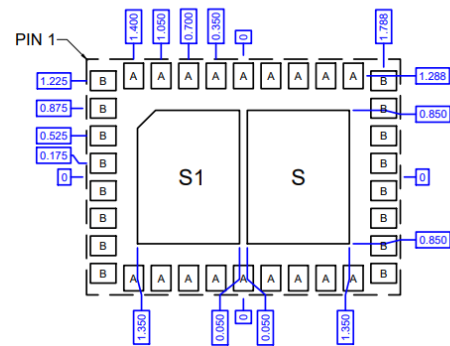
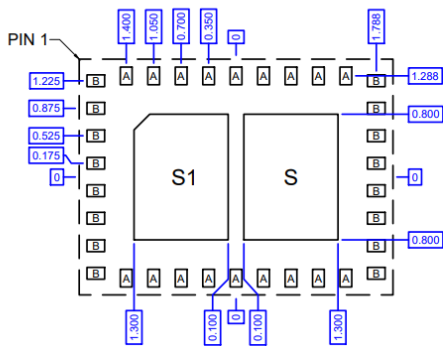
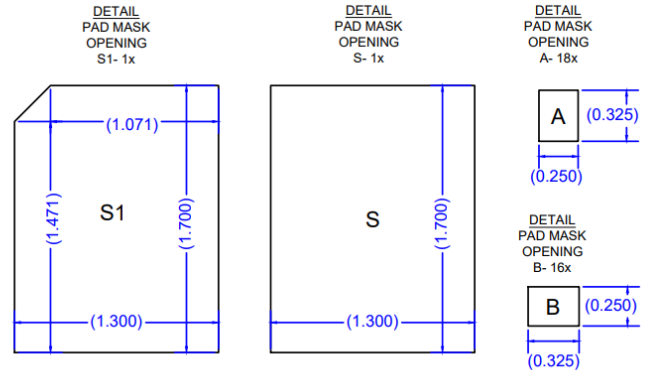
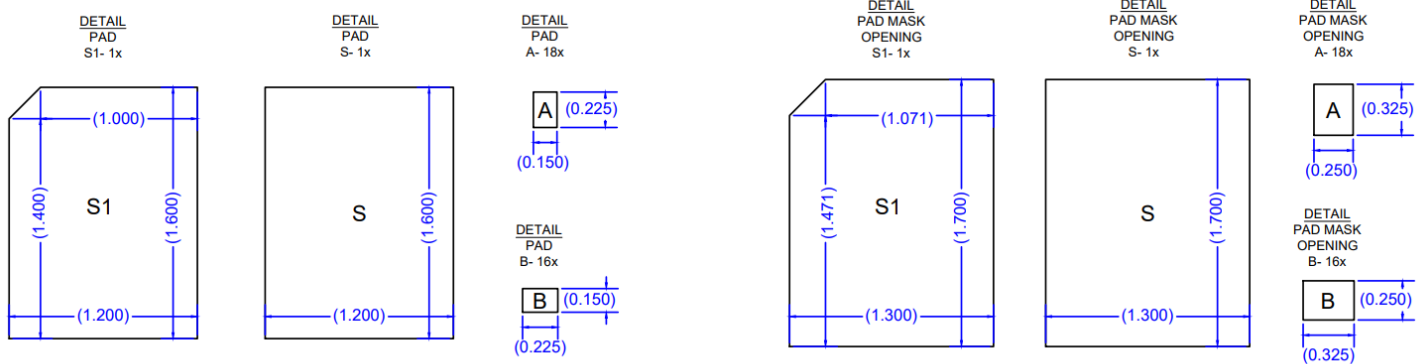


Figure 6a. PCB Footprint Recommended Landing Pattern

Figure 6b. PCB Footprint Recommended Solder Mask Pattern

Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Package Information

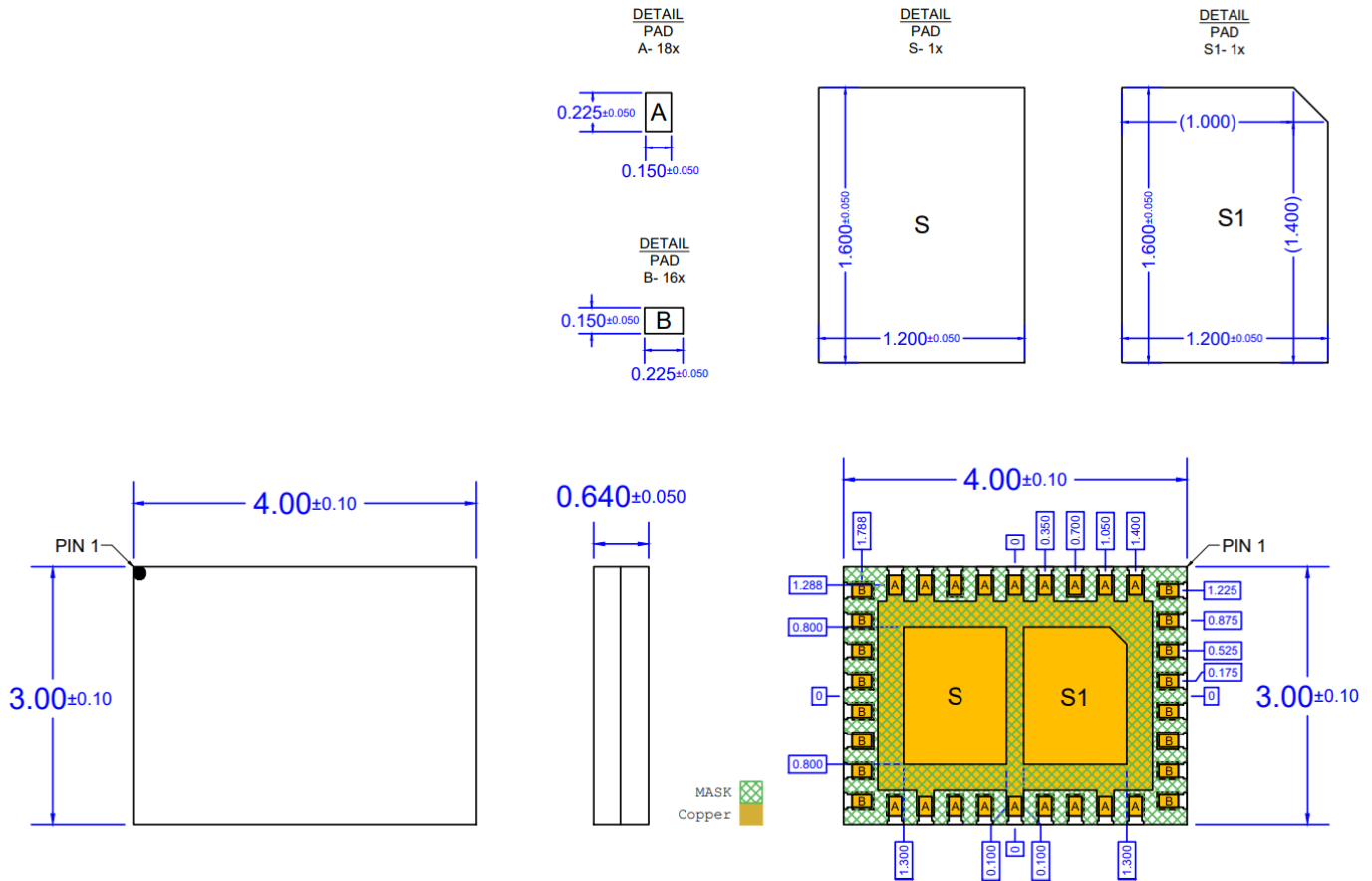


Figure 6c. QPF4591 Marking Diagram

Figure 6d. QPF4591 Package Outline Drawing

Package Style: Laminate
Dimensions: 4.00 x 3.00 x 0.640 mm

Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo® evaluation board for this product.
3. Some modifications may necessary to suit end user assembly materials and processes.

Reflow Profile & Solder Paste

Solder Reflow Recommendation

This information is provided as a guideline to facilitate the successful implementation of a surface mount process customized to the user's requirements.

Solder Reflow Equipment

Recommendations provided are based on a 100% convection reflow oven capable of maintaining temperatures specified in Joint Industry Standard IPC/JEDEC J-STD-020.

Reflow Profile Notes

An optimized reflow profile depends on several factors such as the solder paste, board density and type of reflow equipment used. Additional reflow information can be obtained from solder paste vendor data sheets.

It is recommended that any reflow profile be characterized with a fully populated production PCB. Thermocouples can be used to record temperatures across the surface and any sensitive components on the PCB. Ensure that a thermocouple is placed in contact with the top surface of any moisture sensitive component to ensure maximum temperature is not exceeded.

High Temperature Reflow Profile

Maximum reflow temperature is 260 °C. The temperature used to classify the MSL level appears on the MSL label on each shipping bag. Qorvo® uses reflow profiles in accordance with IPC/JEDEC J-STD-020 for qualification with the exception of the maximum reflow temperature of 260 °C.

Table 4. Qorvo® Recommended Reflow Profile & Conditions

CONDITIONS	
Ramp-up rate	3 °C/second max.
Preheat temperature 175 (±25) °C	180 seconds max.
Temperature maintained above 217 °C	60-150 seconds
Time within 5 °C of actual peak temperature	20-40 seconds
Peak temperature range	260 +0/-5 °C
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤3
Pre-baking requirements	Refer to JEDEC J-STD-033 if original device package is unsealed.
Maximum reflow temperature	260 °C

Table 5. Qorvo® Recommended Low Temperature Solder Paste Specifications

SPECIFICATIONS	
Solder paste	Multicore RP11
Alloy type	Sn62/Pb36/Ag2
Metal content	89.5%
Solder particle size	45 µm to 20 µm

Table 6. Qorvo® Recommended High Temperature Solder Paste Specifications

SPECIFICATIONS	
Solder paste	Multicore 96SCAGS89 (CR39)
Alloy type	Sn95.5/Ag3.8/Cu0.7
Metal content	88.5%
Solder particle size	45 µm to 20 µm

A no-clean solder paste is recommended since it is difficult to completely clean residues under low profile components after they have been soldered to the PCB. Eliminating residues reduces the possibility of solder bridging between non-connected pads. This condition is affected by time, temperature, and humidity and will not be visible during initial inspection after reflow.

Inspection

It is recommended that x-ray inspection be performed for any solder joints that are not visible after assembly. The following analysis and inspection criteria have been shown to result in component attachments that pass all Qorvo® package qualification procedures:

- Evaluate solder paste printing process. Measure print height, and paste slump.
- Perform visual inspection for excess solder on terminal pads before and after reflow.
- Perform x-ray to inspect for proper alignment, solder voids, solder balls, and solder bridging after reflow.
- Check for a minimum of 90% solder coverage on pad.
- There should be sufficient solder coverage on ground pads and I/O.
- Inspect for solder bridging or splatter between I/O pads.

Support Data

For any further data on the QPF4591, please request Qorvo® point of contact such as marketing, sales or a representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo® for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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