



Application Note Pre-Charge Circuit

Power Application Controller® Battery Management



1 PRE-CHARGE CIRCUIT

1.1 Why use a Pre-Charge circuit?

In many large battery cell count battery applications (>10 cells in series), the inrush current should be managed. If the inrush current exceeds component limits, overtime it will result in failure of semiconductor devices, inductors, connectors, traces, and switches.

High cell count battery systems often use pre-charged circuits to limit inrush current prior to the main discharge MOSFET turning on which connects the load to the battery. Controlling this inrush current with a pre-charge circuit protects the system from damage, extends lifespan, and increases reliability.

A pre-charge circuit between a battery and its load is required if any of the following are issues:

- The short circuit protection will activate (nuisance tripping) by the inrush current
- The battery cells have too high impedance for the inrush current
- The load has input capacitors will be damaged by the inrush current
- The main fuse will blow if asked to carry the inrush current

Usage of a Pre-Charge circuit will increase reliability, prevent nuisance issues, and provide safe operation of the system.

1.2 Pre-Charge Circuit Application & Advantage's

It has become common place to use a Pre-Charge circuit with motor applications. For example, when there is a high capacitive load, such as a motor in an electric Bicycle (eBike), a large peak current would occur when the main protection MOSFETs are closed. This would trip the short circuit protection or damage the inline fuse. It could also exceed the safe operating area (SOA) of the protection FET and put excess stress on other components.

In other application cases, contactors are used to connect these high loads, and due to the inrush current, the contacts get damage due arch.

When initially connecting a battery to a load with capacitive input, there is an inrush of current as the load capacitance is charged up to the battery voltage. With large batteries that have a low source impedance and with large capacitance at the load, this inrush current can easily peak 100 times the normal operating current.

A pre-charge circuit limits that inrush current, without limiting the operating current.

1.3 How Pre-Charge Circuit Works

In typical Pre-Charge circuit, it starts at the detection of the load being attached. The system will begin the pre-charge of the load capacitor with a current limited path. This limited current is selected to charge the load capacitor over a period of time such that the delay is not noticeable by the user of the application and below any component limits. Once the load capacitance is charge to almost equal to the battery voltage the main protection discharge MOSFET is turned on and the pre-charge circuit is turned off. Failure to turn on the main discharge MOSFET will prevent the application from being able to run as the pre-charge path cannot support the full load current.

1.4 Example of Firmware Code

For a typical Pre-Charge Circuit, follow these steps. Controller introduces two new states in BMS flow

- 1st state is Pre-Charge Start
- 2nd state is Pre-Charge Complete *config_pre_chg_fet_control_io(void)* function called during

peripheral_init(void) to setup GPIO pin.

- 1) Pre-Charging Start: System detects a load being connected
- 2) System measure voltage at load.
 - a. If the voltage is not within range, start pre-charge via GPIO output by calling *turn_on_pre_chg_fet_control_io(void)*.
- 3) *turn_on_pre_chg_fet_control_io(void)* function call will energize Pre-Charge Circuit pre-charge circuit turns on, load capacitor begins charging.
- 4) System measure voltage at load.
 - a. When the voltage is within range near VBAT, stop pre-charge via GPIO output by calling *turn_off_pre_chg_fet_control_io(void)*.
- 5) Controller enters Pre-Charge Complete state and turns main discharge (DSG) MOSFET on, 6) The system is ready to run the load.

```

void peripheral_init(void)
{
    // Initialize PLL, Clocks, Flash
    init_system();

    // Configure communication ports
    config_comm();

    // Configure SOC Bridge for talking to AFE
    pac_tile_socbridge_config(1, 0);

    // configure_cafe_fault_interrupt();
    configure_adc_emux_engine();

    configure_adc_sequencer();

    // Start ADC
    pac_adc_start();

    // Initialize BMS timerC
    config_bms_timer();

    // Initialize systick timer
    config_systick_timer();

    // Configure CHG/DSG FET IO control
    config_fet_control_io();

    // Configure AFE ADC IO status
    config_afeadc_status_io();

    // Configure PRE-CHG MOSFET IO
    config_pre_chg_fet_control_io();
    turn_off_pre_chg_fet_control_io();

    // config_debugio();
    #if (ENABLE_WATCHDOG == TRUE)
        // Enable Watchdog
        init_watchdog_time_base();
    #endif
}

/**
 * @brief Configure MCU IO which control PRE CHG FET Circuit
 */
void config_pre_chg_fet_control_io(void)
{
    PAC_GPIOE->OUT.P0 = 0;
    PAC_GPIOE->OUTEN.P0 = 1;
}

/**
 * @brief Turn off PRE CHG FET IO
 */
void turn_off_pre_chg_fet_control_io(void)
{
    PAC_GPIOE->OUT.P0 = 0;
}

/**
 * @brief Turn on PRE CHG FET IO
 */
void turn_on_pre_chg_fet_control_io(void)
{
    PAC_GPIOE->OUT.P0 = 1;
}

```

1.5 Example circuitry shows the arrangement

For implantation Q1 should be driven by any GPIO that can source voltage above the desired turn on threshold of Q1. Q1 should have a VDS breakdown above the maximum of VBAT. Q2 needs to be able to source the desired current, which is limited by R1 emitter resistor, ensure that both are rated at the desired power rating. R2 and R3 setup the Q2 turn on Vbe and limit the current for Q1. R5 is to ensure Q1 is off during power up and initialization. R4 is to limit gate transients, and control slew of Q1 gate.

Figure 1-1 Example Circuitry

Q1 = IRF640NPBF

Q2 = KSB546YTU

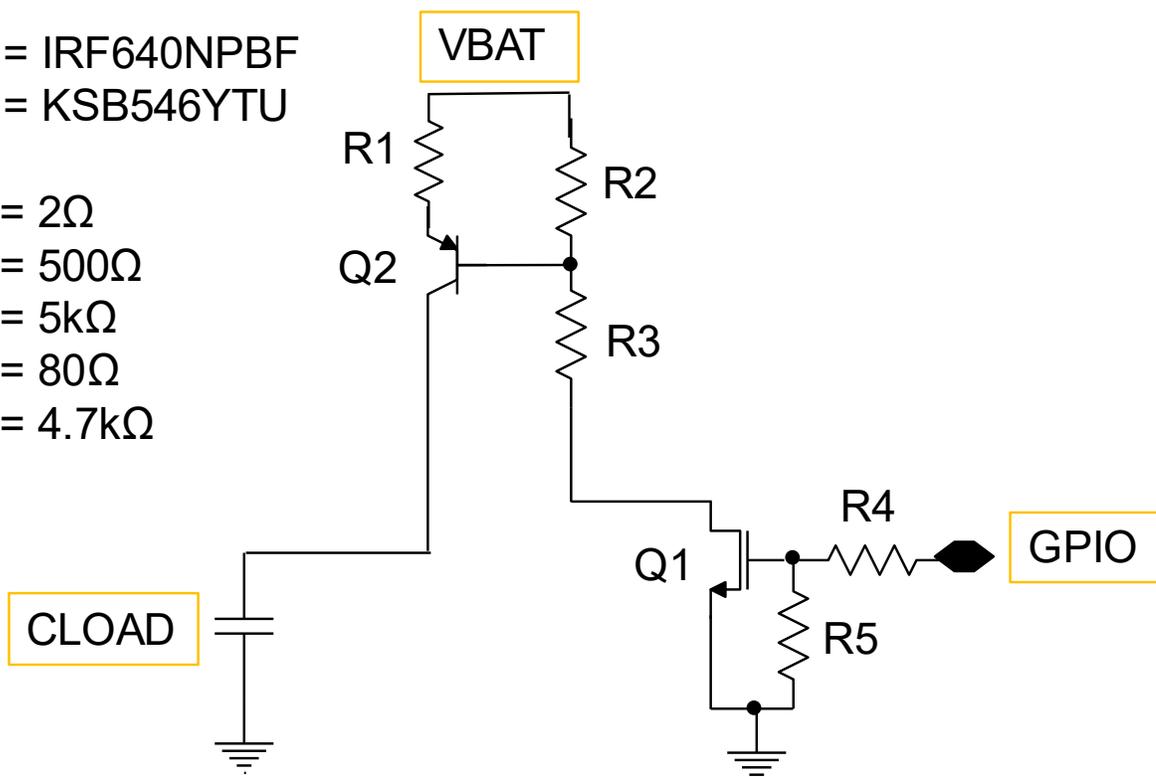
R1 = 2Ω

R2 = 500Ω

R3 = 5kΩ

R4 = 80Ω

R5 = 4.7kΩ

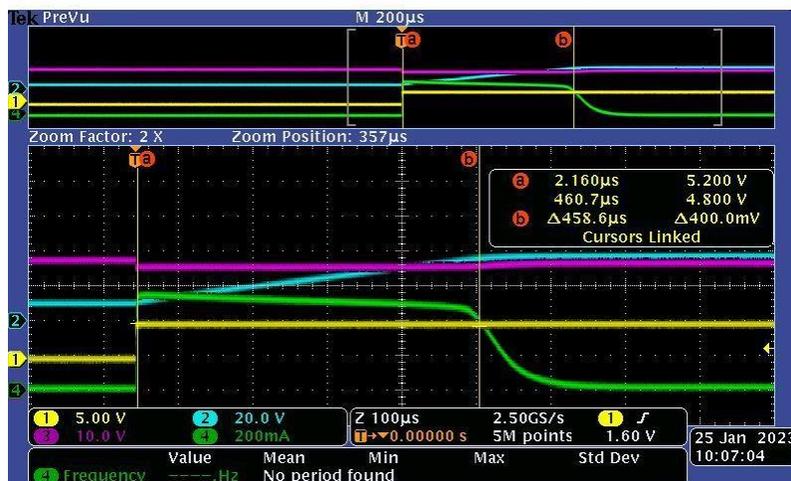


1.6 Example Waveforms

The next three figures show the operation of the example circuitry

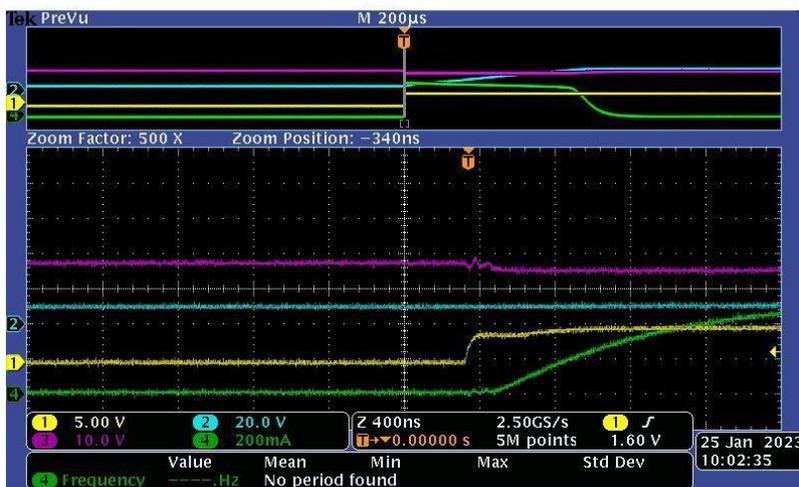
- 1) GPIO
- 2) CLOAD.
- 3) Q2 Base
- 4) Q2 Collector Current

Figure 1-2 Turn On



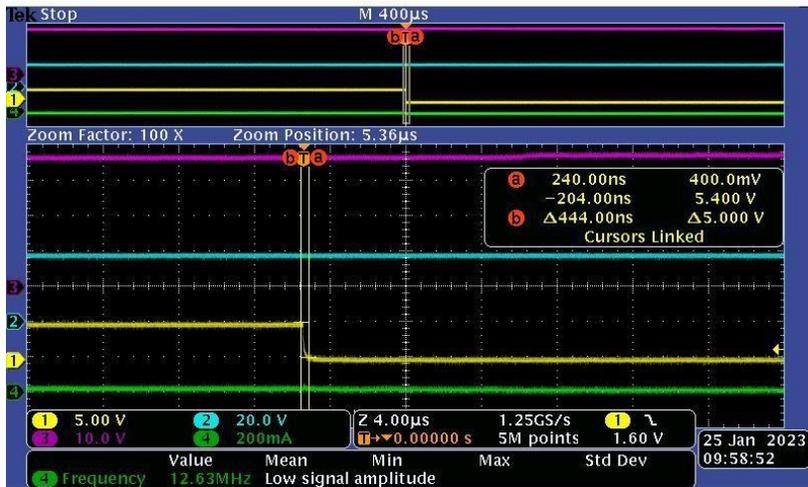
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Figure 1-3 Turn On zoomed in on starting edge



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Figure 1-4 TURN OFF



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1.7 LEGAL INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

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