Application Note PAC2xxxx BMS Parallel FET Operation

Power Application Controller® Battery Management

1 PAC2xxxx BMS Devices

The Qorvo® PAC2xxxx are a family of Intelligent Battery Monitoring System (BMS) that can monitor 10-series to 20-series Li-Ion, Li-Polymer and LiFePO4 battery packs. They integrate a FLASH-programmable MCU, Power Management, Current/Voltage/Temperature Sense and drive circuits for charge/discharge FETs and protection fuses. It can communicate using UART, SPI I2C/SMBus serial interfaces. The devices provide access to multiple analog and digital peripherals required to manage today's high cell count battery packs.

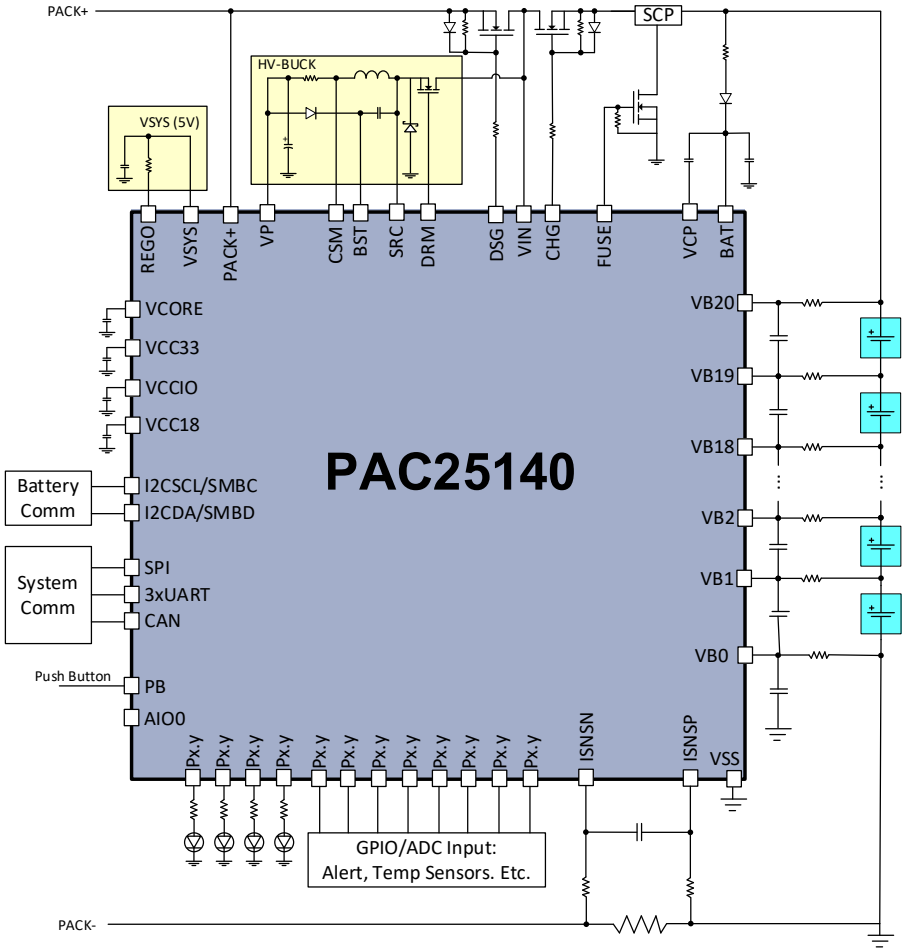

Figure 1 Standard Series FET Arrangement

1.1 What is BMS Parallel FET Operation?

In many large battery cell count battery applications (>20 cells in series), the system may have a high discharge current and will use parallel FETs, aka split FET operation. For such systems that want to improve efficiency and reduce FET heating, splitting the Charge and Discharge path will provide such gains. Figure 2 shows such arrangement. One advantage is now the Charge FET path is no longer involved for the Discharge path. Many systems may use a higher RDSon FET in the Charge path to save BOM cost due to the charge current being much lower than the discharge load current. Additionally, now the heating of the FETs can be reduced since only one FET is passing current when in Discharge. A third advantage is both a charger and a load can be connected in parallel. In the arrangement below, the battery is the main supply, if the charger is to provide power instead then the VIN node should be connected between the diode and charge FET on the PACK+ line.

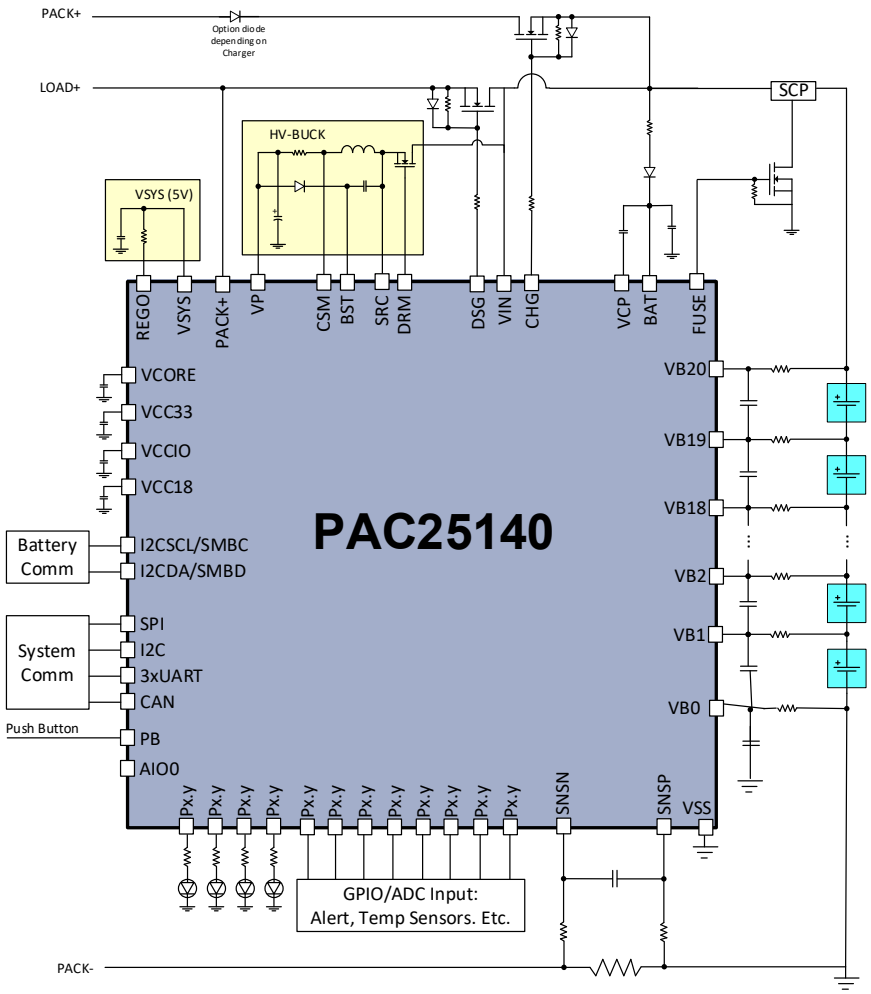

Figure 2 Parallel FET Arrangement

1.2 BMS Parallel FET Operation Simple Calculations

Example:
VPACK = 80V,
Rfet(ON) = 10mΩ
Load = 60A

Power Dissipation in Series FETs $P = I^2 \times R = 60^2 \times (2*0.01) = 72W$
Power Dissipation in Parallel FETs $P = I^2 \times R = 60^2 \times 0.01 = 36W$

If the FETs have a 4W/°C then the FET temperature would increase 9°C. Therefore, in the series configuration both FETs are heat generators versus only one.

1.3 BMS Parallel FET Operation Firmware Considerations

In a system with Series FETs the firmware FET fault handling needs to account for current direction. However, in a Parallel FET configuration the FETs faults do not need to account for current direction due to the FETs being in parallel. The FETs control independent paths.

Table 1: Series FETs state with Software fault handling

No	Fault	Battery State					
		CHARGE		IDLE		DISCHARGE	
		Charge FET (CFET)	Discharge FET (DFET)	Charge FET (CFET)	Discharge FET (DFET)	Charge FET (CFET)	Discharge FET (DFET)
1	Cell under voltage (CUV)	ON	ON	ON	OFF	**OFF**	**OFF**
2	Cell over voltage (COV)	**OFF**	**OFF**	OFF	ON	ON	ON
3	Discharge over current (DOC)	-	-	-	-	**OFF**	**OFF**
4	Charge over current (COC)	**OFF**	**OFF**	-	-	-	-
5	Discharge over temperature (DOT)	-	-	-	-	**OFF**	**OFF**
6	Discharge under temperature (DUT)	-	-	-	-	**OFF**	**OFF**
7	Charge over temperature (COT)	OFF	ON	-	-	-	-
8	Charge under temperature (CUT)	OFF	ON	-	-	-	-
9	IC over temperature (IOTF)	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**
10	Cell undervoltage lockout (UVLO)	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**
11	Cell overvoltage lockout (OVLO)	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**
12	Cell missing	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**
13	Cell delta voltage	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**	**OFF**
14	Current End-Of Charge (IEOC)	OFF	ON	-	-	-	-

Table 2: Parallel FETs state with Software fault handling

No	Fault	Battery State	
		CHARGE/IDLE/DISCHARGE	
		Charge FET (CFET)	Discharge FET (DFET)
1	Cell under voltage (CUV)	ON	**OFF**
2	Cell over voltage (COV)	**OFF**	ON
3	Discharge over current (DOC)	ON	**OFF**
4	Charge over current (COC)	**OFF**	ON
5	Discharge over temperature (DOT)	**OFF**	**OFF**
6	Discharge under temperature (DUT)	**OFF**	**OFF**
7	Charge over temperature (COT)	**OFF**	ON
8	Charge under temperature (CUT)	**OFF**	ON
9	IC over temperature (IOTF)	**OFF**	**OFF**
10	Cell undervoltage lockout (UVLO)	**OFF**	**OFF**
11	Cell overvoltage lockout (OVLO)	**OFF**	**OFF**
12	Cell missing	**OFF**	**OFF**
13	Cell delta voltage	**OFF**	**OFF**
14	Current End-Of Charge (IEOC)	**OFF**	ON

- Means this fault will not occur in the current Battery State.

1.4 BMS Parallel FET Operation Lab Results

To confirm safe operating conditions the following test were performed in the LAB with a modified EVK.

CASE	Test Description	Test condition		Comments	Result
		Temp	VIN/BAT		
1	General Operation	Room	VIN=51V VBAT=47V	Use resistor divider to simulate battery	PASS
2	Single Control Driver, No Load	Room	VIN=51V VBAT=47V	Use resistor divider to simulate battery	PASS
3	Single Control Driver, Have Load	Room	VIN=51V VBAT=47V	Use resistor divider to simulate battery	PASS
4	Control FETs while charging and discharging	Room	VIN=51V VBAT=47V	Use resistor divider to simulate battery	PASS
5	Control FETs while charging and discharging	Room	20 Cells	Real Battery	PASS

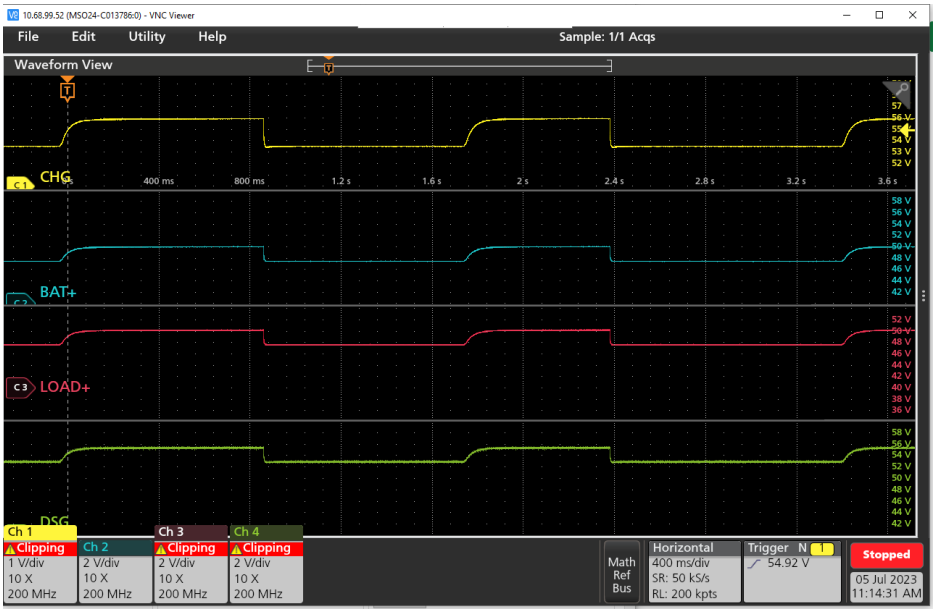

Figure 3 Parallel FET Plug/UnPlug Adapter 1.4A charging, 1A load

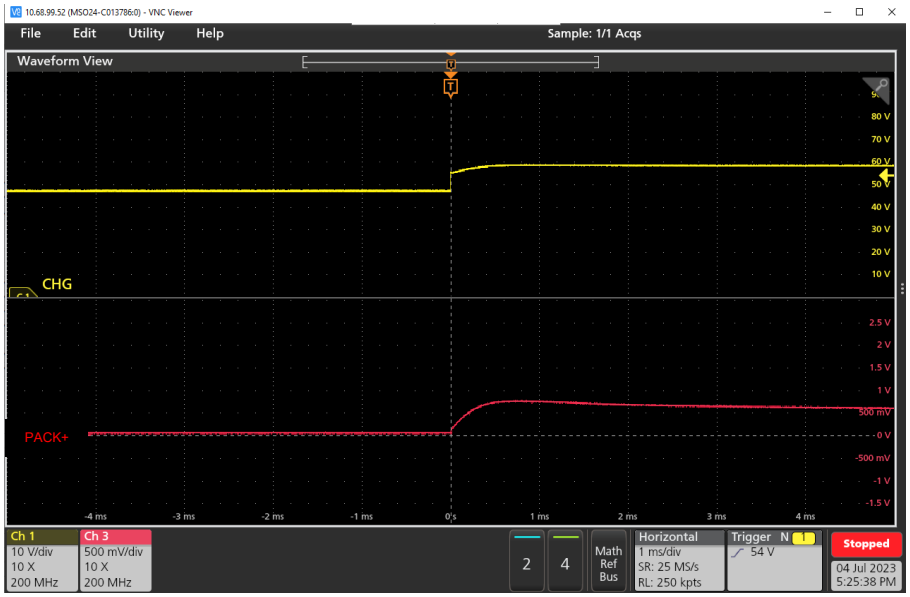

Figure 4 Parallel FET CHG ON

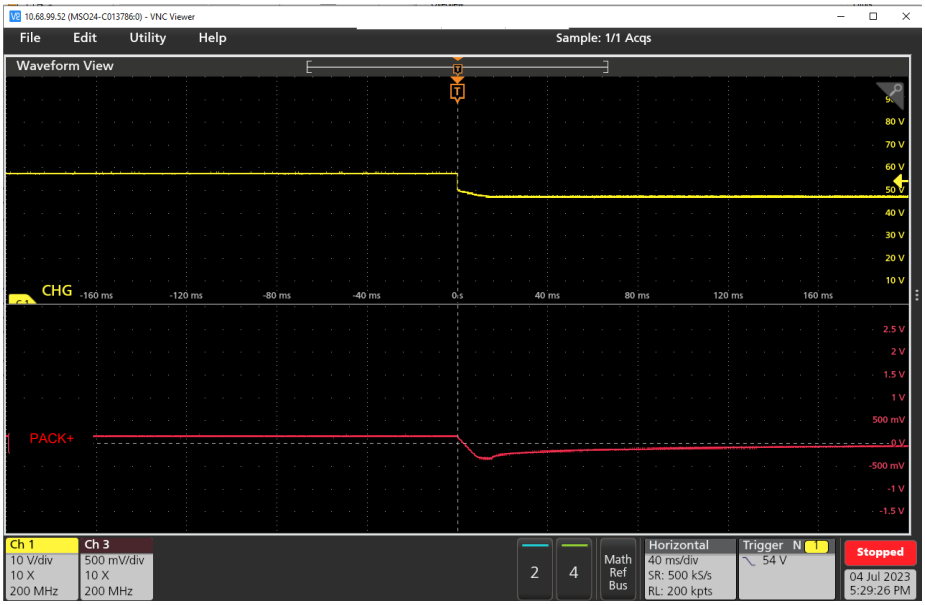

Figure 5 Parallel FET CHG OFF

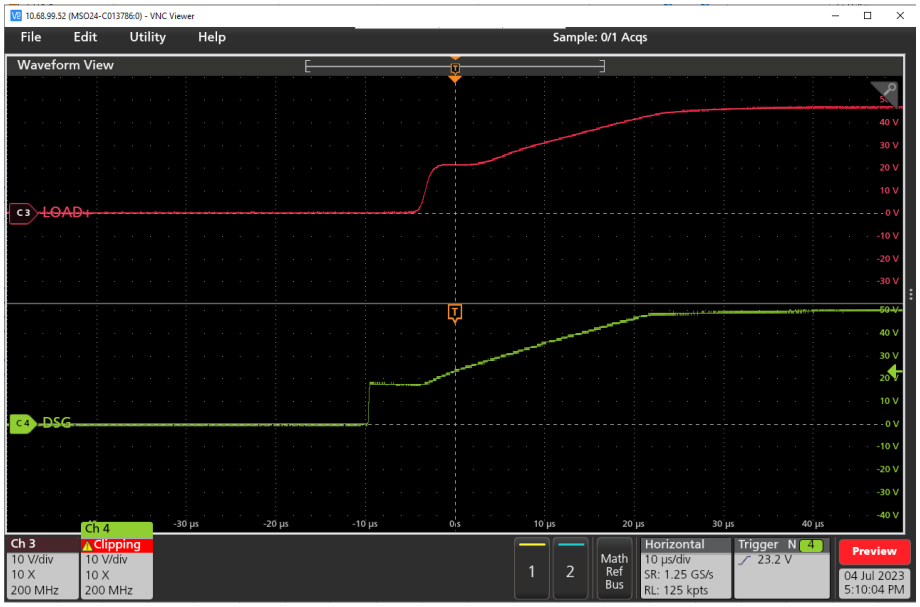

Figure 6 Parallel FET DSG ON

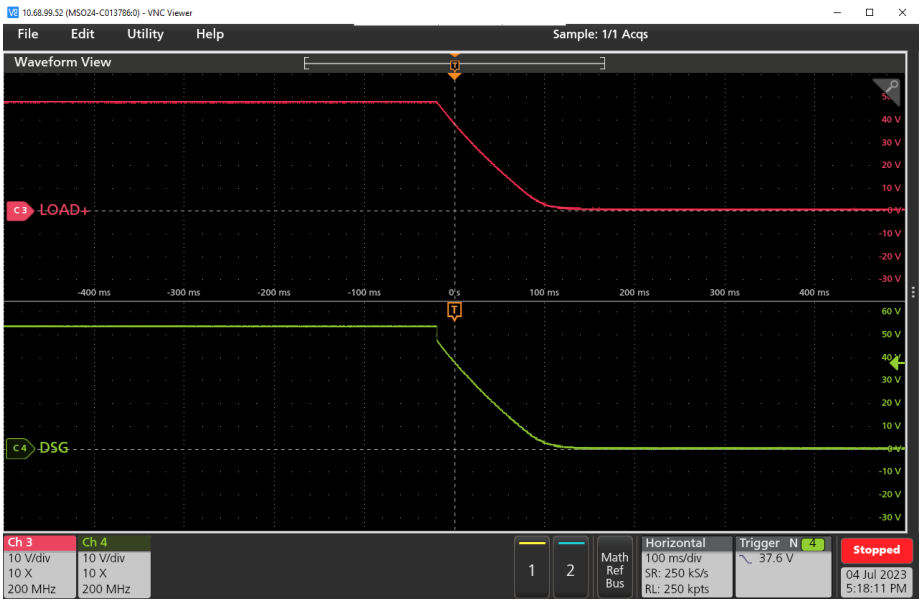

Figure 7 Parallel FET DSG OFF

1.5 LEGAL INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

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