Application Note PAC2xxxx External Cell Balancing

Power Application Controller® Battery Management

1 PAC2xxxx BMS Devices

The Qorvo® PAC2xxxx are a family of Intelligent Battery Monitoring System (BMS) that can monitor 10-series to 20-series Li-Ion, Li-Polymer and LiFePO4 battery packs. They integrate a FLASH-programmable MCU, Power Management, Current/Voltage/Temperature Sense and drive circuits for charge/discharge FETs and protection fuses. It can communicate using UART, SPI I2C/SMBus serial interfaces. The devices provide access to multiple analog and digital peripherals required to manage today's high cell count battery packs. The device support up to 50mA internal cell balancing with the following application diagram.

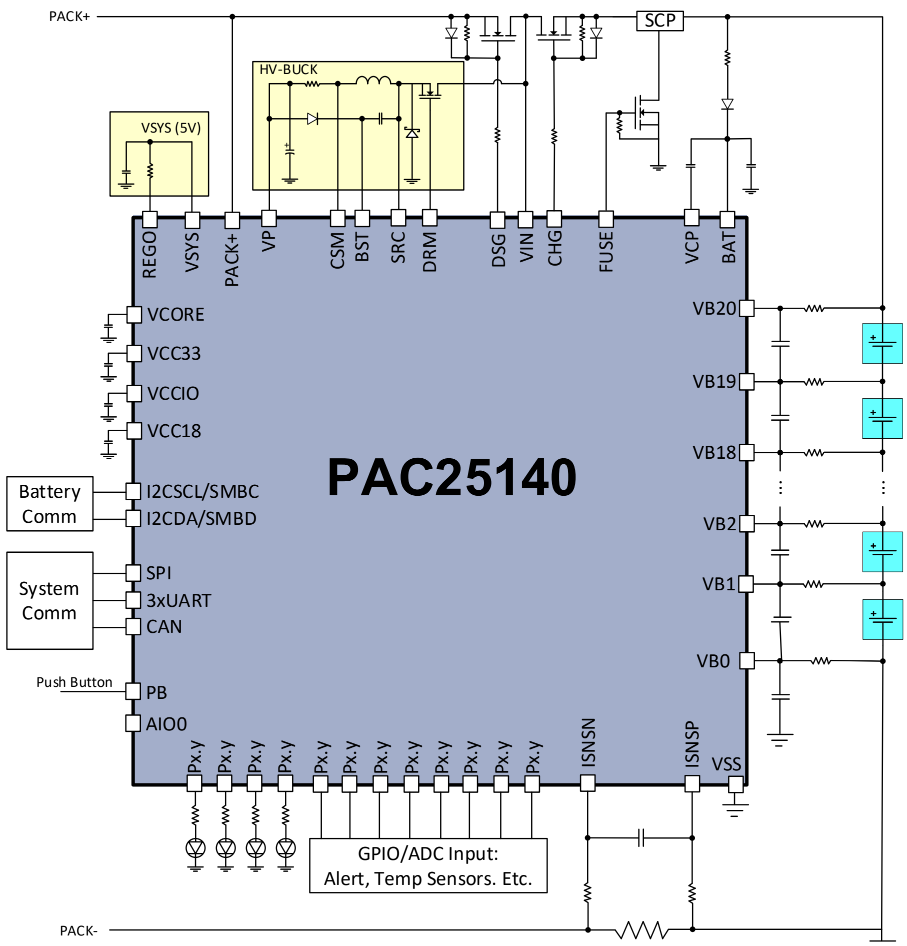

Figure 1-1 Example Standard application diagram using internal Cell Balancing

2 Why use External FET Cell Balancing?

In many large battery cell count battery applications (>10 cells in series), cells should be balanced to achieve the maximum runtime otherwise the weakest cell will limit the battery pack operation. As cell count goes up the probability increases that the cells do not match, and the imbalance will more likely occur.
The PAC2xxxx device family supports passive cell balancing, and internally PAC2xxxx cell balancing is limited in current to less than 50mA due to internal heating. When the internal cell balancing cannot support the desired current then an external FET can be used to increase the current to more than 200mA. The PAC2xxxx firmware is used to control cell balancing whether internal or external method is used.

2.1 External FET Cell Balancing Application

It has become common place to use External Cell Balancing to support faster cell balancing times using external balancing devices of N-channel FETs, P-channel FETs, and BJTs

External Cell Balancing allow much higher current than the internal FET which is limited to 50mA. For large capacity battery packs, this will reduce the delay to achieve balance among all the cells. Additionally, this could allow balancing in all conditions to have an impact on runtime. Such as in a discharge operation when the discharge current is higher by more than 10x the balancing current.

To ensure accurate cell voltage measurement, stop cell balancing before any cell voltage measurements and balance when cell voltages allow the measurement circuitry to work properly.

Design the cell balancing algorithm to prevent damage to the device during any cell balancing combinations.

- Do not balance adjacent cells. This turn on current will be bypassed by the second path, and possibly violating the allowed voltage limitation on the device.
- Beware of balancing nonadjacent cells, opposite sides of one cell (N & N+2), as this could lead to exceeding the allowed voltage on the middle cell input (N+1)

2.2 How External FET Cell Balancing Works

In typical External FET Cell Balancing, it starts with selecting the external device. PNP, NPN, NFET or PFET can be used. Next select the filter resistance to be large enough to ensure the device will turn on when the internal cell balancing circuit is activated, but not so large that it creates additional error in the cell measurement. Internally is a 25Ω FET, so a higher filter resistor will be required and act as a resistor divider on the two cell inputs (VB and VB(n-1)). The filter resistance will provide the turn on voltage across the external device and therefore allow current to bypass the cell. For this application, the lower cell voltage operation, cost and robustness of the bipolar devices makes those devices preferred.

Balance when cell voltages are high enough to allow the application circuit to work properly
Design the algorithm to prevent damage to the cells during any allowed combination
Do not balance adjacent cells. This is due to the turn on current will be canceled by the second path.
Beware of balancing nonadjacent cells, opposite sides of one cell (N & N+2), as this could lead to exceeding the allowed voltage on the middle cell input (N+1)

3 EXTERNAL PNP CELL BALANCING

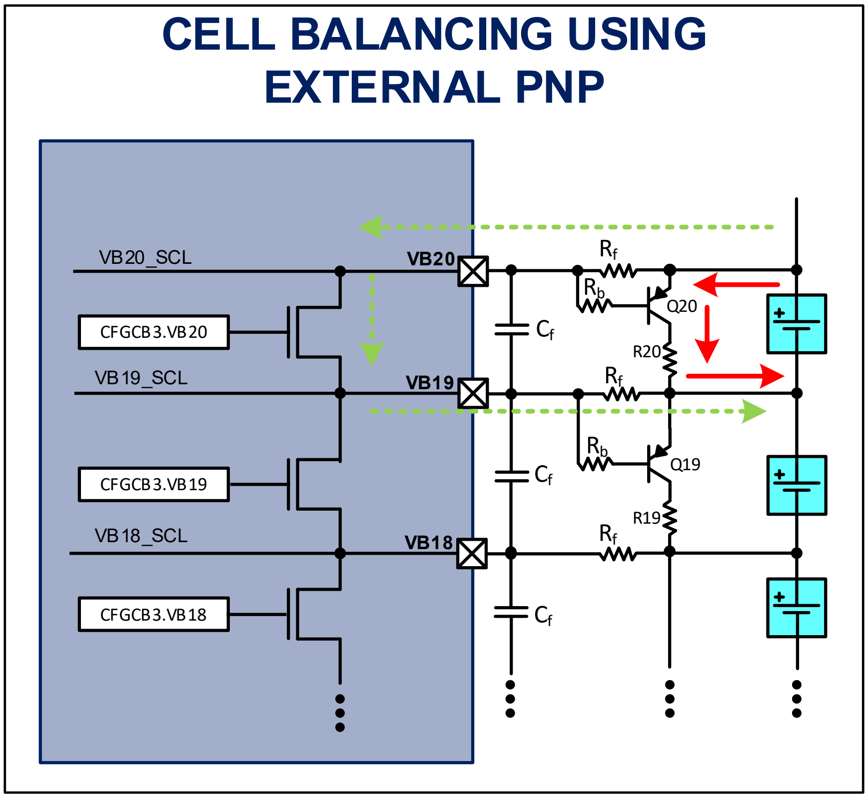

Figure 2-1 Example with PNP Circuitry

To enable the external bipolar PNP, the internal cell balancing FET is turned on and a voltage across the filter resistor (Rf) higher than the turn on value of the external PNP will be produced.

The filter resistor (Rf) should be chosen such that it is not greater than 500Ω but large enough to generate a voltage above the PNP Vbe turn on value. Voltage accuracy is affected by the external cell filter resistance and capacitance; they should be selected within recommended values. If different component values result in a large time constant, the cell input voltage will not settle during the measurement window and an error in the voltage will be measured.

The green lines in figure 2-1 are the internal cell balancing current, limited by 2 x Rf and Internal cell balancing FET (Rint) The red lines are the high current path set by Q20 on resistance and R20 resistance.
Example: Vcell = 3V, Rf = 200Ω, R20 = 20Ω, Rint = 25Ω, Q20 Hfe(100mA) = 30, Rb = 220Ω

Results: Internal CB current = 7mA; External CB current = 106mA Total CB current = 113mA
R20 dissipation is 228mW, Q20 VCE is 0.864V

The green lines are the internal cell balancing current, limited by Rf and Internal cell balancing FET. The red lines are the high current path set by Q20 VCE and R20 resistance. The base resistor Rb will prevent the bipolar saturation and additionally used to prevent ESD or other transients from damaging the PNP or firing the VBx pin ESD.

Component selection

Qxx should have a current rating higher than desired balancing current and break down voltage equal or greater than the battery stack voltage.

Rxx (balancing current limit resistor) should be selected to limit the cell balancing current below Qxx rating and power rating higher than balancing current times the cell maximum voltage.

Rb should be selected to limit the base current during transients, so the PNP does not enter saturation or operate beyond base drive current limitations.

Rf should be large enough to turn on the bipolar, and limit internal current. But not so large to introduce error into the measurement.

3.1 External PNP Cell Balancing Operation Waveforms

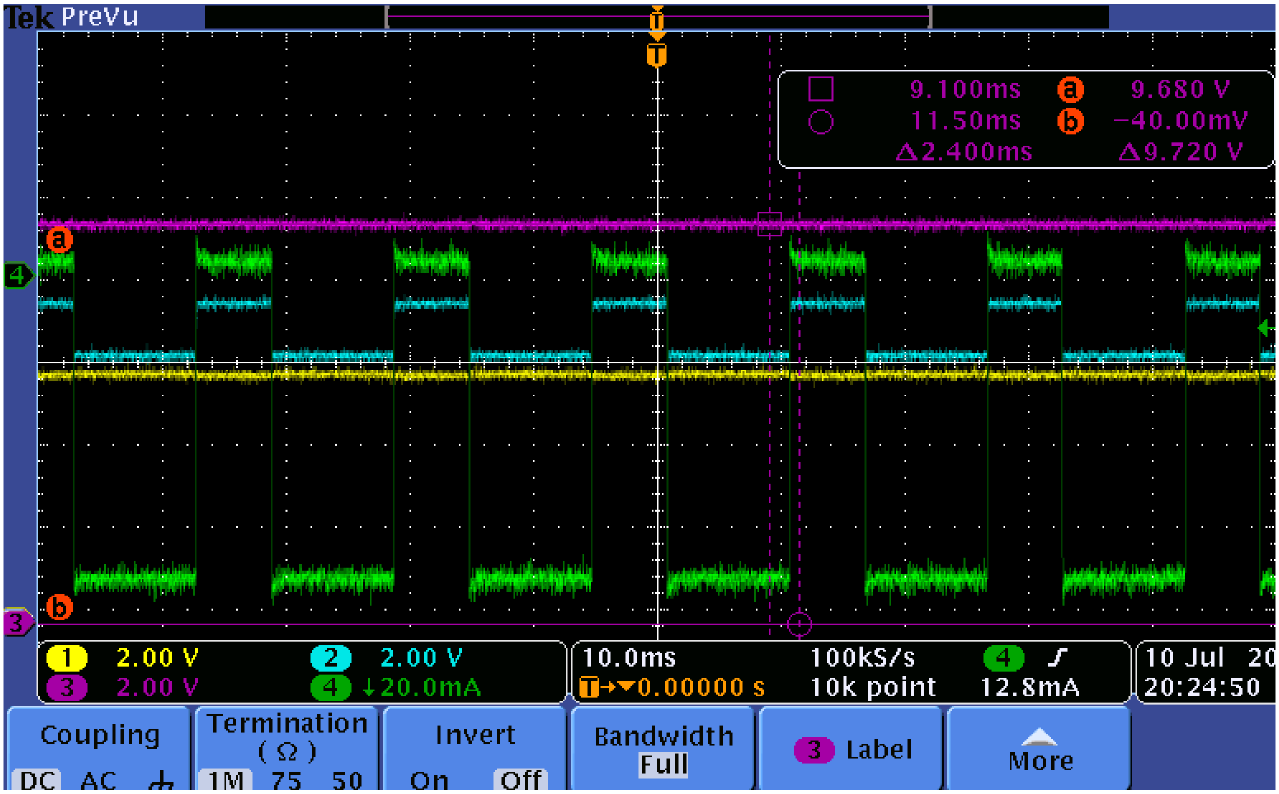

Figure 2-2 PNP Cell Balancing Circuitry Duty Cycling

Green line is the cell balancing current, Blue is the Base voltage.

The current is set by the voltage of the cell and the resistance in series with the PNP. For figure 2-2, the voltage of the cell was reduced.

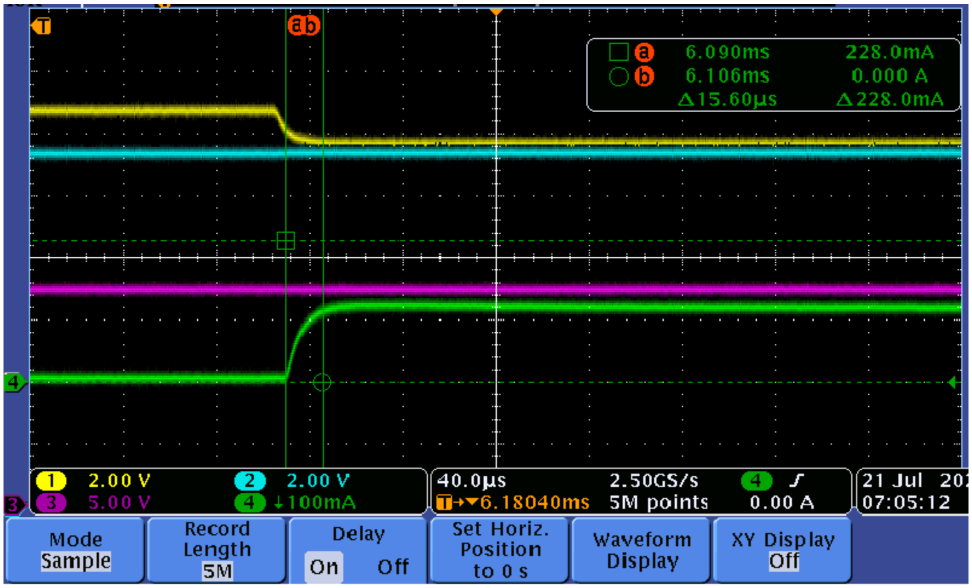

Figure 2-3 PNP Cell Balancing Circuitry Rise Time

Green line is the cell balancing current, Yellow is the Base voltage

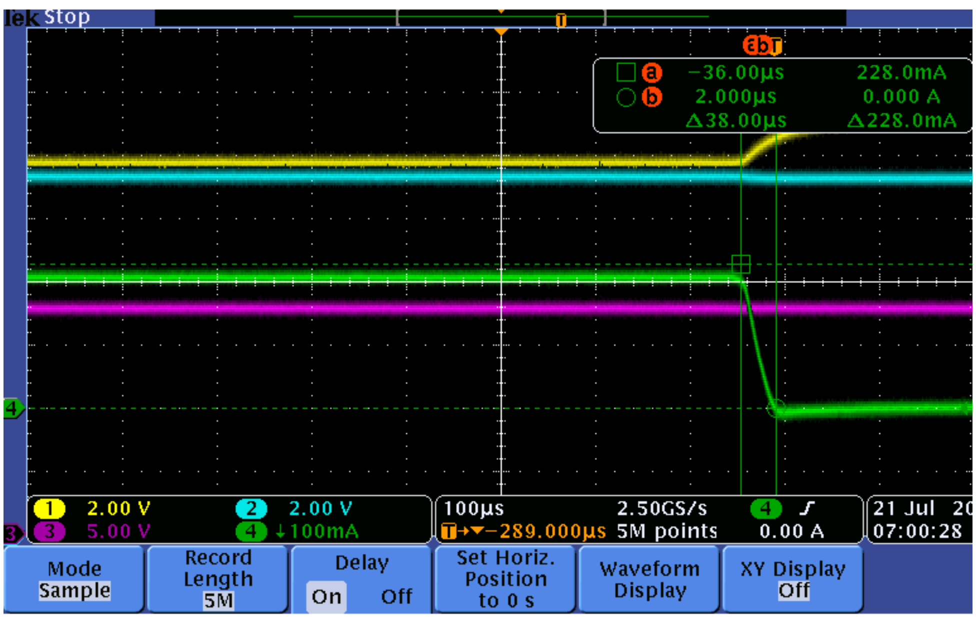

Figure 2-4 PNP Circuitry Cell Balancing Fall Time

Green line is the cell balancing current, Yellow is the Base voltage

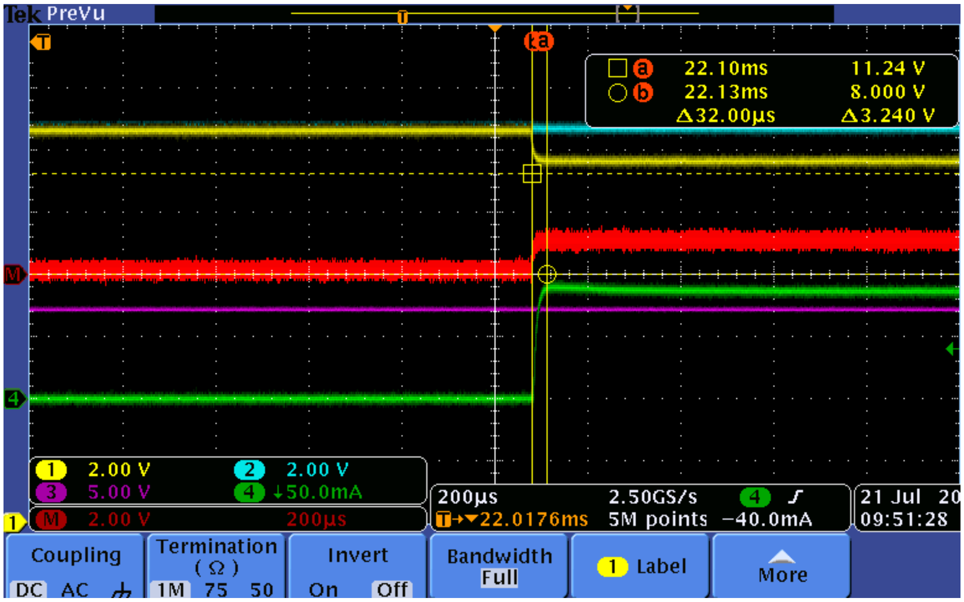

Figure 2-5 PNP Circuitry Turn On

Green line is the cell balancing current, Yellow is the Base voltage, Red is Vbe

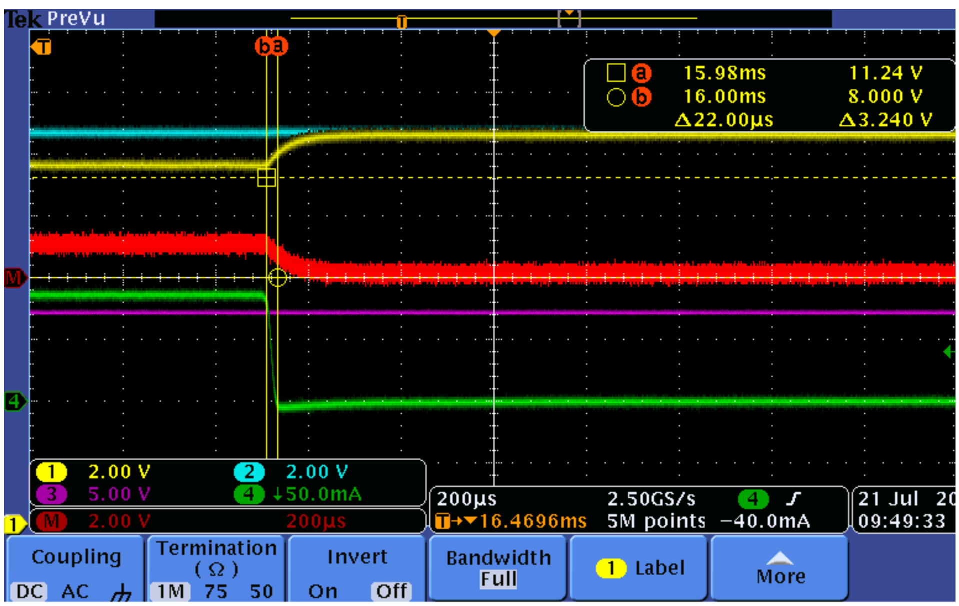

Figure 2-6 PNP Circuitry Turn Off

Green line is the cell balancing current, Yellow is the Base voltage, Red is Vbe

4 External NPN Cell Balancing

Alternatively, an NPN device can be configured to support external cell balancing.

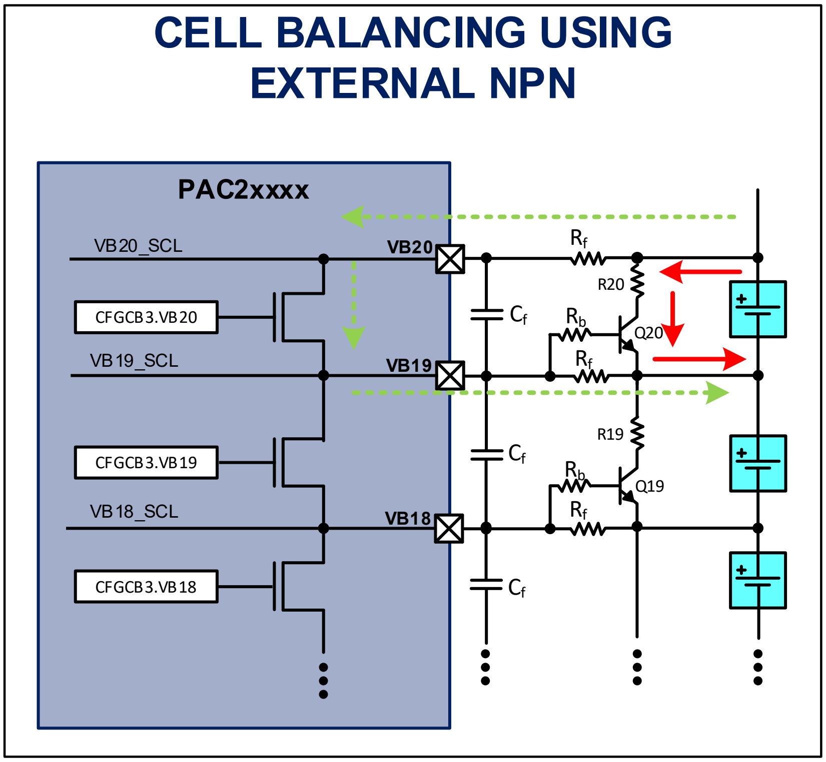

Figure 4-1 Example with NPN Circuitry

4.1 External NPN Cell Balancing

To enable the external bipolar NPN, the internal cell balancing FET is turned on and a voltage across the filter resistor (Rf) higher than the turn on value of the external NPN will be produced. The filter resistor (Rf) should be chosen such that it is not greater than 500Ω but large enough to generate a voltage above the NPN Vbe turn on value.

The green lines are the internal cell balancing current, limited by 2 x Rf and Internal cell balancing FET (Rint) The red lines are the high current path set by Q20 on resistance and R20 resistance.

Example: Vcell = 3V, Rf = 200Ω, R20 = 20Ω, Rint = 25Ω, Q20 Hfe(100mA) = 30, Rb = 220Ω

Results: Internal CB current = 7mA; External CB current = 106mA Total CB current = 113mA
R20 dissipation is 228mW, Q20 VCE is 0.864V

The green lines are the internal cell balancing current, limited by Rf and Internal cell balancing FET. The red lines are the high current path set by Q20 VCE and R20 resistance. The base resistor Rb will prevent the bipolar saturation and additionally used to prevent ESD or other transients from damaging the NPN or firing the VBx pin ESD.

Component selection

Qxx should have a current rating higher than desired balancing current and break down voltage equal or greater than the battery stack voltage.

Rxx (balancing current limit resistor) should be selected to limit the cell balancing current below Qxx rating and power rating higher than balancing current times the cell maximum voltage.

Rb should be selected to limit the base current during transients, so the NPN does not enter saturation or operate beyond base drive current limitations.

Rf should be large enough to turn on the bipolar, and limit internal current. But not so large to introduce error into the measurement.

5 External NFET Cell Balancing

Alternatively, an NFET device can be configured to support external cell balancing.

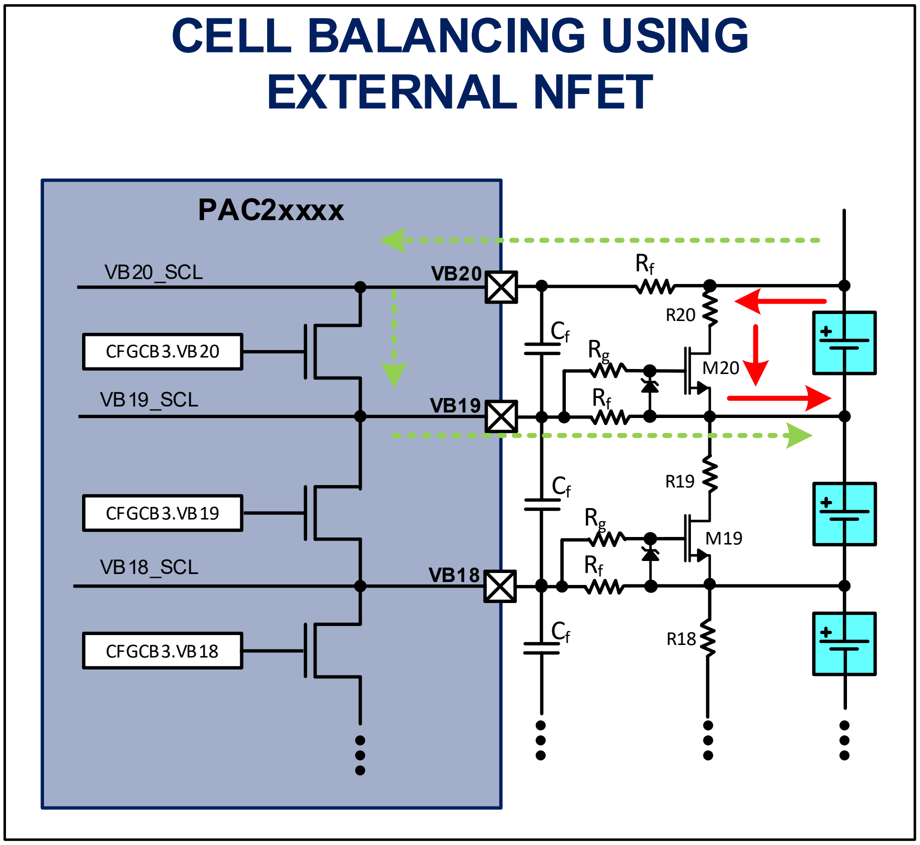

Figure 5-1 Example with NFET Circuitry

5.1 External NFET Cell Balancing

To enable the external NFET, the internal cell balancing FET is turned on and a voltage across the filter resistor (Rf) higher than the turn on threshold of the external NFET will be produced. The filter resistor (Rf) should be chosen such that it is not greater than 500Ω but large enough to generate a voltage above the NFET turn on threshold.

The green lines are the internal cell balancing current, limited by 2 x Rf and Internal cell balancing FET (Rint) The red lines are the high current path set by M20 on resistance and R20 resistance.

Example: Vcell = 3V, Rf = 200Ω, R20 = 20Ω, Rint = 25Ω, M20 = 2Ω, Rg = 500Ω

Results: Internal CB current = 7mA; External CB current = 136mA Total CB current = 143mA
R20 dissipation is 370mW, M20 VGS is 1.41V

If transient protection is necessary, then add a gate resistor (Rg) and protection zener for the VGS. For example, in the event of a short across the pack in a 20-cell battery, Cell 20 could have 80V across Rf during the event and the opposite due to flyback at the release of the pack short circuit. The gate should be connected through a resistor to limit the current when the diode conducts during transients. During normal operation, the Zener does not conduct, so the resistor value is not critical to normal operation. For an 80V pack a 1kΩ should be acceptable and limit the current to 80mA.
Care must be taken to select an external NFET with a low RDSON defined at low VGS. For example, if the cell balancing minimum voltage is 3.0V, from the example above. The external NFET should have an RDSON of 2Ω value at or below VGS = 1.41 V.

Component selection

Mxx should have a current rating higher than desired balancing current and break down voltage equal or greater than the battery stack voltage.

Rxx (balancing current limit resistor) should be selected to limit the cell balancing current below Mxx rating and power rating higher than balancing current times the cell maximum voltage.

Rg should be selected to limit the clamping current going through the gate protection diode during transients.

Rf should be large enough to turn on the NFET, and limit current going into the device. But not so large to introduce error into the measurement.

6 LEGAL INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

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