

SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD
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LAYER STACK LEGEND

	Material	Layer	Thickness	Dielectric Material	Type	Comment
		Top Overlay			Legend	HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
	Surface Material	Top Solder	0.0004	Solder Resist	Solder Mask	LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN.
	Copper	Top Layer	0.0018		Signal	FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH
	Core		0.0080	Rogers 4003	Dielectric	
	Copper	Bottom Layer	0.0018		Signal	FINISH THICKNESS=0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH
Finished board thickness: 0.0120						

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
FABRICATE IN ACCORDANCE WITH IPC-6018, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS
COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
METAL 1 (TOP) AND METAL 2 (BOTTOM):
ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
ELECTROLESS NICKEL per IPC-4552, 118 - 236µin. (3 - 6µm)
IMMERSION GOLD per IPC-4552, 3 - 10 µin (0.08 - 0.25µm)
4. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) +/- 10%
5. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM)
EXCEPT AROUND CONNECTOR AREA WHERE EDGE PLATING IS NECESSARY.
THE PRODUCT PERFORMANCE IS SIGNIFICANTLY COMPROMISED WITH LARGE PULL BACKS. WE WILL ACCEPT
BURRS.
6. CONTROLLED IMPEDANCE: CPW LAYER 1 TRACES ARE 0.014 +/- 0.001, REF LAYER 2. TARGET IMPEDANCE IS 50 OHMS
+/-5%. TARGET FREQUENCY 6GHz. CORE DIELECTRIC CAN BE ADJUSTED TO OBTAIN FINISHED THICKNESS.
7. PCB OUTLINE: ±0.003in.TOLERANCE AND IS CRITICAL TO RF PERFORMANCE
8. SINGULATION: EXTERNAL OUTLINE IS TO BE COMPLETED
VIA OPTICAL (LENZ) ROUTING OR LASER TO ACHEIVE PCB OUTLINE TOLERANCE. LASER
ROUTING IS AUTHORIZED ONLY IF IT YIELDS A CONTAMINANT FREE SURFACE ADJACENT
TO THE LASER-SAWN EDGE.
9. SLIGHT BURRS ARE ACCEPTABLE.
10. VIA PLATING/FILLING:
ALL 0.006in, 0.008in AND 0.015in VIAS ARE TO BE EPOXY FILLED OVER PLATED AND PLANERIZED.
ALL OTHER PLATED THRU HOLES ARE TO BE PLATED TO 0.0007 ± 0.0004in. MIN. THICKNESS.
11. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
12. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
13. NO ELECTRICAL TEST NEEDED.
14. NO VENDOR MARKING ALLOWED EXCEPT DATE CODE FOR TRACEABILITY.
15. BOARDS TO BE SINGLULATED PER MECHANICAL 3 (OUTLINE) AND DELIVERED AS SINGLES

16. BOARD TO BE EDGE PLATED AS SHOWN.

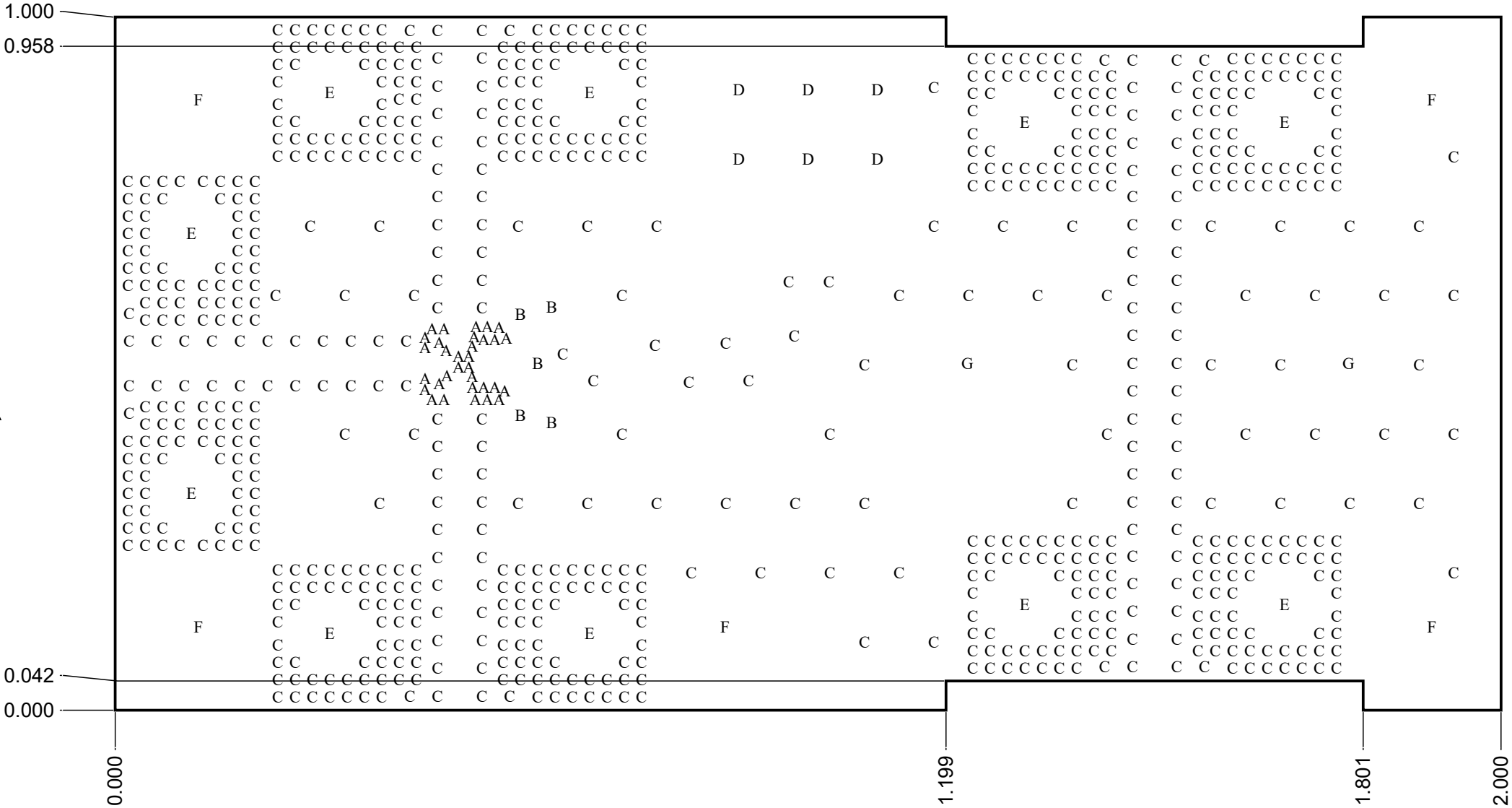
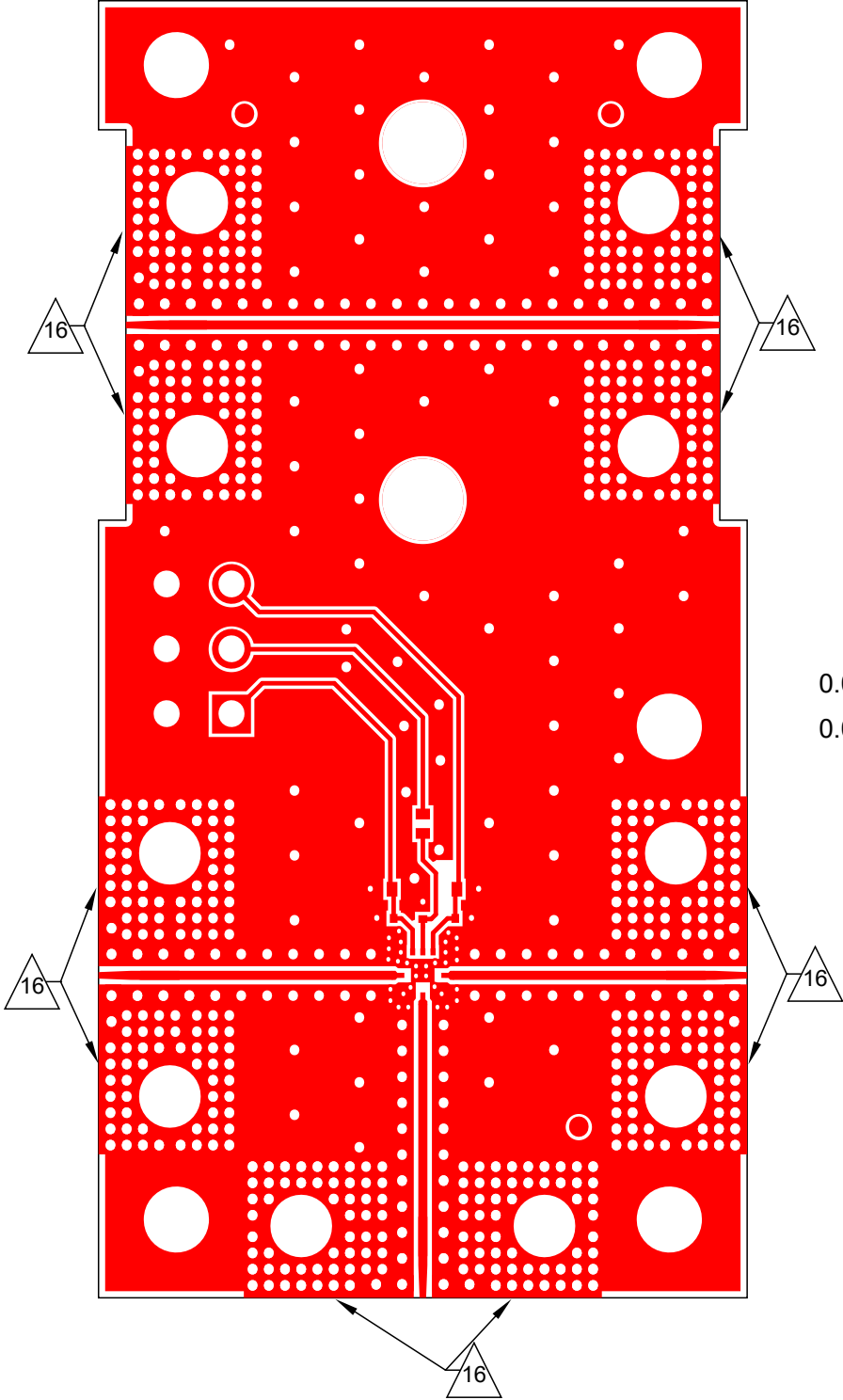
* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 303636						
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE						
	DESIGNER J. MORRIS		DATE	TITLE: QPC0542 EVALUATION PCB DESIGN PACKAGE			
	ENGR. R. KINCAID		02/15/2023				
	INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009						
	PDE CONTROLLED			SIZE B	DOCUMENT NUMBER: QPC0542-4000	PROTOTYPE INSTANCE: [11]	REV. 1
	THIRD ANGLE PROJECTION DO NOT SCALE DRAWING	CAGE CODE	1CVM1				
		SHEET 1 OF 7		CAD: ALTIUM DESIGNER		SCALE: 2:1	

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WARNING - THIS DOCUMENT CONTAINS TECHNICAL DATA WHOSE EXPORT IS UNDER CONTROL OF THE UNITED STATES DEPARTMENT OF COMMERCE UNDER THE EXPORT ADMINISTRATION REGULATIONS (15 CFR 730-774). DIVERSION CONTRARY TO U.S. LAW IS PROHIBITED. INFORMATION AND GUIDANCE ON EXPORT CONTROL REQUIREMENTS CAN BE FOUND AT www.BIS.doc.GOV

Top Layer (Scale 3.5901:1)



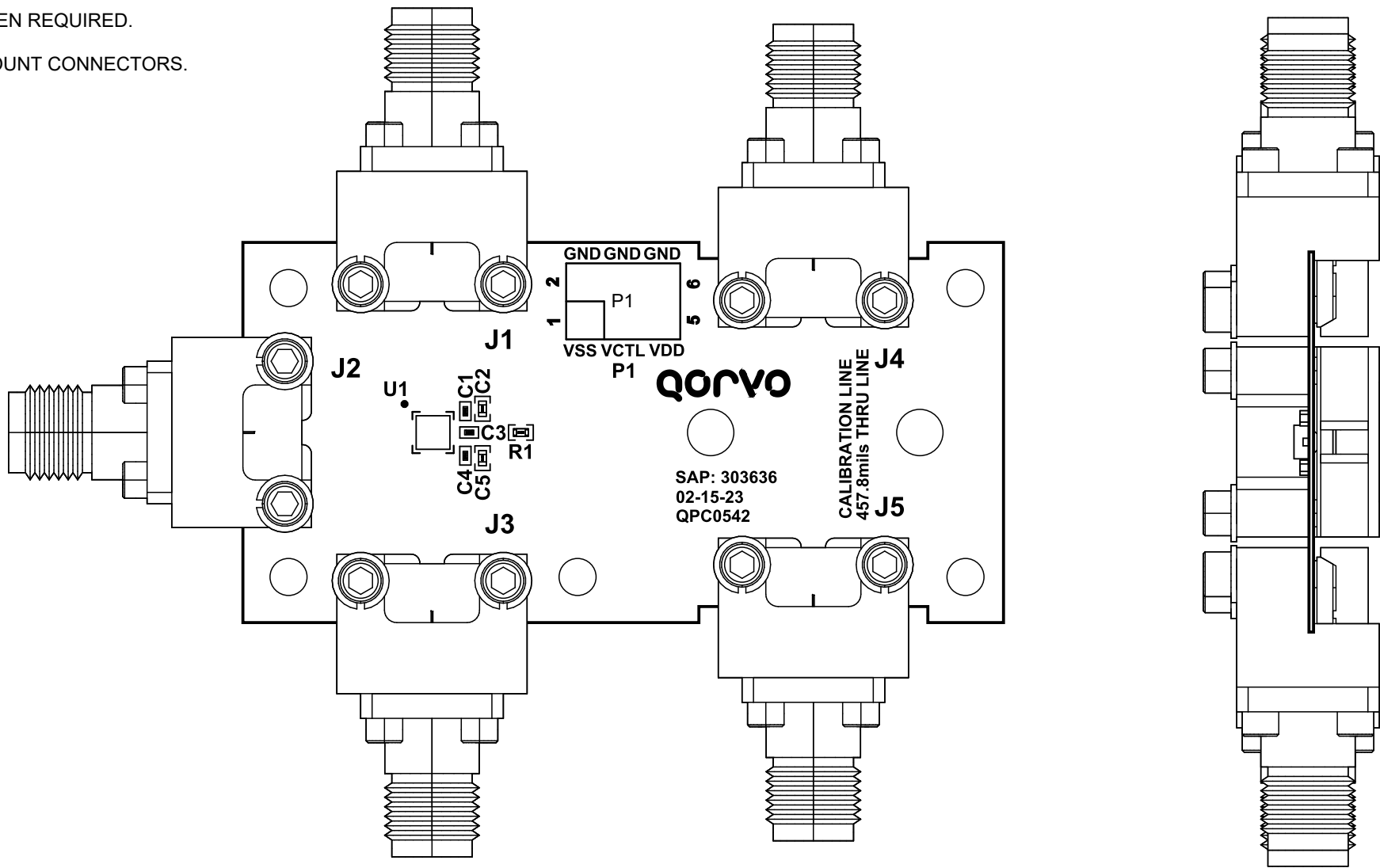
Drill Table

Symbol	Count	Hole Size	Plated	Drill Layer Pair
A	32	0.006	Plated	Top Layer - Bottom Layer
B	5	0.008	Plated	Top Layer - Bottom Layer
C	730	0.015	Plated	Top Layer - Bottom Layer
D	6	0.040	Plated	Top Layer - Bottom Layer
E	10	0.095	Plated	Top Layer - Bottom Layer
F	5	0.100	Plated	Top Layer - Bottom Layer
G	2	0.125	Non-Plated	Top Layer - Bottom Layer
	790 Total			

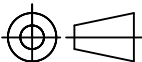
ASSEMBLY NOTES:

- 17. WORKMANSHIP & SOLDER PER IPC-A-610C, CLASS 2.
- 18. MANUFACTURERS' PART NUMBERS ARE SUBJECT TO CHANGE BY THE MANUFACTURERS FOLLOWING THE ISSUE OF THIS DOCUMENT, AND ARE THEREBY INCLUDED FOR REFERENCE ONLY. CONTACT QORVO CORORATE ENGINEERING MATERIALS WITH QUESTIONS REGARDING SPECIFIC MANUFACTURERS' PART NUMBERS.
- 19. QORVO DEVICES (DUT) MAY REQUIRE BAKING PER IPC/JEDEC J-STD-020 FOR A MINIMUM OF 24 HOURS AT 125 +5/-0 DEGREES C. ASSEMBLY MUST TAKE PLACE WITHIN 12 HOURS OF BAKE COMPLETION.
- 20. LOW TEMP SOLDER SHALL BE USED FOR ALL SMDs AND PRE-TINNING WHEN REQUIRED.
- 21. LEAD FREE (HIGH TEMP) SOLDER SHALL BE USED FOR SMA AND EDGE MOUNT CONNECTORS.

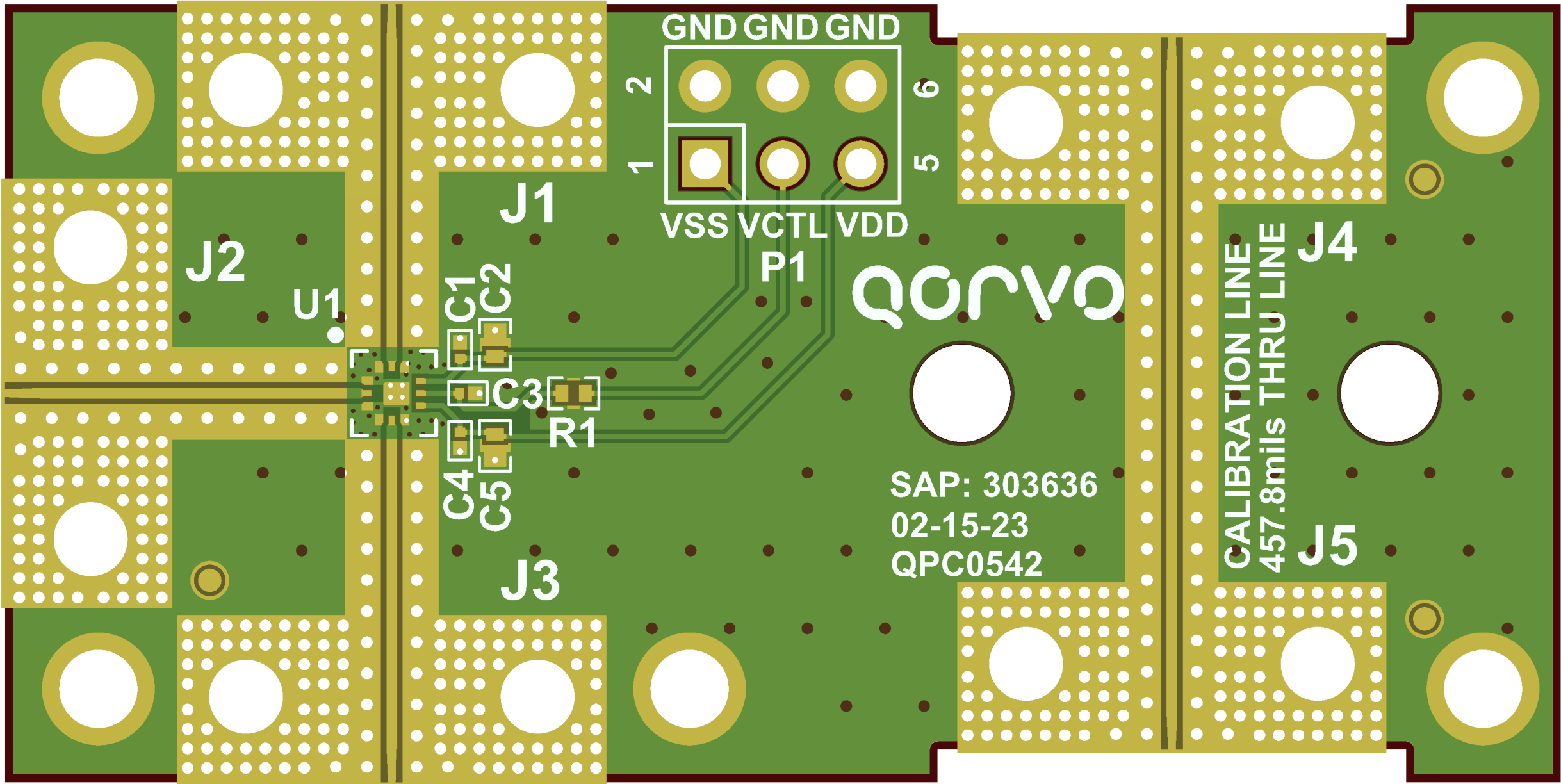
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		TOLERANCES . XX = ±.01 . XXX = ±.005 . XXXX = ±.0010 ANGLES = ± 0.5°		APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE		DATE		TITLE: QPC0542 EVALUATION PCB DESIGN PACKAGE			
				DESIGNER	J. MORRIS	02/15/2023					
				ENGR.	R. KINCAID						
		INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009		PDE CONTROLLED							
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		THIRD ANGLE PROJECTION DO NOT SCALE DRAWING						SHEET 3 OF 7		CAD: ALTIUM DESIGNER	

TOP VIEW (UNPOPULATED)



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					SHEET 4 OF 7			CAD: ALTIUM DESIGNER	
							SCALE: 2:1		

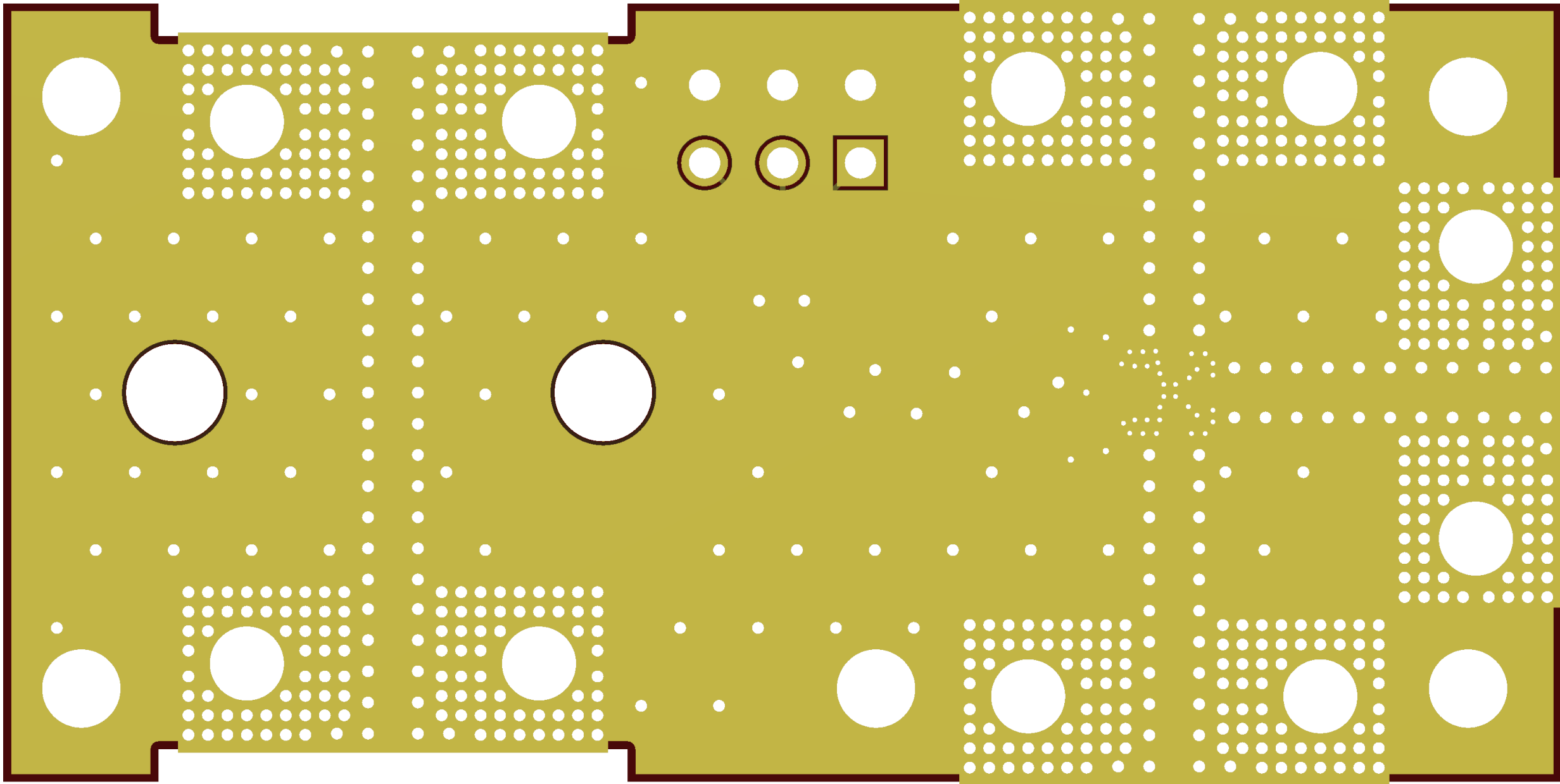
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3

2

1

BOTTOM VIEW (UNPOPULATED)



B

B

A

A

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Current Date & Time: 3/3/2023 8:21 AM

FOR-001456 REV B

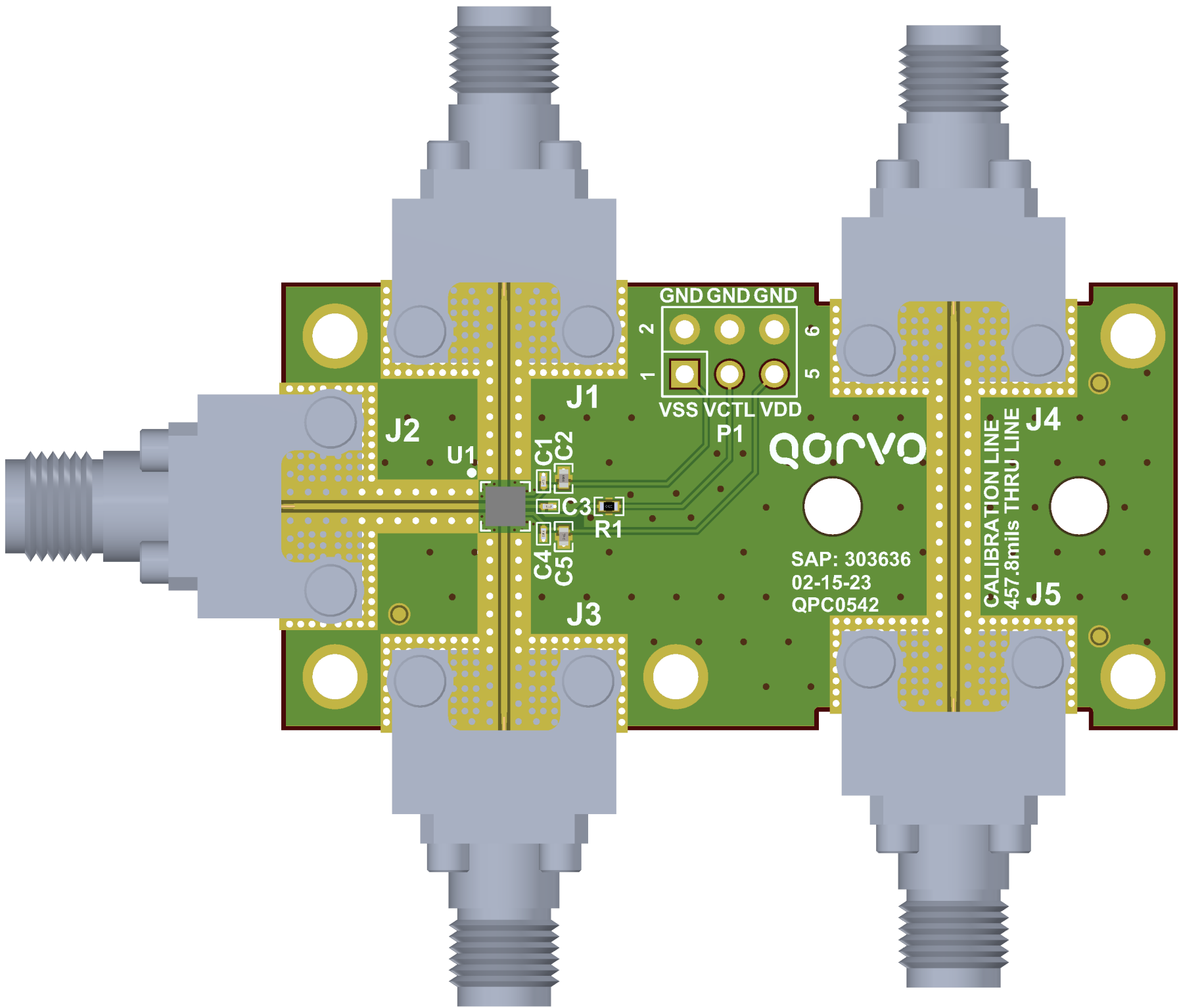
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3

2

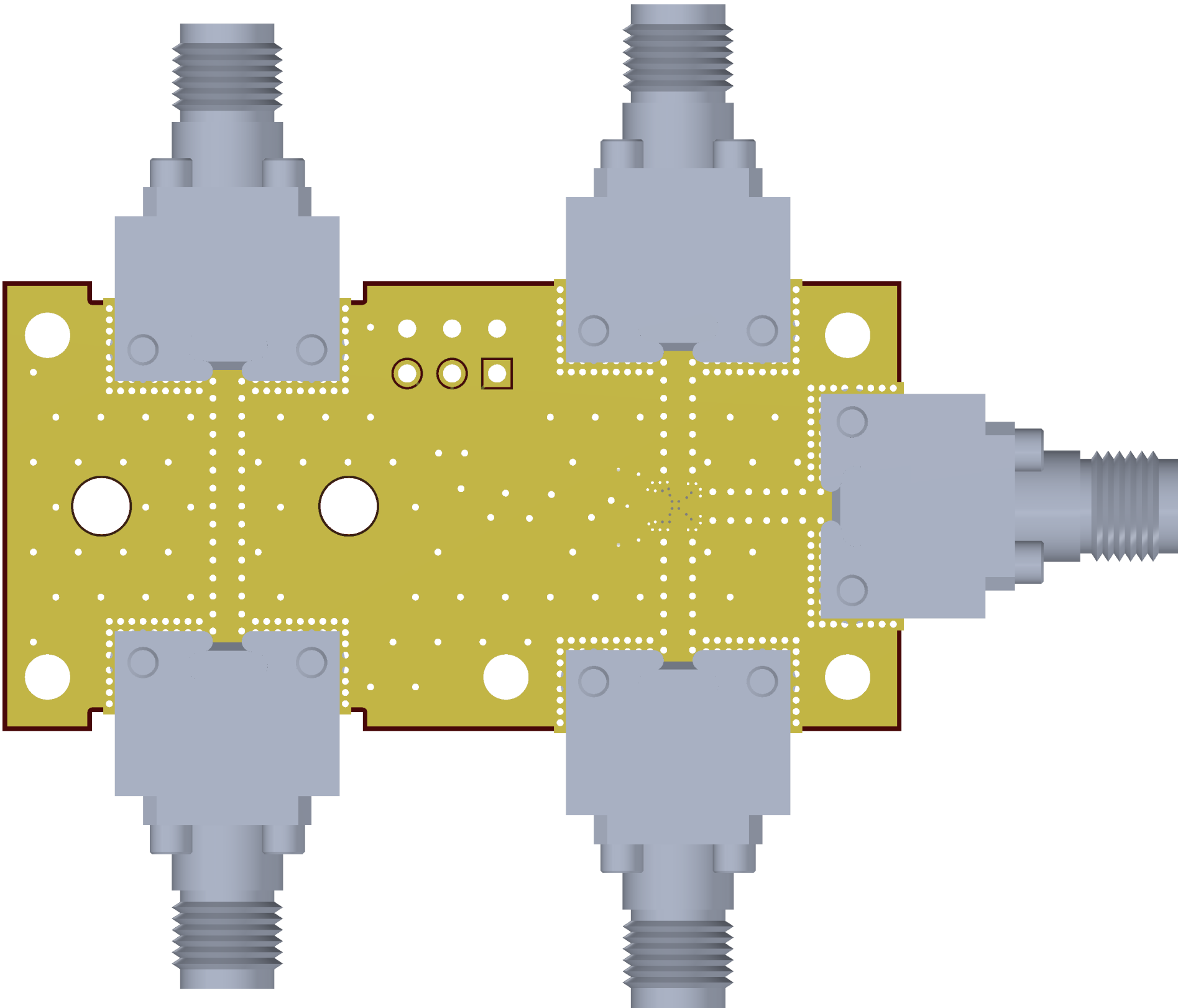
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TOP VIEW (POPULATED)



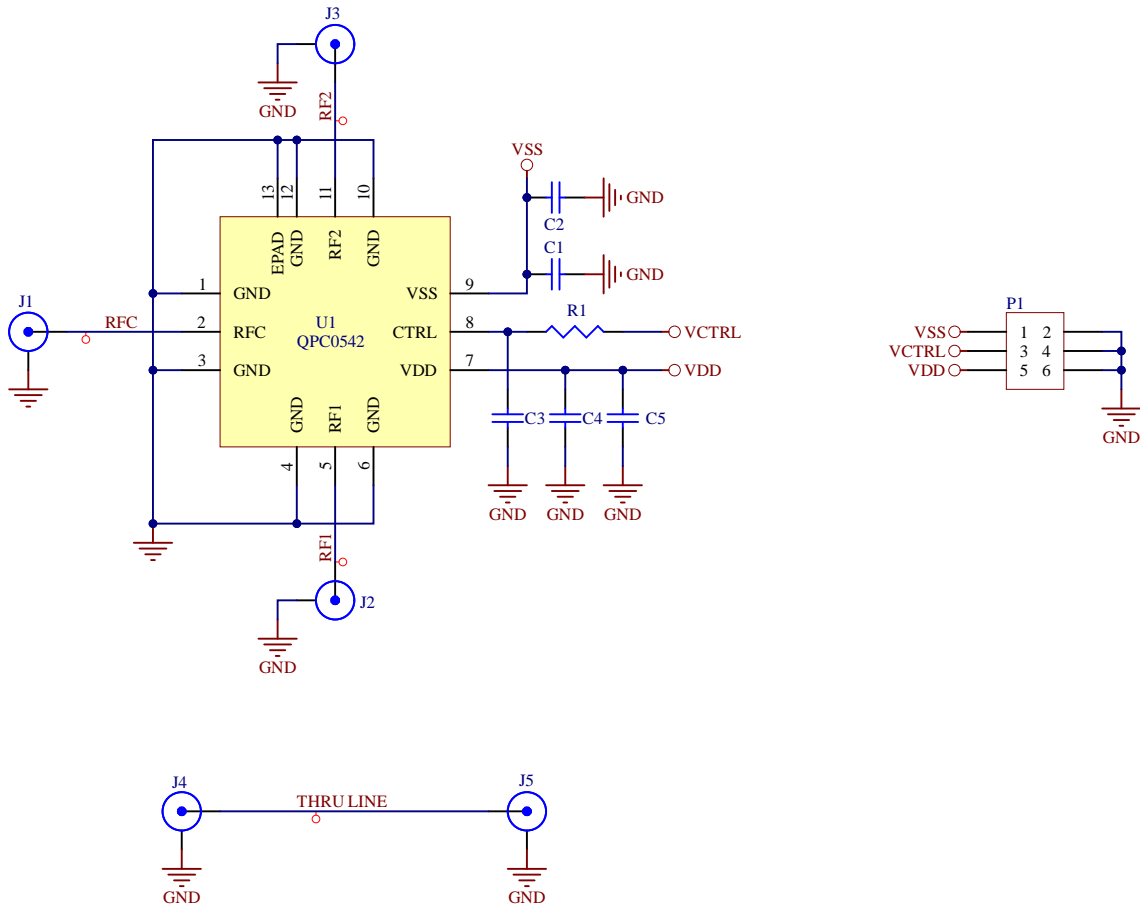
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BOTTOM VIEW (POPULATED)



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		SHEET 7 OF 7		CAD: ALTUM DESIGNER				SCALE:

REVISION HISTORY			
REV	DESCRIPTION	DATE	APPROVAL
1	PROTOTYPE RELEASE	02/15/2023	R. KINCAID



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