all around you

Advances in Technology for High Power CATV Gain Blocks and the Related Challenges in Linearity Testing During Design and Volume Production

The Engine for HFC: CATV Gain Blocks

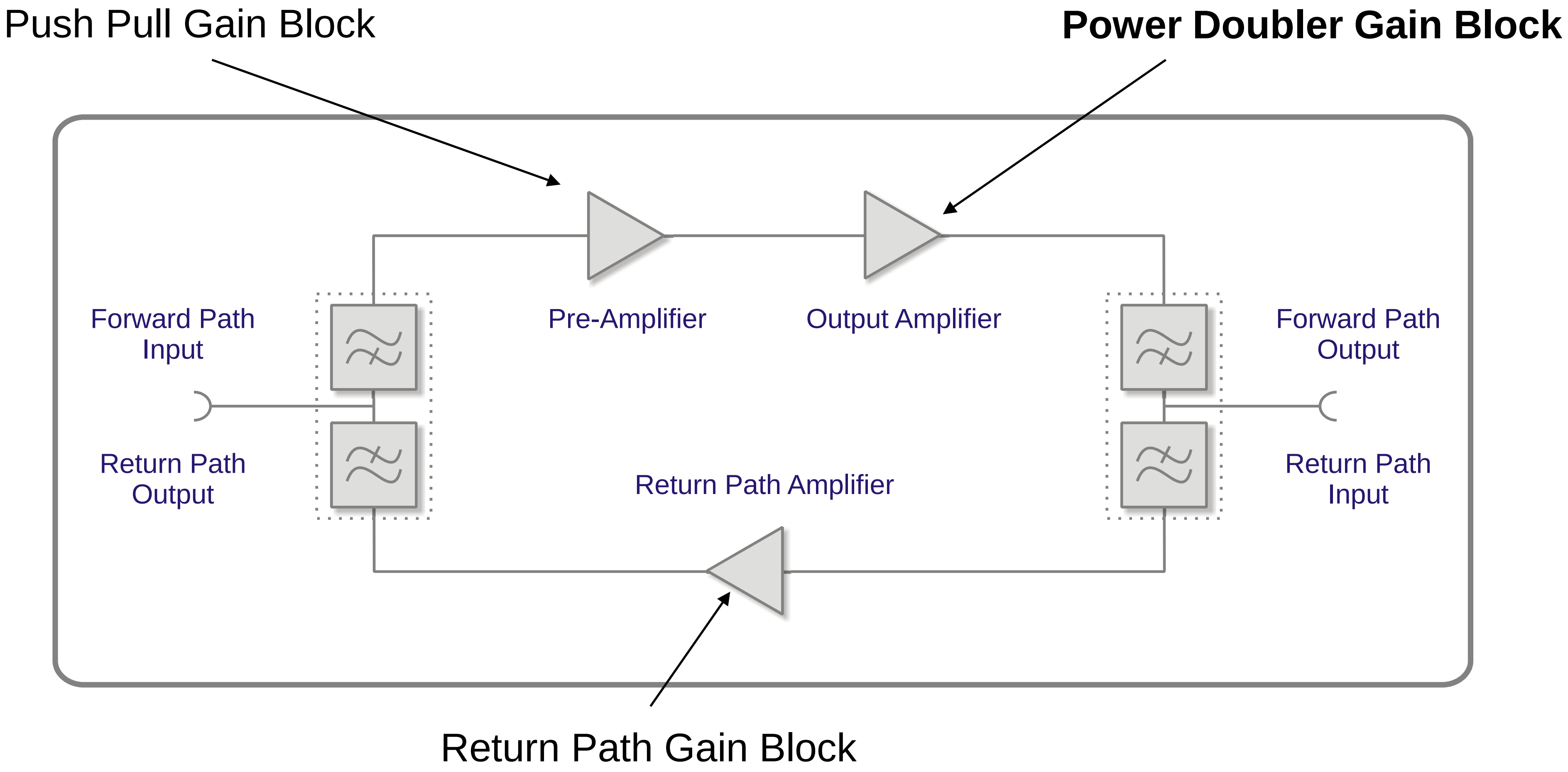
Agenda

- Gain Blocks for CATV networks
- Evolution of semiconductor technology
- Packaging and thermal design
- Linearity characterization and test development
- High volume assembly and test

GAIN BLOCK FOR CATV NETWORKS

CATV Amplifier

Simplified Block Diagram



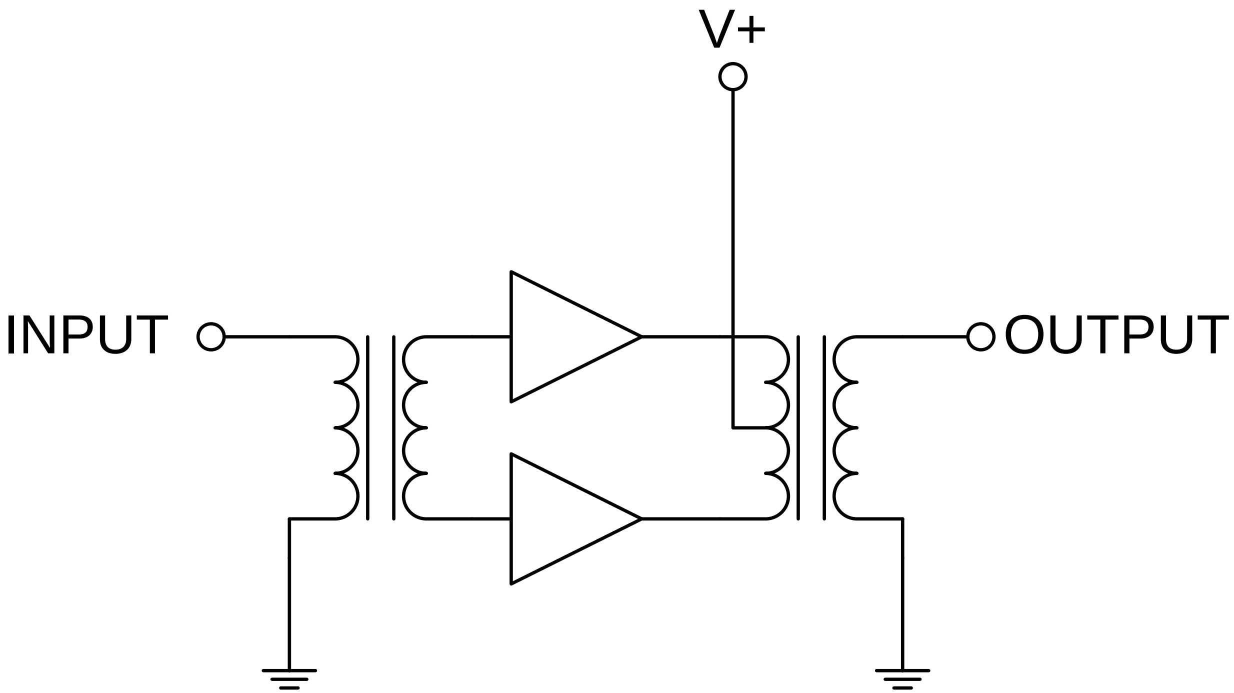
CATV Power Doubler Gain Blocks

Key Features

- Extremely robust
- Extremely reliable
- Extremely wide bandwidth (more than 5 octaves)
- Extremely linear
- Extremely high linear output power

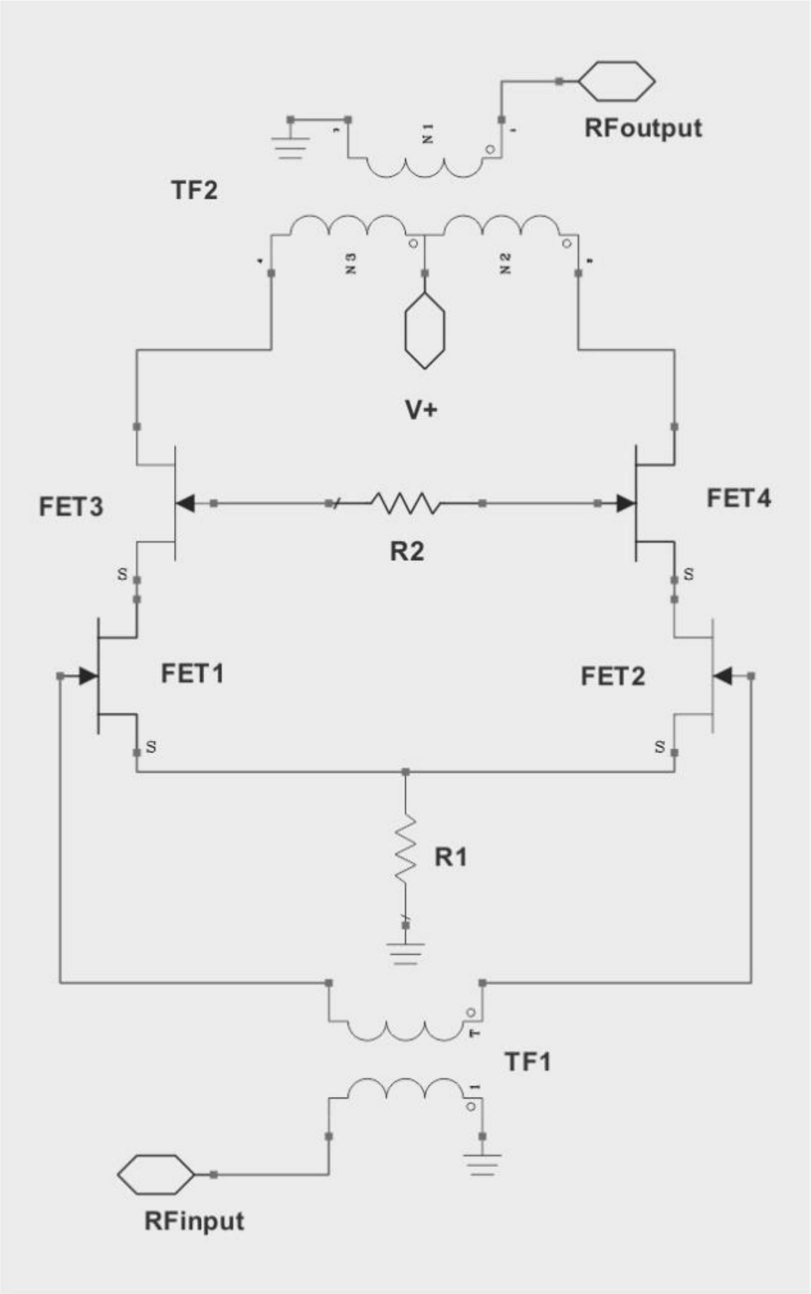
CATV Gain Block

Block Diagram



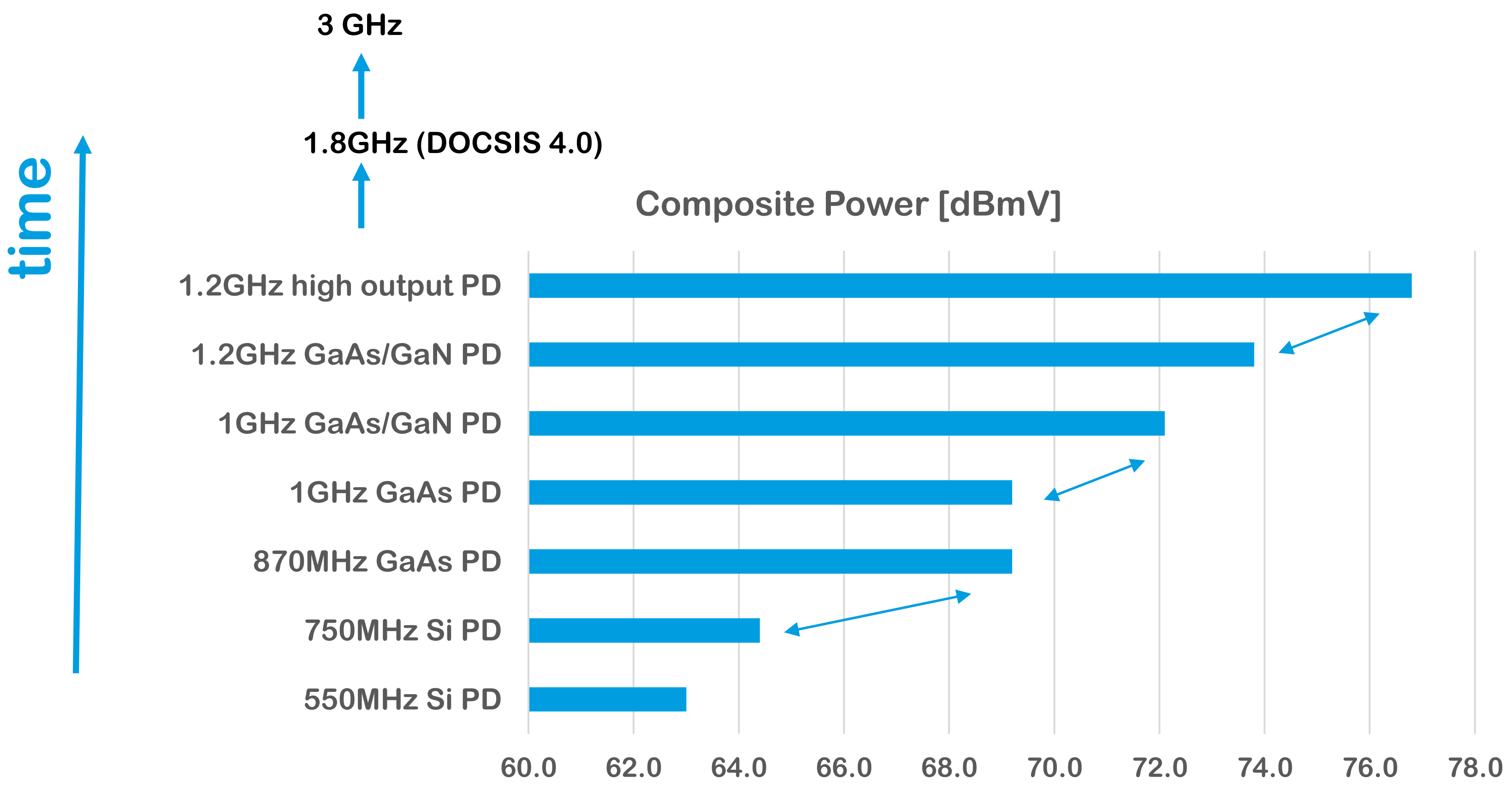
CATV Gain Block

Simplified Schematic



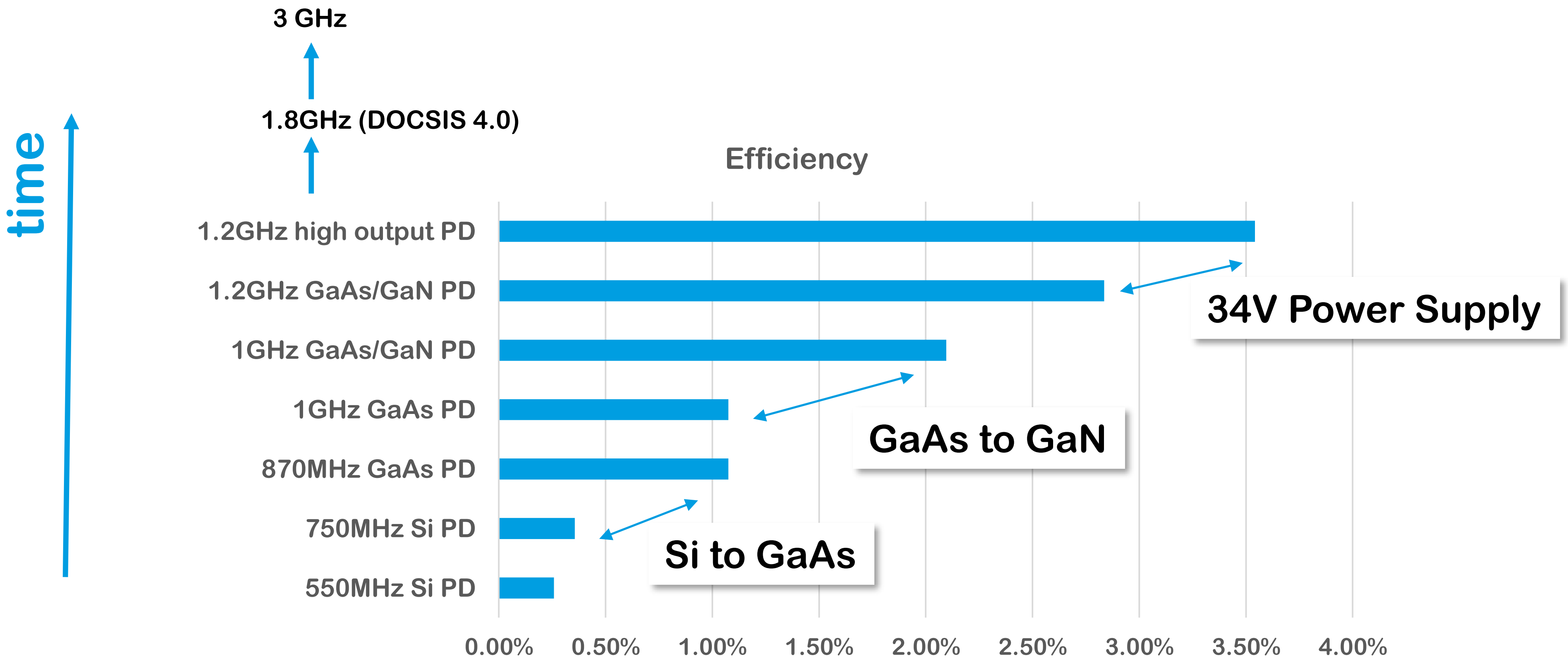
Advances in Linear Output Power

Efficiency and Composite Output Power



Advances in Linear Output Power

Efficiency and Composite Output Power



SEMICONDUCTOR EVOLUTION

Semiconductor Evolution for CATV

GaAs versus Si

- Higher energy bandgap of GaAs (1.43 eV for GaAs vs. 1.11eV for Si)
  - Better isolator

- Higher electron mobility of GaAs compared to Si
  - Enables higher frequencies and bandwidths

- Thermal Design
  - FET design of GaAs transistors enable assembly directly on heat-sink
  - Si bipolar transistor require isolating layer

- FET design offers lower third order distortion because of its square law property

$$ID=Idss\ (1-Vgs/Vp)^2$$

Semiconductor Evolution for CATV

Si vs. GaAs vs. GaN (on SiC substrate)

Property	Si	GaAs	SiC	GaN	Benefits
Energy Gap [eV]	1.11	1.43	3.2	3.4	High Voltage, Ruggedness
Charge Density ($1x10^{13}/cm^2$)	0.3	0.3	0.4	1	High Current Density, Power Handling
Thermal Conductivity (W/cmK)	1.5	0.5	3.3	1.5	
Mobility (cm^2/Vs)	1300	6000	600	1500	High Frequency

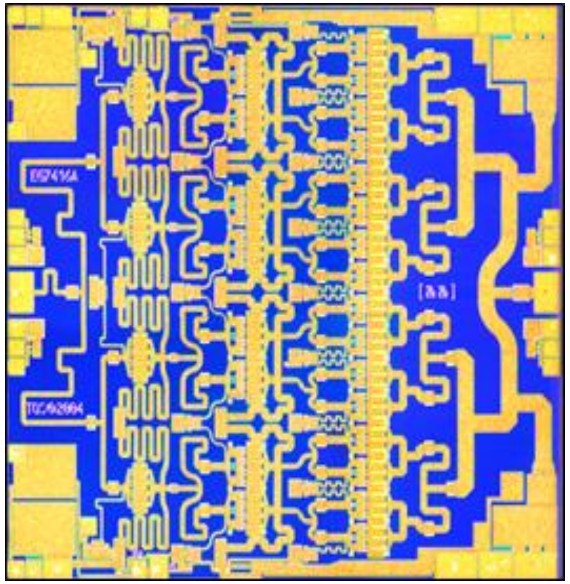
Basics of GaN Devices

Device Density & Thermal Benefits

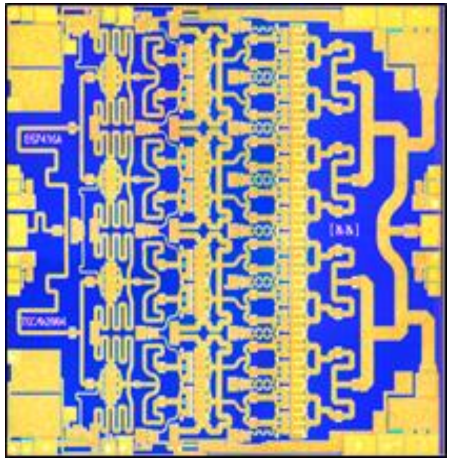
SEMICONDUCTOR DEVICE DENSITY

GaN 10W/mm,
Si-LDMOS 1.4W/mm,
GaAs 1W/mm

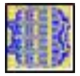
- Benefits of higher power density
  - Smaller geometry for given power level
    - Lower device capacitances: higher bandwidths
    - Lower combining losses: higher gain & efficiency



GaAs (10x GaN)



Si-LDMOS (7.1x GaN)

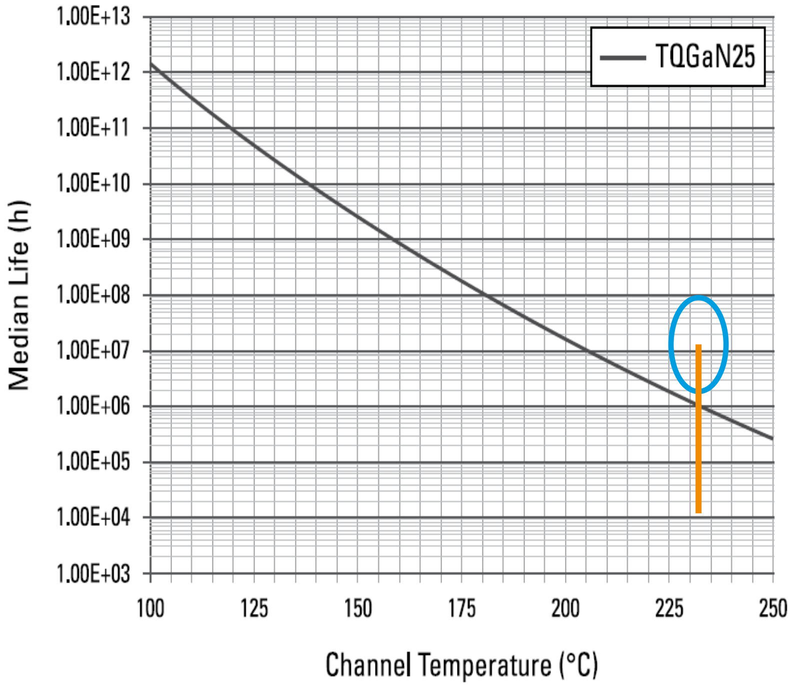


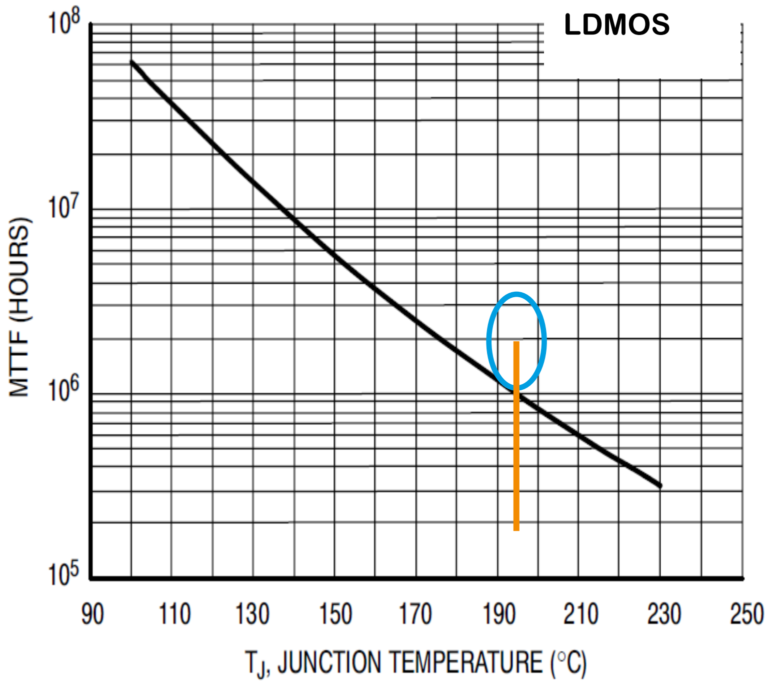
GaN

Basics of GaN Devices

Performance & Thermal Benefits

GaN on SiC devices offer higher power density and can operate at higher channel temperature and still offer 1x10^{6} MTTF reliability





Can dissipate more power without raising device temperature

Thermal Conductivity Comparison

GaAs ~ 0.52W/cm -°C

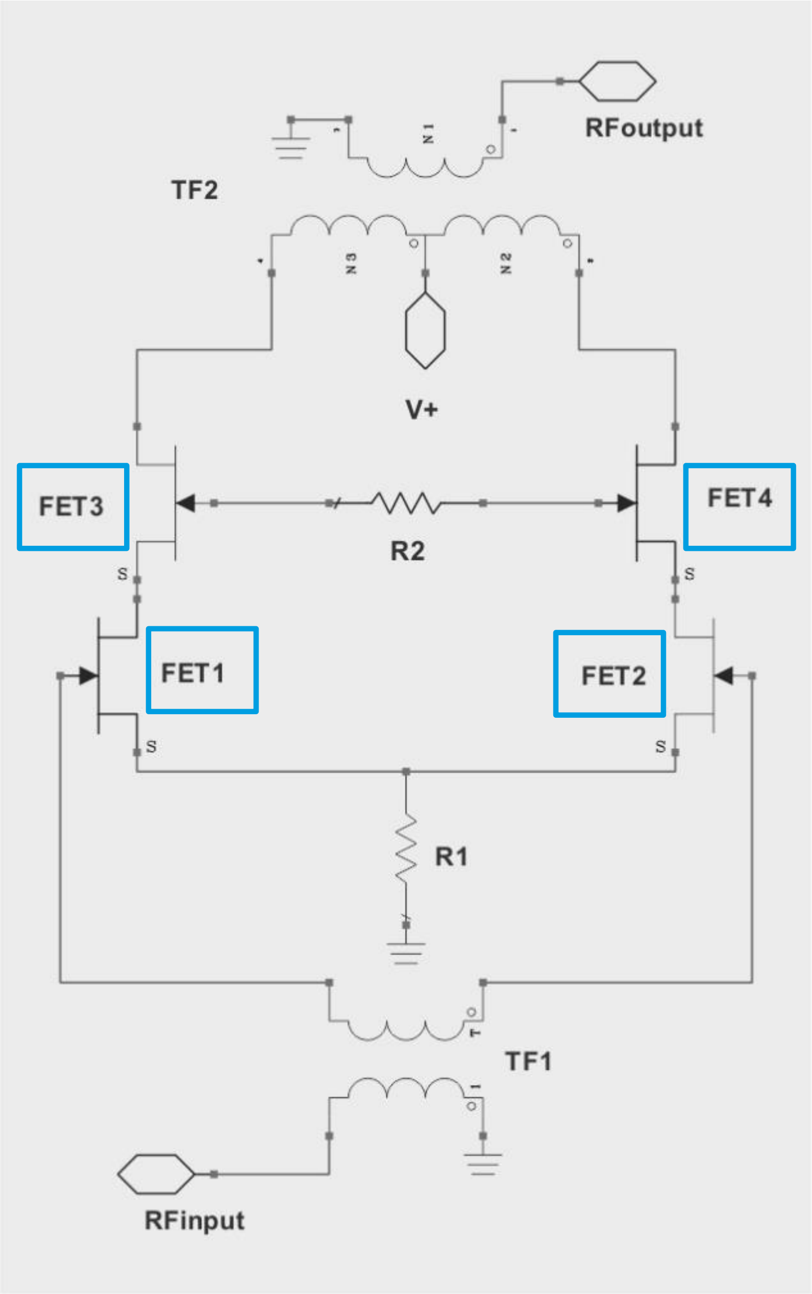
Si ~1.45W/cm -°C

GaN - SiC ~ 3.30W/cm -°C

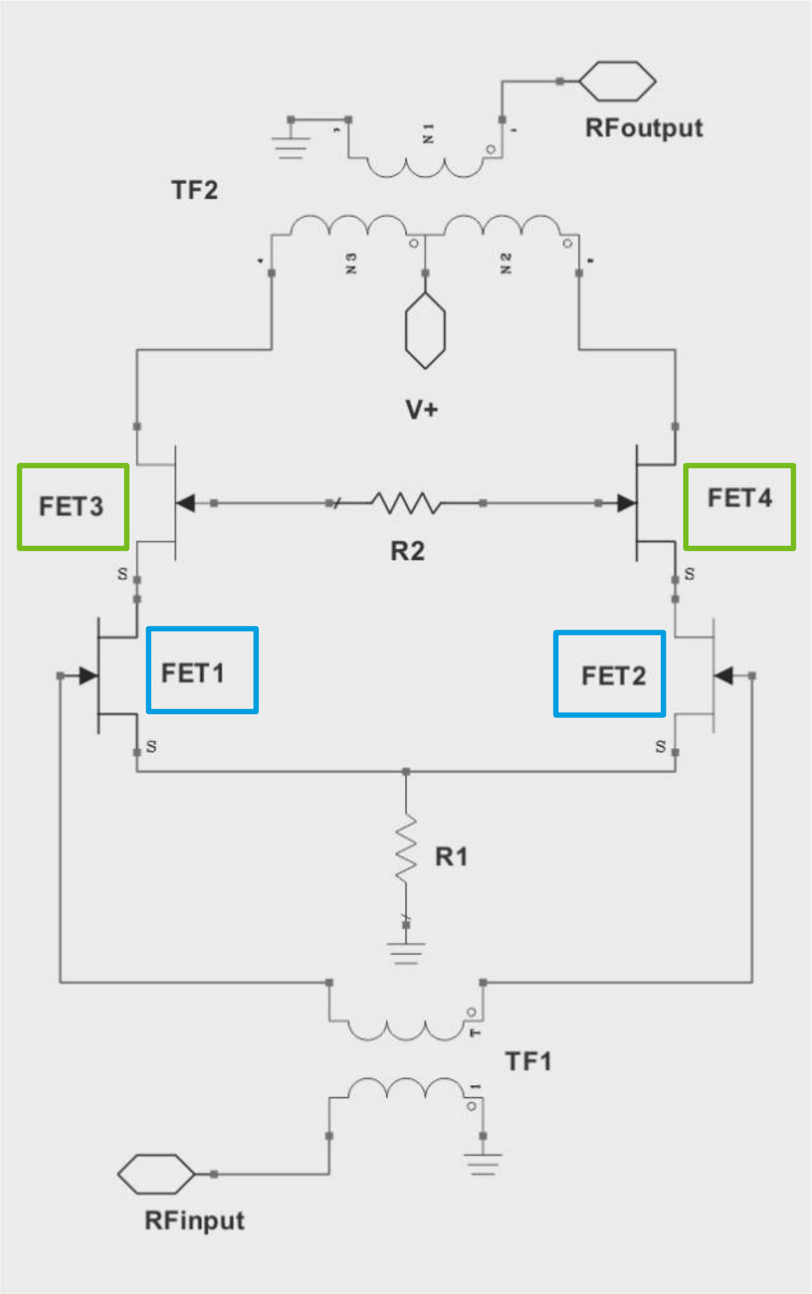
Semiconductor Evolution for CATV

GaAs-based Gain Block

FET1 to FET4 = GaAs



Semiconductor Evolution for CATV



GaAs/GaN-based Gain Block

FET1 to FET2 = GaAs
FET3 to FET4 = GaN

Semiconductor Evolution for CATV

GaN enables CATV customers to:

- Increase the linear output power
    - Keep existing amplifier spacing, thereby minimizing upgrade cost
    - Enable Fiber Deep solutions

- Capable of reducing current by 20%, saving overall power

- Provide High Reliability

- Improved ruggedness compared to GaAs

- Offer mature designs: >20MU CATV GaN Die to date

- Amplifier Design for frequencies > 1.8GHz

LINEARITY CHARACTERIZATION AND TEST DEVELOPMENT

Distortion Parameters

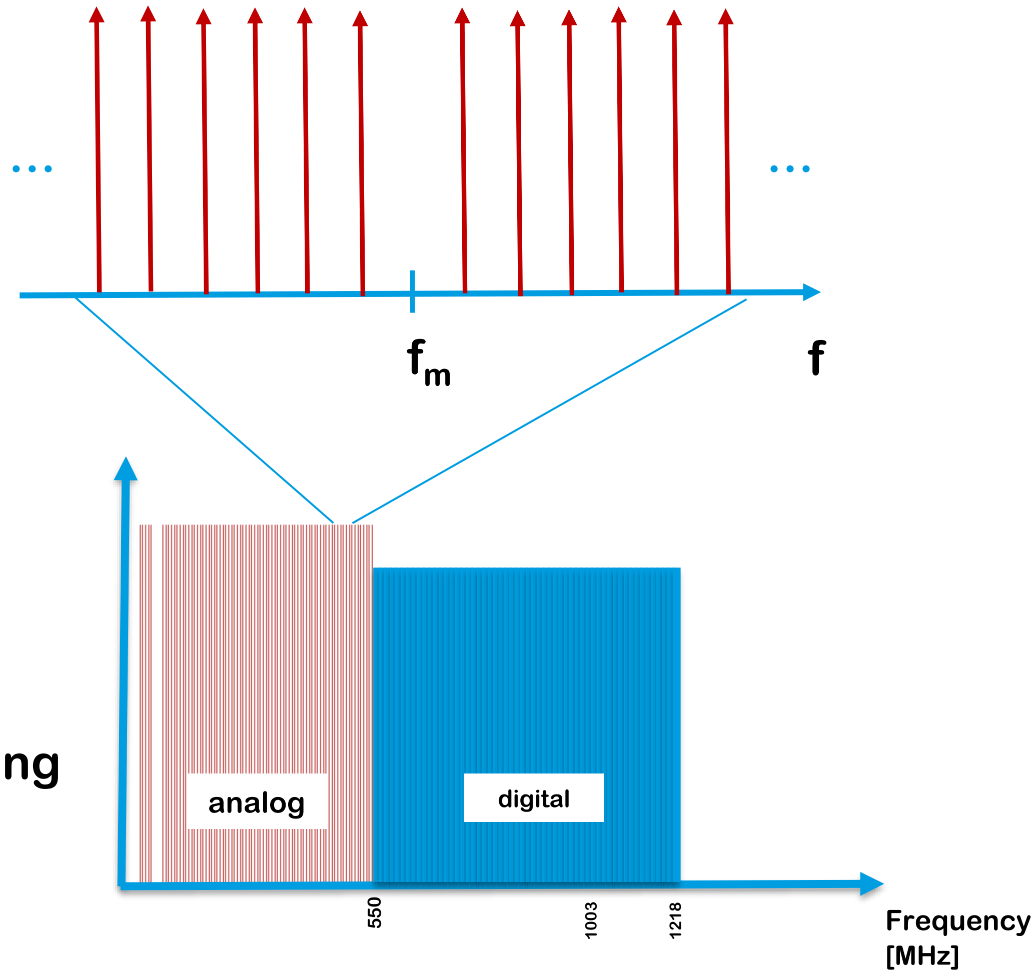
Analog Band

CTB (Composite Triple Beat)

CSO (Composite Second Order)

XMod (Cross Modulation)

CCN (Carrier to Composite Noise)



Channel Loading

Distortion Parameters

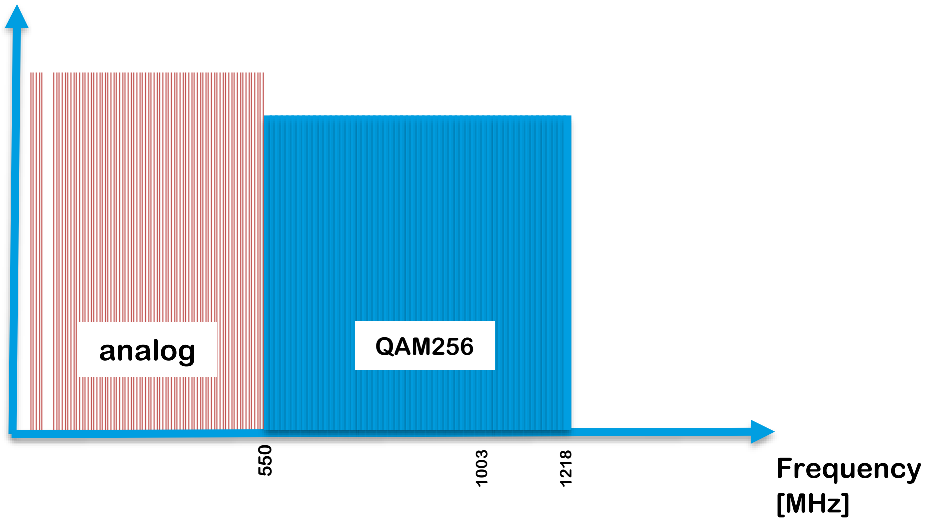
Digital Band

CCN (Carrier to Composite Noise)

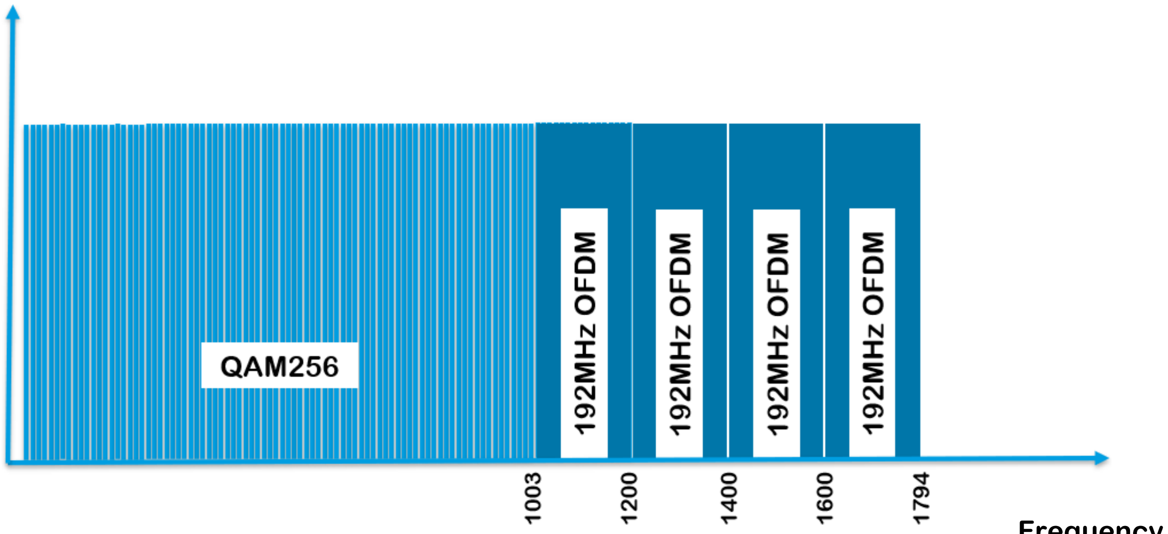
MER (Modulation Error Ratio): $\text{MER (dB)} = 10 \log_{10}(P_{signal}/P_{error})$

BER (Bit Error Ratio) BER = Number of errors / total number of bits sent

Channel Loading Examples for Digital Loading



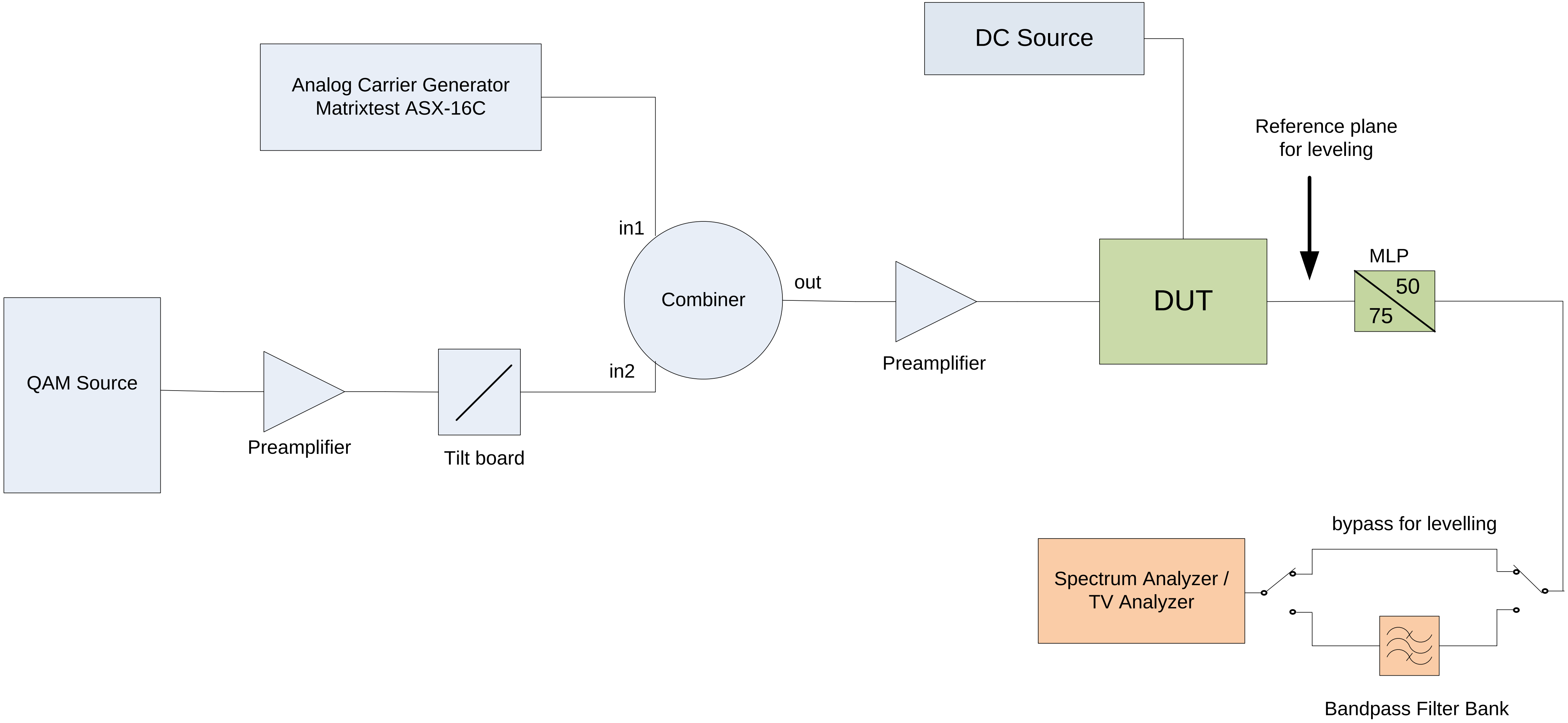
Mixed Channel Loading (analog plus digital)



Pure Digital Loading (SC QAM and OFDM channels)

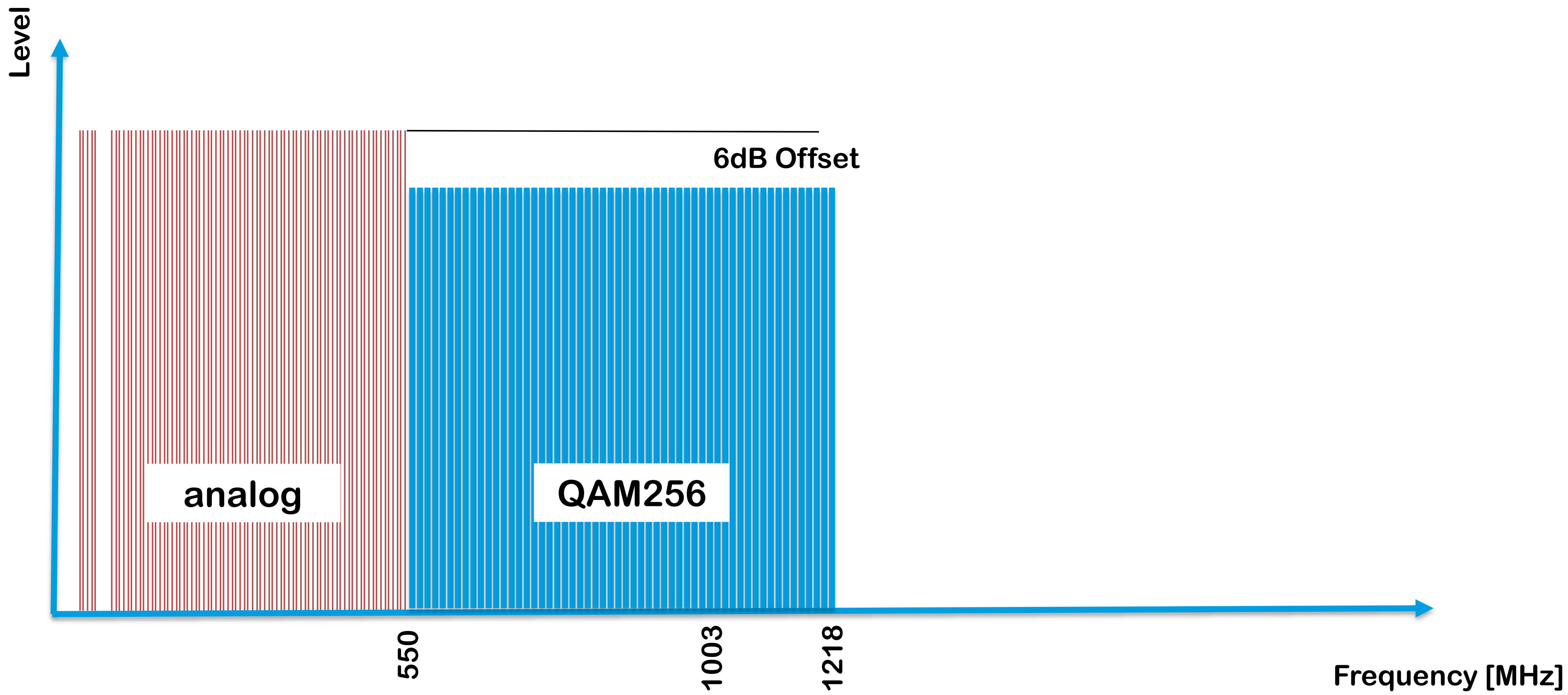
DOCSIS 3.1 / 4.0 Testing

Simplified Block Diagram



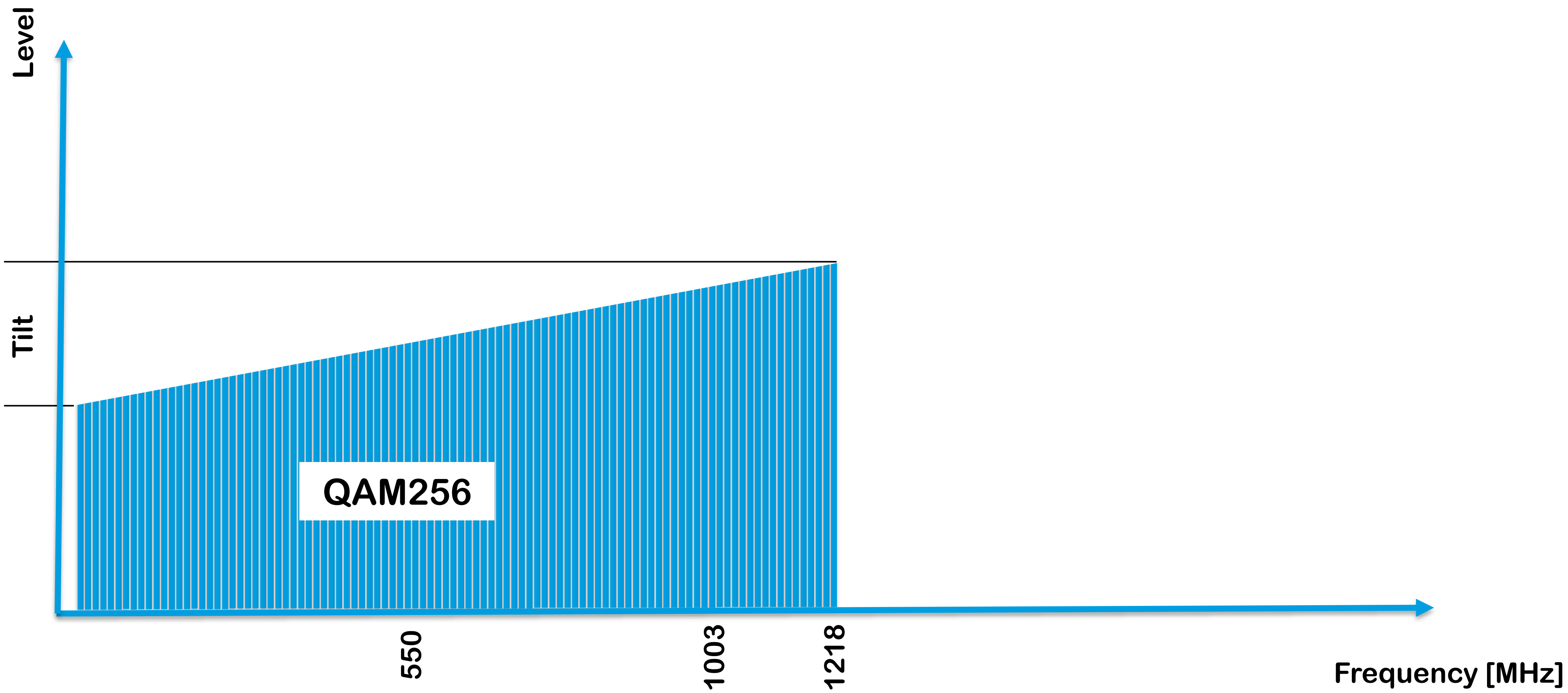
Distortion Test Evolution

Loadings: Mixed Channel Loading (analog plus digital)



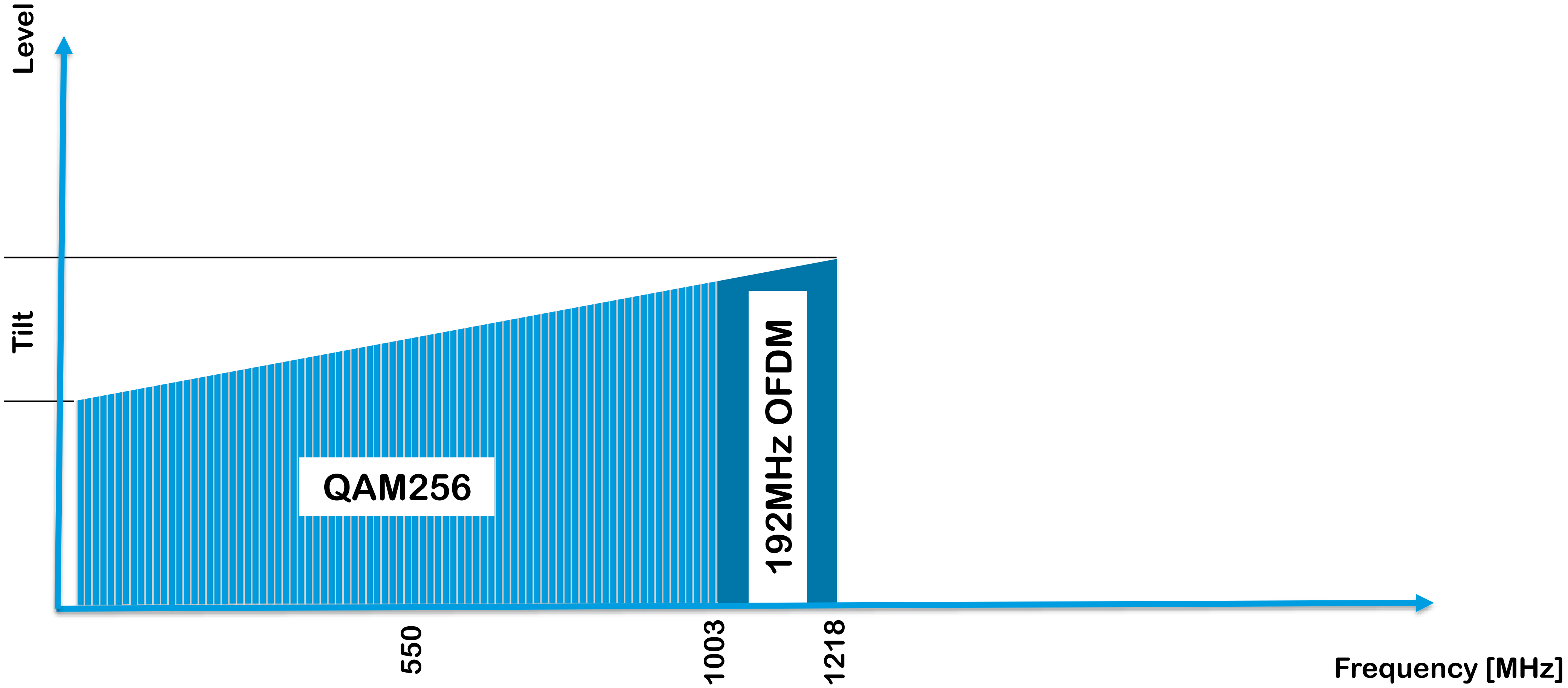
Distortion Test Evolution

Pure Digital Loadings



Distortion Test Evolution

DOCSIS 3.1 loading example

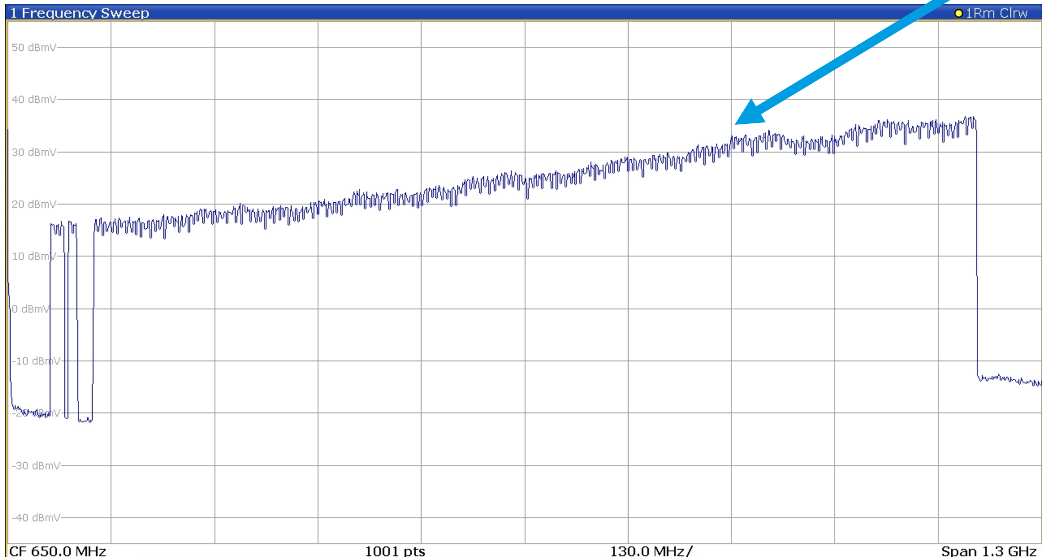


DOCSIS Testing

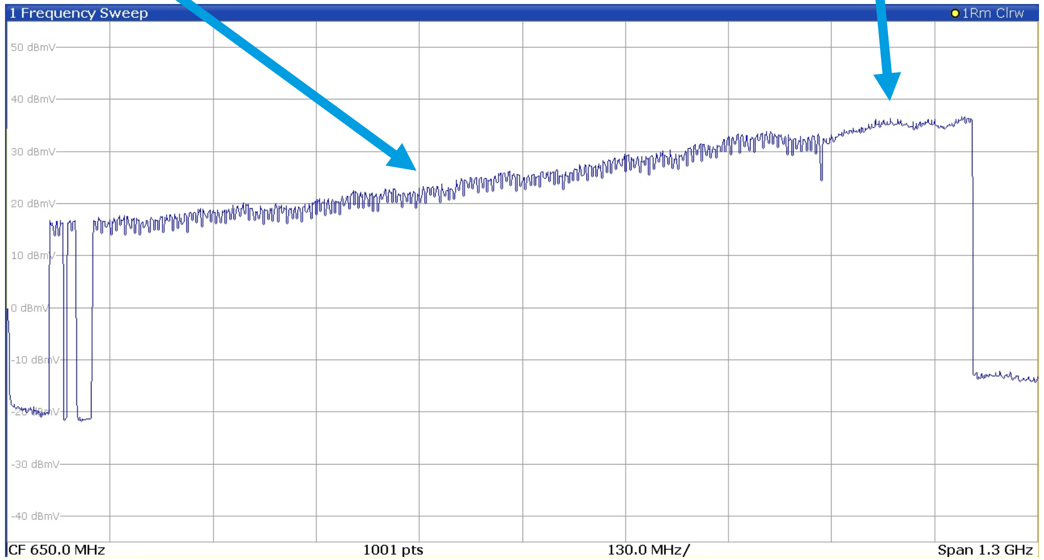
QAM vs. QAM/OFDM Loading

192MHz OFDM channel

QAM 256 channels



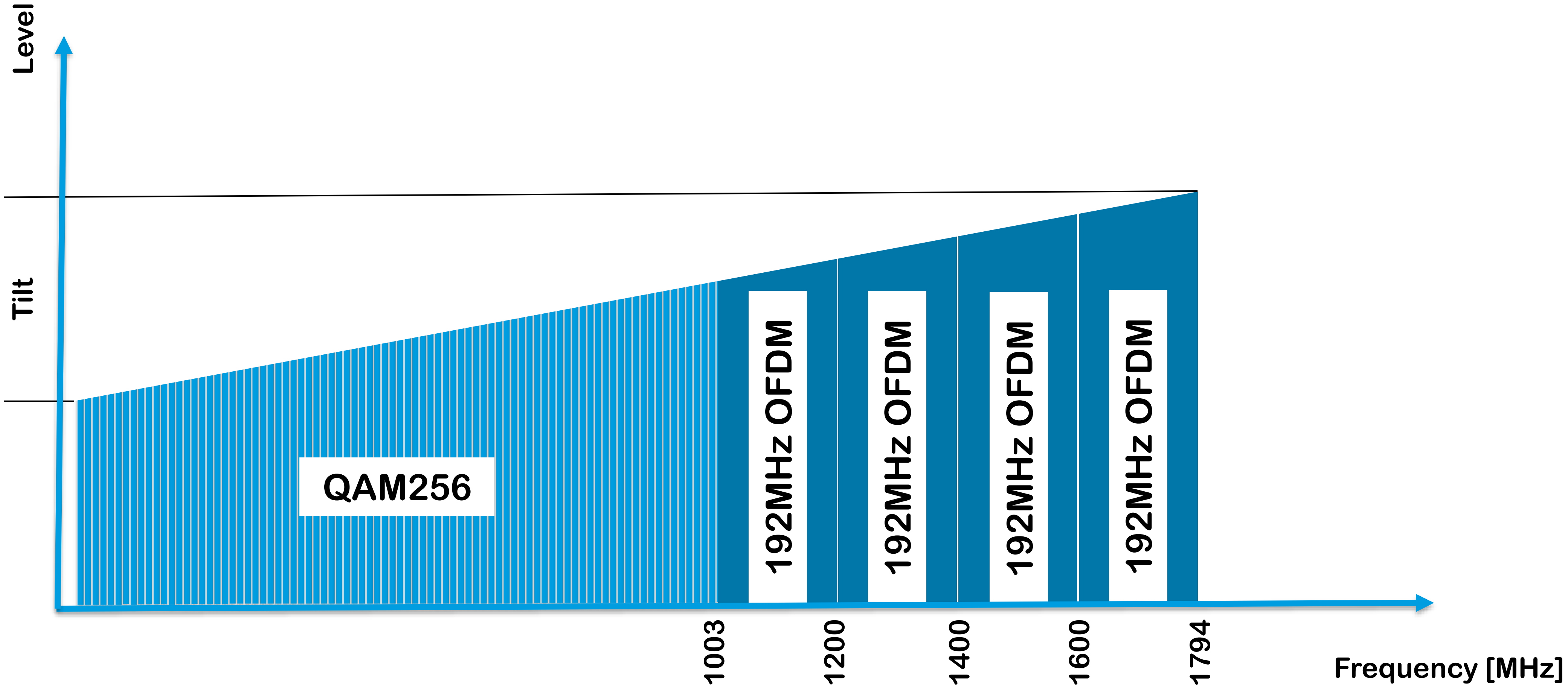
190 channels 256 QAM (ITU-T/J.83 Annex B)
22dB tilt



1 OFDM channel (192MHz) @1122MHz, QAM256 sub carriers
+ 158 channels 256 QAM (ITU-T/J.83 Annex B)
22dB tilt

Distortion Test Evolution

DOCSIS 4.0 loading example



HIGH VOLUME PRODUCTION ASSEMBLY AND TEST

High Volume Production Assembly

Automation is key for multi million pcs./year production

- State of the art solder and epoxy connections to support a proper thermal design
- Automated assembly to ensure a reliable and reproducible performance
- Automated laser-trim and tune for as little as possible part to part variation

High Volume Production Testing

Full specification compliant testing

- 100% small signal and distortion test required
- Multi carrier (composite) distortion test
- Analog channel loading
  - → Mixed channel loading: analog plus digital channels
    - → Pure digital loading
      - → DOCSIS 3.1 → DOCSIS 4.0

[Watch video to learn more]

Thank You

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