50W/cu-in power density, ten times smaller than the state-of-the-art versions at the time. The winner achieved better than 145W/cu-in using WBG technology.

However, there is a vast market for upgrading existing equipment where total redesign is neither feasible nor economical. Most WBG switch solutions are a poor match for designed-in components such as IGBTs or Si-MOSFETs; the gate-drive systems for these components are incompatible with the precise gate-drive voltages needed for say, SiC-MOSFET or GaN HEMT devices. However, cascode SiC JFETs can drop right in. They are available in the traditional TO-247 and TO-220 case styles and can accept a wide range of gate-drive voltages, encompassing every other device standard (**Figure 6**). Some cascodes also include a gate-clamping diode to protect from overvoltage and ESD. Gates of IGBTs and Si-MOSFETs in existing systems are often directly driven through a transformer with inexact voltages, varying with duty cycle. Again, the wide tolerance of the gate voltage drive to SiC cascodes makes substitution easy.

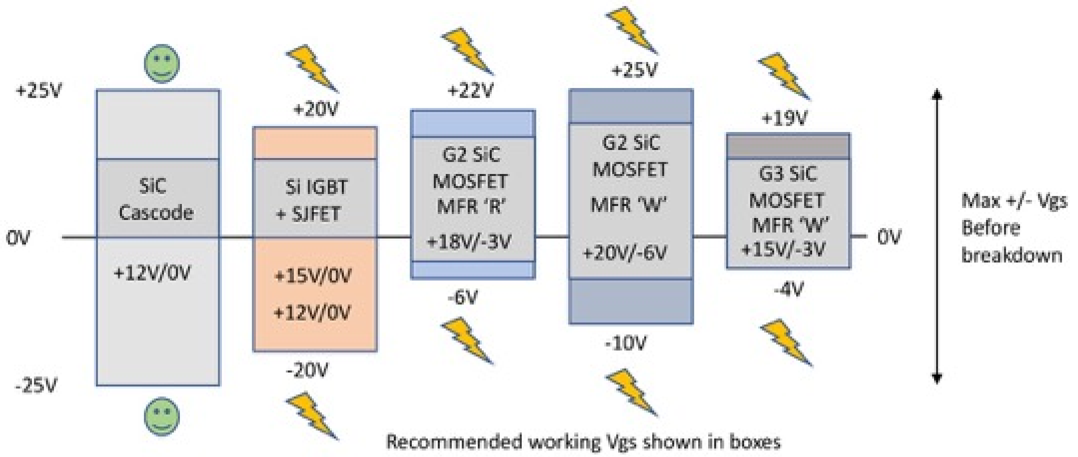

Figure 6. SiC cascodes encompass other allowable gate-drive voltage ranges

The cascode can be slowed down with a choice of gate resistors to match the existing design while dramatically reducing energy loss in the body diode, compared with Si-MOSFETs and IGBTS with an external fast-recovery diode.

System stability and potential speed are improved, with the Miller effect practically absent, and gate-drive power is much reduced. As an example, if a SiC cascode from UnitedSiC-type UJC1210K 800V/20A is compared with an IGBT-type IRG7PH35UD 600V/25A, the total gate charge $Q_{G(total)}$ of the cascode is 47.5nC and that of the IGBT 85nC. This may not seem to be a huge difference, but the cascode can be switched with 0V/12V on its gate while the IGBT may need -9V/+15V. Gate-drive power requirement P_G is given by:

$$P_G = Q_{G(total)} . F . V_{SW}$$

where F is the operating frequency and V_{SW} is the total gate voltage swing, which for the IGBT is twice the cascode value. Total power required is therefore about a quarter with the cascode. Note that the power is constant at any duty cycle as long as the gate is fully charged and discharged each switching period.

SiC cascodes can therefore be dropped into many applications using IGBTs, Si-MOSFETs or even SiC-MOSFETs with little more than a change in series gate resistor value to optimize switching speed. A typical gate-drive circuit for SiC cascodes is given in **Figure 7**. Note that unusually, $R_{(on)}$ is typically lower than $R_{(off)}$, which should have a minimum value of about 10 ohms to avoid internal oscillation in the cascode. The series ferrite bead is optional for damping.

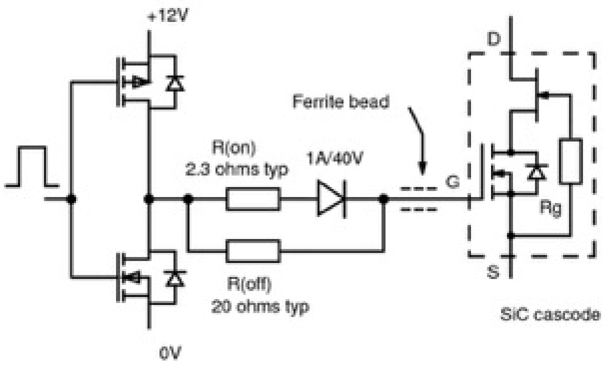

Figure 7. Typical SiC-cascode gate-drive circuit

SiC vs GaN

Coming later than SiC, GaN has had slow adoption due to cost, yield and reliability concerns. It is certainly theoretically capable of higher switching speed than SiC or Si, with its much higher electron mobility, but with a thermal conductivity lower than SiC by a factor of three, its power density potential is limited. Currently SiC devices are common at around 650V through 1.2kV rating and higher, while GaN is limited to around 650V, where it struggles to compete with the current lower cost and proven robustness of the more mature SiC offering at the same voltage. GaN suppliers are hoping that the lower voltage/power market including data centers, EV/HEV and photovoltaics will open up as the hoped-for cost savings materialize. However SiC cascodes also address these market areas, especially in applications for bi-directional DC-DC converters and totem-pole PFC (see below). Data from IHS [1] shows the relative split in usage remaining similar up to the mid-2020s, with the combined WBG market reaching $3.5B, of which GaN is still only about $500M.

SiC is well established in the supply chain now, with parts available in the catalogs of high-service distributors.

SiC trench cascodes have a natural advantage over GaN and indeed Si-MOSFETs and SiC-MOSFETs in that their figure of merit R_{DSA} is much better (**Figure 8**). R_{DSA} is a measure of what combination of ON-resistance is achieved in a particular die area, and if you compare the same power levels across the devices, SiC cascodes for example are 5–10 times better than GaN. In other words, the die size can be 5–10 times smaller, giving lower capacitances and more die per wafer with the associated cost savings. There is less area for heat transfer but SiC has a thermal conductivity three times better than GaN, and anyway tolerates junction temperatures up to 250°C with little variation in characteristics.

Device	SiC Cascode UJC06505K	SiC MOSFET SCT3120KL	E-mode GaN GS66508B	Si Superjunction IPP65R045C7
R_{DSA} mohm-cm^2	0.75	3.5	6.6	10
Rds*Eoss mohm-uJ	255	600	350	462
Vth (V)	5	4.5	1.3	3.5
Avalanche	Yes	Yes	No	Yes
Gate voltage rating (V)	+/-25	+22/-4	+/-10	+/-20
Diode behavior	Excellent	Excellent	Excellent	Poor

Figure 8. Comparative figures of merit

Perhaps a factor that gives SiC an edge in industrial systems, even if GaN voltage ratings improve to compete, is the ability of SiC to withstand voltage avalanche conditions, as can happen with inductive loads. Manufacturers have extensive data showing SiC reliability overvoltage overstress, whereas GaN makes no claims except to say maximum voltage should not be exceeded otherwise damage will occur.

A more tangible difference between the devices is the packaging available; SiC parts are commonly available in TO-247 and T0-220 styles, allowing them to drop in as replacements for MOSFETs and IGBTs in existing designs, giving immediate advantages. Various standard surface mount options are under development. However, GaN device manufacturers have recognized that leaded packages with their inherent speed-limiting connection inductances would be a barrier to getting the best potential performance from their parts. They have therefore mostly opted for surface-mount, single-source, chip-scale packaging, which limits their adoption to new designs. Here, the system design can be matched to the

GaN device properties to give smaller passive components, particularly magnetics and capacitors.

Where we are today

SiC cascodes are commonly available with 650V and 1200V ratings at currents up to around 85A with ON-resistances of around 30 milliohms. “Super cascodes” are also available – series-connected JFETs with greater than 3.5kV rating. SiC-MOSFETs up to 1700V at around 70A and 45 milliohms are available, but their internal body diode is relatively slow, unlike with cascodes, and often has to be bypassed with a costly, fast SiC external diode when the application requires it, for example in hard-switched bridge circuits.

GaN devices top out at 650V with about 60A and 25 milliohms rating, equivalent to many SiC parts but theoretically capable of faster switching. Interestingly, available GaN devices at 100V rating are no better than traditional Si-MOSFETs for ON-resistance and therefore rely on their speed advantage to counter the significant cost added over commodity MOSFETs at this level.

For the future, the IHS data clearly shows a significant increase in WBG device design-ins, although IGBT and traditional MOSFET sales will also increase in a growing market. The debate is how the different WBG devices might dominate particular market segments. **Figure 9** is one view of the possible future split in power and operating frequency for power devices, although the GaN presence again depends on prospective cost reductions.

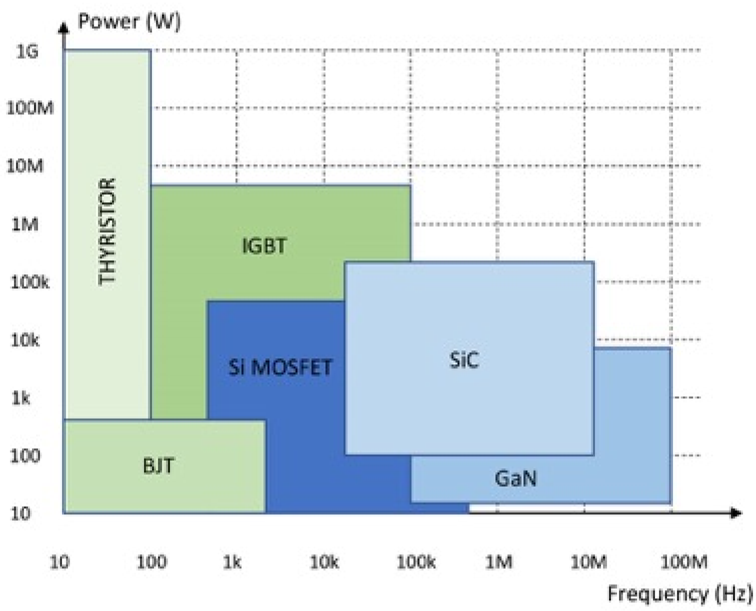

Figure 9. A possible future scenario

The applications

The high temperature capability of WBG devices with potentially fast switching and low losses makes them ideal for military and industrial applications where performance is key. Bridge circuits are an obvious candidate used at high power for inverters, welding, class D audio amplifiers, motor drives and more. A particular application where major benefits are seen is the bridgeless totem-pole PFC circuit. (**Figure 10**). Here, previous circuits using Si technology have been limited by the slow performance of body diodes in the MOSFETs typically used. A parallel SiC diode helps, but defeats the object of reducing component count. This forces “critical conduction” mode to be used, which sets switching current to zero at the end of each conduction period. However, this variable-frequency mode produces high peak currents and high EMI. Using cascode SiC JFETs, “continuous conduction” mode can be used, increasing efficiency, reducing inductor size and easing filtering and EMI problems with fixed operating frequency. An example circuit using UnitedSiC UJC06505K devices at 1.5kW and 230VAC-line showed an impressive efficiency of 99.4% [2].

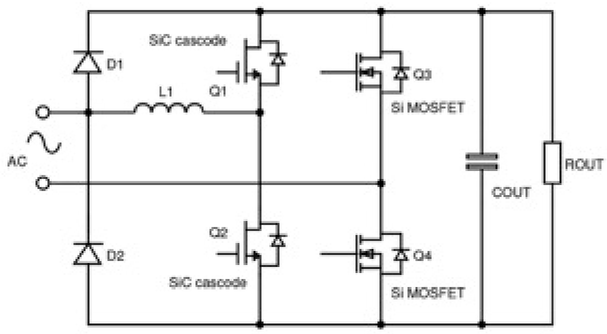

Figure 10. SiC devices in a bridgeless totem-pole PFC stage

Achieving high efficiency in converter primary switches must be matched with similar improvements in rectification for DC outputs. Again, SiC cascodes fit here as they can be configured for “synchronous rectification” (**Figure 11**). In so-called third-quadrant operation current flows from source to drain of one or other of the cascodes through the output inductor to load during the “forward” and “flywheel” periods of forward or buck-derived converters. Current flow through the body diode sets the JFET gate-source voltage to approximately +0.7V, turning it naturally hard ON. If the cascode gate is set high, the internal Si-MOSFET channel conducts and the total ON-resistance becomes the $R_{DS(on)}$ of the cascode, giving low conduction losses. Q1 forms the flywheel rectifier and Q2 the forward rectifier.

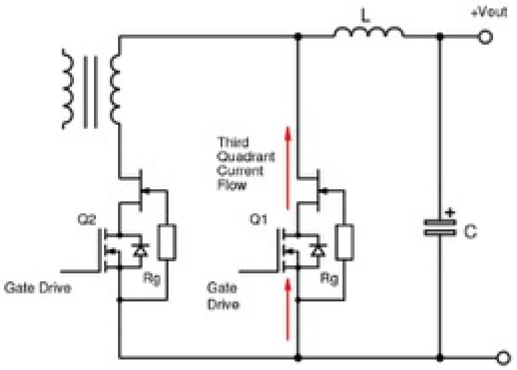

Figure 11. SiC cascodes in synchronous rectification

Robustness concerns

In high-power applications, robustness with transient short-circuits and overvoltages is a major concern. A typical cascode SiC JFET has excellent characteristics in this respect. The pinch-off effect has already been mentioned, limiting saturation current with its negative temperature coefficient.

For overvoltages, the SiC JFET gate-drain diode conducts, causing current flow in the built-in gate resistor and turning the JFET channel ON to clamp the overvoltage. Again, the inherent high temperature rating of the SiC die gives a good margin of safety for significant avalanche energy levels even in the relatively small die sizes encountered. As an additional confidence measure, all parts are subjected to 100% avalanche at final test [3].

References

1. https://technology.ihs.com/521146/sic-gan-power-semiconductors-2016
2. http://unitedsic.com/wp-content/uploads/2016/11/Totem-Pole-PFC-AppNotes.pdf
3. http://unitedsic.com/wp-content/uploads/2016/02/bp_2015_05-Robustness-of-SiC-JFETs.pdf

For more information, visit: http://www.unitedsic.com