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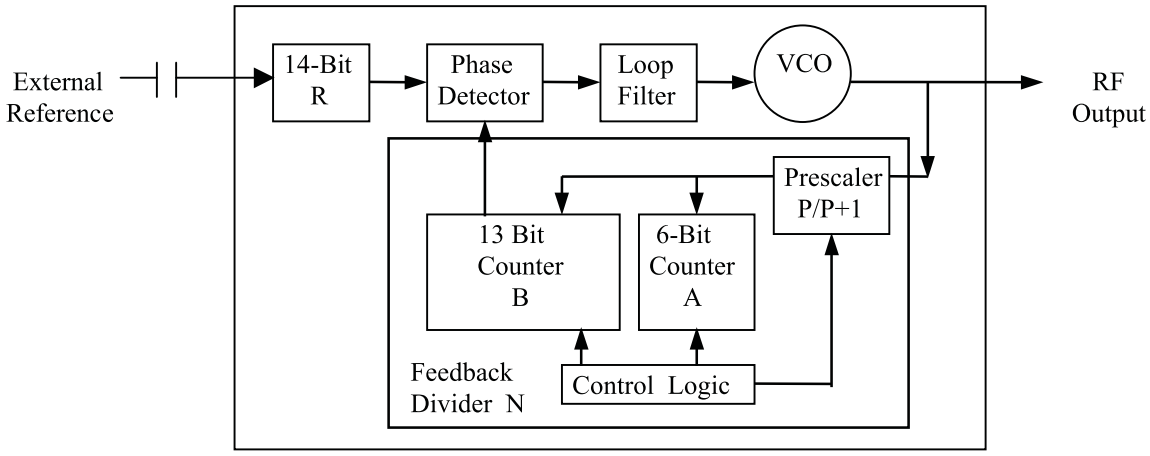
AN113: PLL Synthesizer Programming

Overview

The Phase Locked Loop (PLL) Synthesizer is programmed via a 3-wire serial interface. There are three words that need to be transmitted to the unit. These are the Function word, the Reference Counter word and the AB-Counter word. This programming note explains how to calculate the bit pattern for each word to obtain a particular output frequency, and how the bits must be sent. The block diagram for the unit is shown below.



There are some limits on the values for A, B, R, and P.

$1 \le R \le 16383$
$0 \le A \le 63$
$3 \le B \le 8191$
$P=8, P+1=9$ for Options 0xxxxx
$P=16, P+1=17$ for Options 1xxxxx
$P=32, P+1=33$ for Options 2xxxxx
$P=64, P+1=65$ for Options 3xxxxx
$N=BP+A$ and $B \ge A$

The programmed values are calculated with these equations:

$$R=\left(\frac{\text{Reference Input}}{\text{Channel Spacing}}\right)$$

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For example, in a system with 200kHz channel spacing and a 10MHz reference.

$$R=\frac{10\,MHz}{200\,kHz}=50$$

This produces a 14-bit digital word of: MSB 0 0 0 0 0 0 0 0 1 1 0 0 1 0 LSB

This meets the requirements for R.

$$1\leq 50\leq 16383$$

The feedback divider is set as follows:

$$N=\frac{\text{Output Frequency}}{\text{Channel Spacing}}=(B\text{x}P)+A$$

so

$$B=\text{truncate}\left(\frac{N}{P}\right)$$

$$A=N-(B\text{x}P)$$

For example using the same 200kHz channel spacing from above and an output frequency of 900MHz with programming option 2xxxxx yields:

$$N=\frac{900\,MHz}{200\,kHz}=4500$$

so

$$B=\text{truncate}\left(\frac{4500}{32}\right)=140$$

$$A=4500\text{-}(140\text{x}32)=20$$

The 13-bit pattern for B is then: MSB 0 0 0 0 0 1 0 0 0 1 1 0 0 LSB

And the 6-bit pattern for A is: MSB 0 1 0 1 0 0 LSB

These numbers meet the requirements for B and A:

$140\geq 20$
$3\leq 140\leq 8191$
$0\leq 20\leq 63$

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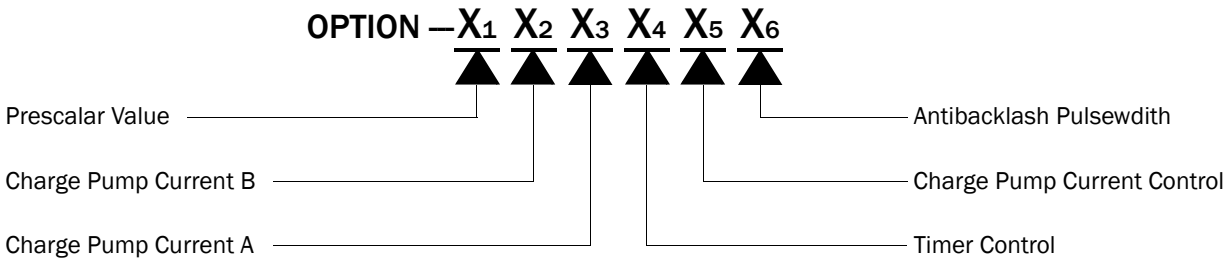
The 3 words to program the unit should be sent in the following order:

Function Word
Reference Counter Word
AB-Counter Word

The contents of each word may vary depending on the programming option specified in the product specification. The option is a six-digit number which specifies the following parameters:



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Function Word:

The function word will only vary depending on the programming option specified in the product specification. Use the tables below to choose the bit pattern based on the programming option.

MSB **LSB**

b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
P_2	P_1	0	B_3	B_2	B_1	A_3	A_2	A_1	T_4	T_3	T_2	T_1	F_2	F_1	0	1	0	0	1	0	0	1	1

Timer Control

Option	T_4	T_3	T_2	T_1	Description
xxx0xx	0	0	0	0	3 Cycles
xxx1xx	0	0	0	1	7 Cycles
xxx2xx	0	0	1	0	11 Cycles
xxx3xx	0	0	1	1	15 Cycles
xxx4xx	0	1	0	0	19 Cycles
xxx5xx	0	1	0	1	23 Cycles
xxx6xx	0	1	1	0	27 Cycles
xxx7xx	0	1	1	1	31 Cycles
xxx8xx	1	0	0	0	35 Cycles
xxx9xx	1	0	0	1	39 Cycles
xxxAxx	1	0	1	0	43 Cycles
xxxBxx	1	0	1	1	47 Cycles
xxxCxx	1	1	0	0	51 Cycles
xxxDxx	1	1	0	1	55 Cycles
xxxExx	1	1	1	0	59 Cycles
xxxFxx	1	1	1	1	63 Cycles

Charge Pump Current A

Option	A_3	A_2	A_1	Description
xx0xxx	0	0	0	1/8 max.
xx1xxx	0	0	1	1/4 max.
xx2xxx	0	1	0	3/8 max.
xx3xxx	0	1	1	1/2 max.
xx4xxx	1	0	0	5/8 max.
xx5xxx	1	0	1	3/4 max.
xx6xxx	1	1	0	7/8 max.
xx7xxx	1	1	1	max.

Charge Pump Current B

Option	B_3	B_2	B_1	Description
x0xxxx	0	0	0	1/8 max.
x1xxxx	0	0	1	1/4 max.
x2xxxx	0	1	0	3/8 max.
x3xxxx	0	1	1	1/2 max.
x4xxxx	1	0	0	5/8 max.
x5xxxx	1	0	1	3/4 max.
x6xxxx	1	1	0	7/8 max.
x7xxxx	1	1	1	max.

Prescalar Values

Option	P_2	P_1	Description
0xxxxx	0	0	8/9
1xxxxx	0	1	16/17
2xxxxx	1	0	32/33
3xxxxx	1	1	64/65

Charge Pump Current Control

Option	F_2	F_1	Description
xxxx0x	0	0	Current A
xxxx1x	0	0	Current B
xxxx2x	1	1	Fastlock

Reference Counter Word:

The Reference Counter Word will vary based on the programming option specified in the product specification and the value R. Use the table below to choose the bit pattern based on the programming option and replace Bits b15 to b2 with the bit pattern for R that was calculated. The bits listed below are for the above example.

MSB LSB

								14 bit R value															
b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0	0	W_2	W_1	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0

Antibacklash Pulsewidt

Option	W_2	W_1	Description
xxxxx0	0	0	3.0nsec
xxxxx1	0	1	1.5nsec
xxxxx2	1	0	6.0nsec

AB - Counter Word:

The AB Counter Word will vary based on the programming option specified in the product specification and the values of A and B. Use the table below for the bit pattern and replace Bits b20 to b8 with the bit pattern for A that was calculated and Bits b7 to b2 with the bit pattern for B. The bits listed below are for the above example.

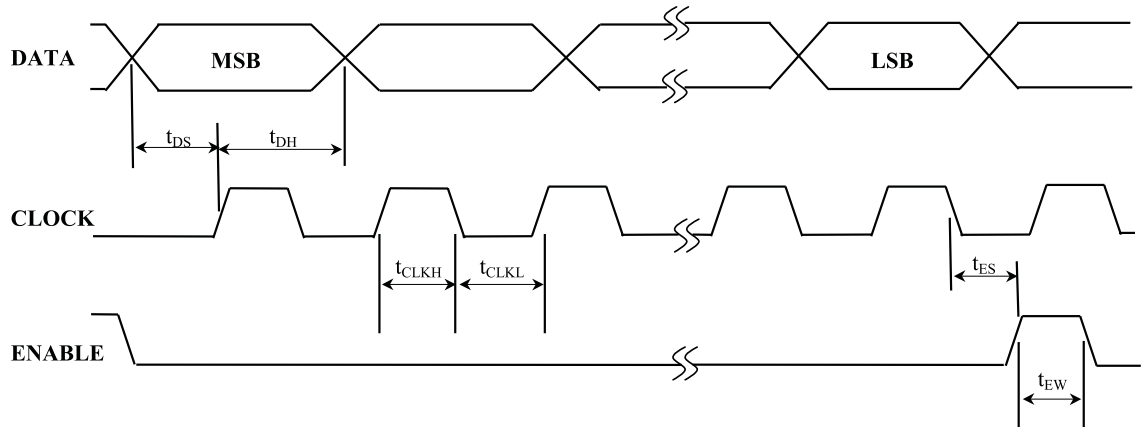
MSB LSB

			13 bit B value													6 bit A value							
b23	b22	b21	b20	b19	b18	b17	b16	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
0	0	F_3	0	0	0	0	0	1	0	0	0	1	1	0	0	0	1	0	1	0	0	0	1

Charge Pump Current Control

Option	F_3	Description
xxxx0x	0	Current A
xxxx1x	1	Current B
xxxx2x	1	Fastlock

Timing for Words:



all timing values are 10% to 90%

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Clock, Data, and Enable Inputs					
Input Capacitance (C_I)			10	pF	
H-Input Current (I_H)			1	µA	
L-Input Current (I_L)	-1			µA	
H-Input Voltage (V_{IH})	$.8V_{CC}$			V	
L-Input Voltage (V_{IL})			$.2V_{CC}$	V	
Data to Clock Setup (t_{DS})	10			nSec	
Data to Clock Hold (t_{DH})	10			nSec	
Clock High Duration (t_{CLKH})	25			nSec	
Clock Low Duration (t_{CLKL})	25			nSec	
Clock to Enable Setup (t_{ES})	10			nSec	
Enable Pulsewidth (t_{EW})	20			nSec	
RF Output					
Coupling		AC			
Output Impedance		50		Ω	
Reference Input					
Input Voltage	0.4	0.75	2.0	Vp-p	
Input Frequency (R_I)	5		100	MHz	

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