RF1138

5 bit Tunable Capacitor with Switch

The RF1138 is a 0.5pF – 8.8pF 5 bit, 32 states PAC (Programmable Array of Capacitors) for tunable RF applications. The RF1138 features a low loss switch. With a tunable capacitor and a switch, RF1138 can be configured in different architectures for impedance matching requirements. The high power handling, high Q, and excellent linearity make it ideal for use in multimode GSM/EDGE/WCDMA/LTE Tx/Rx antenna tuning applications. The RF1138 includes an integrated LDO (Low Drop Out) regulator to enable V_{BAT} connect. RF1138 is packaged in a compact 1.6 mm x 2.0 mm, 14-pin, wafer level chip scale package (WLCSP).

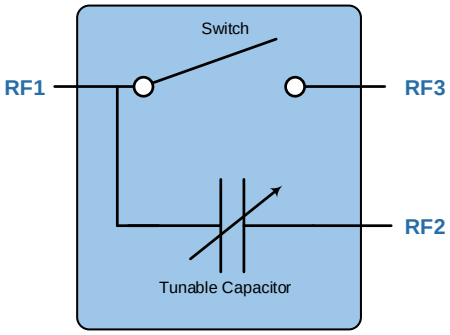


Figure 1. Functional Schematic

Features

- 5 bit, 32 states programmable capacitor array
- Programmable low loss switch
- RFFE control interface
- Wide tuning range (0.5 pF to 8.8pF in series configuration)
- High RF power handling (40 V_P RF voltage)
- High linearity
- Wide voltage supply range
- Low current consumption (typ. 60 µA at 2.85 V)
- HBM ESD Class 2 compliant
- Small 1.6 mm x 2.0 mm, 14 pin wafer level chip scale package (WLCSP)

Applications

- Multimode GSM/EDGE/WCDMA/LTE Tx/Rx main antenna tuning applications
- Antenna tuning networks
- Tunable RF filters
- Tunable RF matching networks
- Phase shifters

Ordering Information

RF1138DK	Design Kit
RF1138SR	100-pc 7" Reel
RF1138TR13-5K	5000-pc, 13" Tape and Reel

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage, V_{DD}	+4.8	V
VIO	+2.8	V
SDATA/SCLK	+2.8	V
Max voltage between any combination of RF ports or ground V_{RF} VDD = 2.85V, VIO = 1.8V, Temp=25C	40	V_P
Operating Case Temperature	-30 to +90	°C
Storage Temperature	-40 to +150	°C
ESD All Pins, HBM, JESD22-A114	2	kV

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Nominal conditions unless otherwise specified. V_{DD} = 2.85V, VIO = 1.8V, Temp = 25°C, 50Ω.
Operating supply voltage, V_{DD}	2.4	-	4.5	V	
Supply current, I_{DD}		60		µA	Active Mode
		-		µA	Low Power Mode
		-		µA	Shutdown Mode
VIO	1.65	1.8	1.95	V	
VIO Current, I_{VIO}		-		µA	
SDATA, SCLK Control voltage HIGH	0.8*VIO	VIO	1.95	V	Must not exceed VIO voltage
SDATA, SCLK Control voltage LOW	0	0	0.45	V	
VIO_{RST}[1]			0.24	V	Register RESET (VIO)[1] - Min voltage required to RESET all registers
Switching Speed, T_{SS} (Small Signal)			15	µs	Time from 50% falling edge of bus park of the activating command sequence to 10%-90% capacitance delta between any two states.

Application Notes

[1] – Application note:

Register RESET by Software	Write a "01" to bits 7:6 of the PM_TRIG register (0x001C, puts the device into STARTUP state). All the registers are reset by setting the PWR_MODE into the STARTUP state Note: The Software RESET should be used if the minimum VIO voltage is ≥ 0.45V since a VIO of ≥ 0.45V will not reset the registers.

Electrical Specifications – Series Configuration, Linear Parameters

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Nominal conditions unless otherwise specified. V_{DD} = 2.85V, VIO = 1.8V, Temp = 25°C, 50Ω.
Minimum Series Capacitance		0.50		pF	State 0
Maximum Series Capacitance		8.80		pF	State 31
Switch Insertion Loss State 32 **(RF2 - Open)**		0.28 0.42		dB dB	915 MHz 1910 MHz
Switch Insertion Loss State 32 **(RF2 - 50Ω)**		0.4 0.8		dB dB	915 MHz 1910 MHz

Electrical Specifications – Series Configuration, Nonlinear Parameters

Parameter	Specification			Unit	Conditions
	Min	Typ	Max		
					Nominal conditions unless otherwise specified. V_{DD} = 2.85V, VIO = 1.8/0V, Temp = 25°C, 50Ω.
Second Harmonics, $2f_0$		-100 -110		dBc	State 0 to State 31, Pin = 35dBm, 915 MHz Switch State, Pin = 35dBm, 915 MHz
Third Harmonics, $3f_0$		-82 -94 -100 -92		dBc	State 0 to State 3, Pin = 35dBm, 915 MHz State 4 to State 15, Pin = 35dBm, 915 MHz State 16 to State 31, Pin = 35dBm, 915 MHz Switch State, Pin = 35dBm, 915 MHz
Second Harmonics, $2f_0$		-105		dBc	All States, Pin = 33dBm, 1910 MHz
Third Harmonics, $3f_0$		-85 -95 -100 -94		dBc	State 0 to State 3, Pin = 33dBm, 1910 MHz State 3 to State 15, Pin = 33dBm, 1910 MHz State 16 to State 31, Pin = 33dBm, 1910 MHz Switch State, Pin = 33dBm, 1910 MHz
IIP2, Low		120		dBm	Refer to IIP2 Conditions Table
IIP2, High		130		dBm	
IIP3 Cell		75		dBm	Refer to IIP3 Conditions Table
IIP3 IMT		75		dBm	
Receive Spurious 700 – 2700 MHz $P_{OUT\ Spur}$		-115		dBm	No RF signal
		-110		dBm	RF – 915MHz at 35dBm
		-110		dBm	RF – 1910 at 33dBm

IIP2 Test Conditions

Band	In-band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band I Low (IMT)	2140	1950	+20	190	-15
Band I High (IMT)	2140	1950	+26	4090	-20
Band II Low (PCS)	1960	1880	+20	80	-15
Band II High (PCS)	1960	1880	+26	3840	-20
Band V Low (Cell)	881.5	836.5	+20	45	-15
Band V High (Cell)	881.5	836.5	+26	1718	-20
Band VIII Low	942.5	897.5	+20	45	-15
Band VIII High	942.5	897.5	+26	1840	-20

IIP3 Test Conditions

Band	In-band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band I High (IMT)	2140	1950	+20	1760	-15
Band V High (Cell)	881.5	836.5	+20	791.5	-15

RFFE Communication

The RF1138 is controlled by a RFFE compatible interface. An external pin, ID0, on the part provides the user with an option to set 1 bit of the USID.

The ID0 pin is internally connected to V_{High} to map the S0 address bit of USID to 1. The ID0 pin should be connected to ground to map the address bit S0 to 0.

ID0 Pin Connection	S0 Address	Antenna tuner USID [S3:S0]
No connect	1	0111 (Default)
Connect to ground	0	0110 (Programmable)

Register Map

Register	Description
Register 0	Set the state of the PAC and switch
Register 28	Select the operating state of the device
Register 29	Contains the Product ID
Register 30	Contains the least significant bits of manufacturer ID
Register 31	Contains the USID and remaining bits of the manufacturer ID

Register 0 Data Frame[2]

Data bits	Function and description
D7	Reserved for future use.
D6	Reserved for future use.
D5	Data bit D5, controls the switch. 0 = Switch is OFF, 1 = Switch is ON.
D4,D3,D2,D1,D0	Data bits D4-D0 control the state of the PAC. (D4 is most significant bit, D0 is least significant bit).

Product ID = 01100000

Application Notes

[2] – Application note:

Shadow Registers in Direct Mode Writes	The *Shadow Register* does not get overwritten during a write to Register 0 in *Direct Mode*. The means the shadow register might contain old data from the last time Register 0 was in *Trigger Mode*. Anytime Register 0 is placed in Trigger Mode, it should be written to prior to triggering in order to ensure correct data is loaded.

Capacitance Table - Register 0 Data Frame

State	Capacitance Table						Capacitance (pF)
	D5	D4	D3	D2	D1	D0	
State 0	0	0	0	0	0	0	0.50
State 1	0	0	0	0	0	1	0.76
State 2	0	0	0	0	1	0	1.03
State 3	0	0	0	0	1	1	1.30
State 4	0	0	0	1	0	0	1.56
State 5	0	0	0	1	0	1	1.82
State 6	0	0	0	1	1	0	2.09
State 7	0	0	0	1	1	1	2.35
State 8	0	0	1	0	0	0	2.62
State 9	0	0	1	0	0	1	2.88
State 10	0	0	1	0	1	0	3.15
State 11	0	0	1	0	1	1	3.41
State 12	0	0	1	1	0	0	3.68
State 13	0	0	1	1	0	1	3.94
State 14	0	0	1	1	1	0	4.21
State 15	0	0	1	1	1	1	4.47
State 16	0	1	0	0	0	0	4.83
State 17	0	1	0	0	0	1	5.09
State 18	0	1	0	0	1	0	5.36
State 19	0	1	0	0	1	1	5.62
State 20	0	1	0	1	0	0	5.89
State 21	0	1	0	1	0	1	6.15
State 22	0	1	0	1	1	0	6.42
State 23	0	1	0	1	1	1	6.68
State 24	0	1	1	0	0	0	6.95
State 25	0	1	1	0	0	1	7.21
State 26	0	1	1	0	1	0	7.48
State 27	0	1	1	0	1	1	7.74
State 28	0	1	1	1	0	0	8.01
State 29	0	1	1	1	0	1	8.27
State 30	0	1	1	1	1	0	8.54
State 31	0	1	1	1	1	1	8.80
Switch Mode State 0	1	0	0	0	0	0	Switch + State 0
Switch Mode State 31	1	1	1	1	1	1	Switch + State 31

Note – Capacitance values rounded to two decimal places.

Register Definition

Register Map

Registers		Fields				Default Values		Supported Access		
Address	Name	Bit(s)	Function	Description		Reset	Low Pwr	B/G ID	Trigger	R/W
0x0000	REGISTER_0	7:6	SPARE			0b00	N/A	No	0 - 2	R/W
		5	Switch	0: Switch is OFF	1: Switch is ON	0	N/A	No	0 - 2	R/W
		4:0	PAC_CTRL[4:0]	00000: State 0	01011: State 11	10110: State 22	0b0_0000	N/A	No	0 - 2	R/W
				00001: State 1	01100: State 12	10111: State 23					
				00010: State 2	01101: State 13	11000: State 24					
				00011: State 3	01110: State 14	11001: State 25					
				00100: State 4	01111: State 15	11010: State 26					
				00101: State 5	10000: State 16	11011: State 27					
				00110: State 6	10001: State 17	11100: State 28					
				00111: State 7	10010: State 18	11101: State 29					
				01000: State 8	10011: State 19	11110: State 30					
				01001: State 9	10100: State 20	11111: State 31					
				01010: State 10	10101: State 21						
0x0001	SPARE	7:0	SPARE			0x00	N/A	No	0 - 2	R/W
0x001A	RFFE_STATUS	7	SOFTWARE RESET	Setting this bit initiates a software reset **Note:** On software reset, this register and all configurable registers are reset except for USID, GSID, and PM_TRIG. This bit will always read as 0.		0	N/A	No	No	W
		6	COMMAND_FRAME_PARITY_ER	Command Frame received with a parity error		0	N/A	No	No	R/W
		5	COMMAND_LENGTH_ERR	Command Sequence received with an incorrect length		0	N/A	No	No	R/W
		4	ADDRESS_FRAME_PARITY_ERR	Address Frame received with a parity error		0	N/A	No	No	R/W
		3	DATA_FRAME_PARITY_ERR	Data Frame received with a parity error		0	N/A	No	No	R/W
		2	READ_UNUSED_REG	Read Command Sequence received with an invalid address		0	N/A	No	No	R/W
		1	WRITE_UNUSED_REG	Write Command Sequence received with an invalid address		0	N/A	No	No	R/W
		0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID **Note:** Reading this register resets this register.		0	N/A	No	No	R/W
0x001B	GROUP_SID	7:4	RESERVED			0x0	N/A	No	No	R
		3:0	GSID[3:0]	Group Slave ID		0x0	N/A	No	No	R/W
0x001C	PM_TRIG	7:6	PWR_MODE[1:0]	00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: LOW POWER - Retain register values, Antenna in isolation 11: Reserved **Note:** Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.		0b00	N/A	B/G	No	R/W
		5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] **Note:** When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.		0b000	N/A	No	No	R/W
		2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers **Note:** When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.		0b000	N/A	B/G	No	W
0x001D	PRODUCT_ID	7:0	PRODUCT_ID[7:0]	Product Number **Note:** This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.8.3 for details.		0x60	N/A	No	No	R
0x001E	MANUFACTURER_ID	7:0	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI Manufacturer ID **Note:** This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.8.3 for details.		0x34	N/A	No	No	R
0x001F	MAN_USID	7:6	RESERVED			0b00	N/A	No	No	R
		5:4	MANUFACTURER_ID[9:8]	Upper two bits of MIPI Manufacturer ID **Note:** This is a read-only field. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this field, but does not update it. See MIPI 6.8.3 for details.		0b01	N/A	No	No	R
		3:0	USID[3:0]	Programmable Unique Slave ID The default value at reset is selected via pin ID0. ID0 = 0 → USID = 0b0110 ID0 = 1 → USID = 0b0111 **Note:** USID is only writeable using a special programming sequence. See MIPI 6.8.3 for details.		0x7	N/A	No	No	R/W
0x0021	VERSION_ID	7:0	VERSION_ID[7:0]	CMOS Version ID **Note:** The VERSION_ID register contains this product's version number which is set by RFMD according to manufacture date. The value may change throughout the product life cycle.		0x00	N/A	No	No	R

Pin Configuration

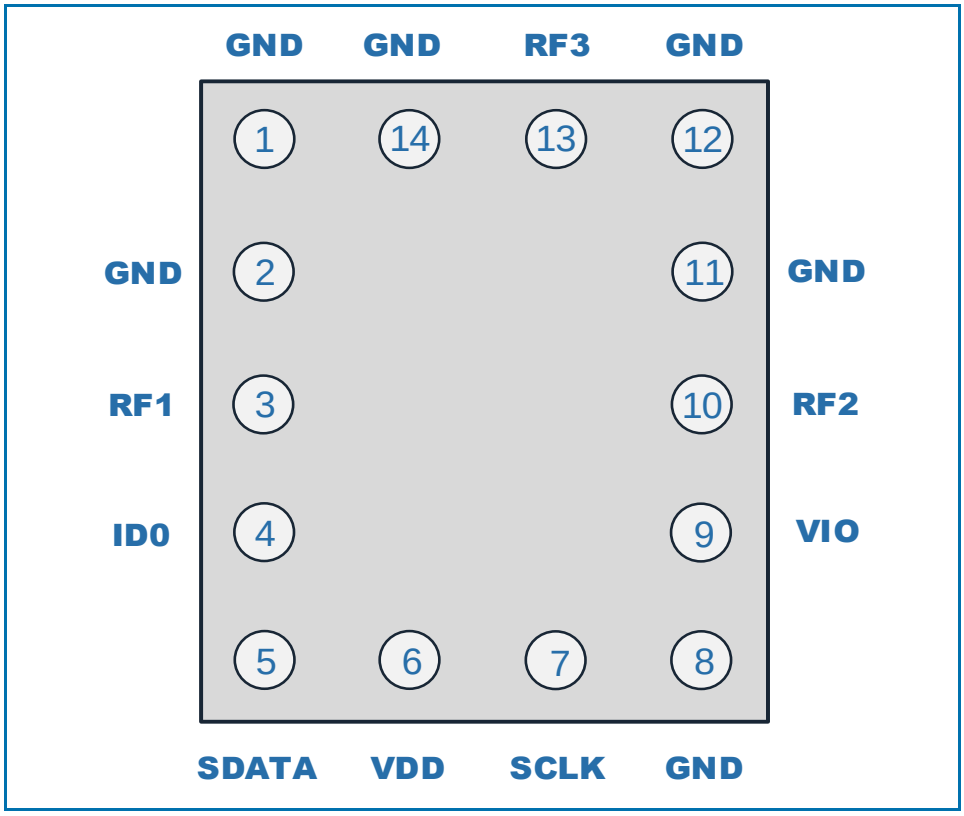


Figure 2.

Pin Names and Descriptions

Pin #	Pin Name	Description
1	GND	Ground
2	GND	Ground
3	RF1	RF Port 1
4	ID0	USID0 Control Input
5	SDATA	Serial Data Input
6	VDD	DC Power Supply
7	SCLK	Serial Clock Input
8	GND	Ground
9	VIO	Logic power supply
10	RF2	RF Port 2
11	GND	Ground
12	GND	Ground
13	RF3	RF Port 3
14	GND	Ground

Evaluation Board Schematic

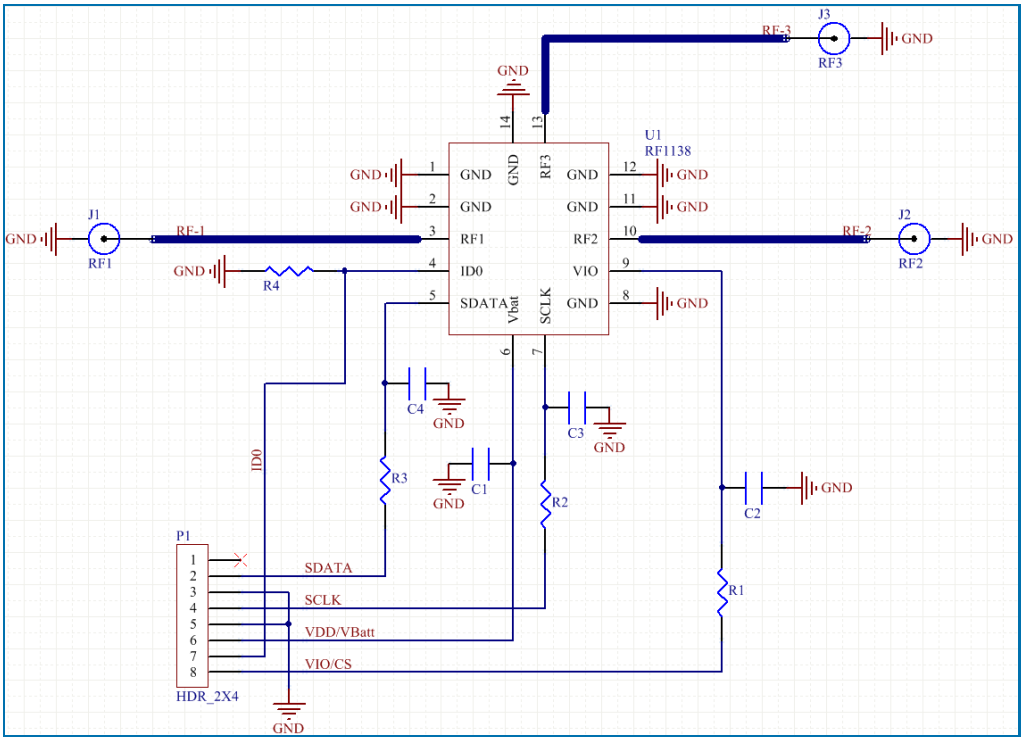


Figure 3.

Parts List

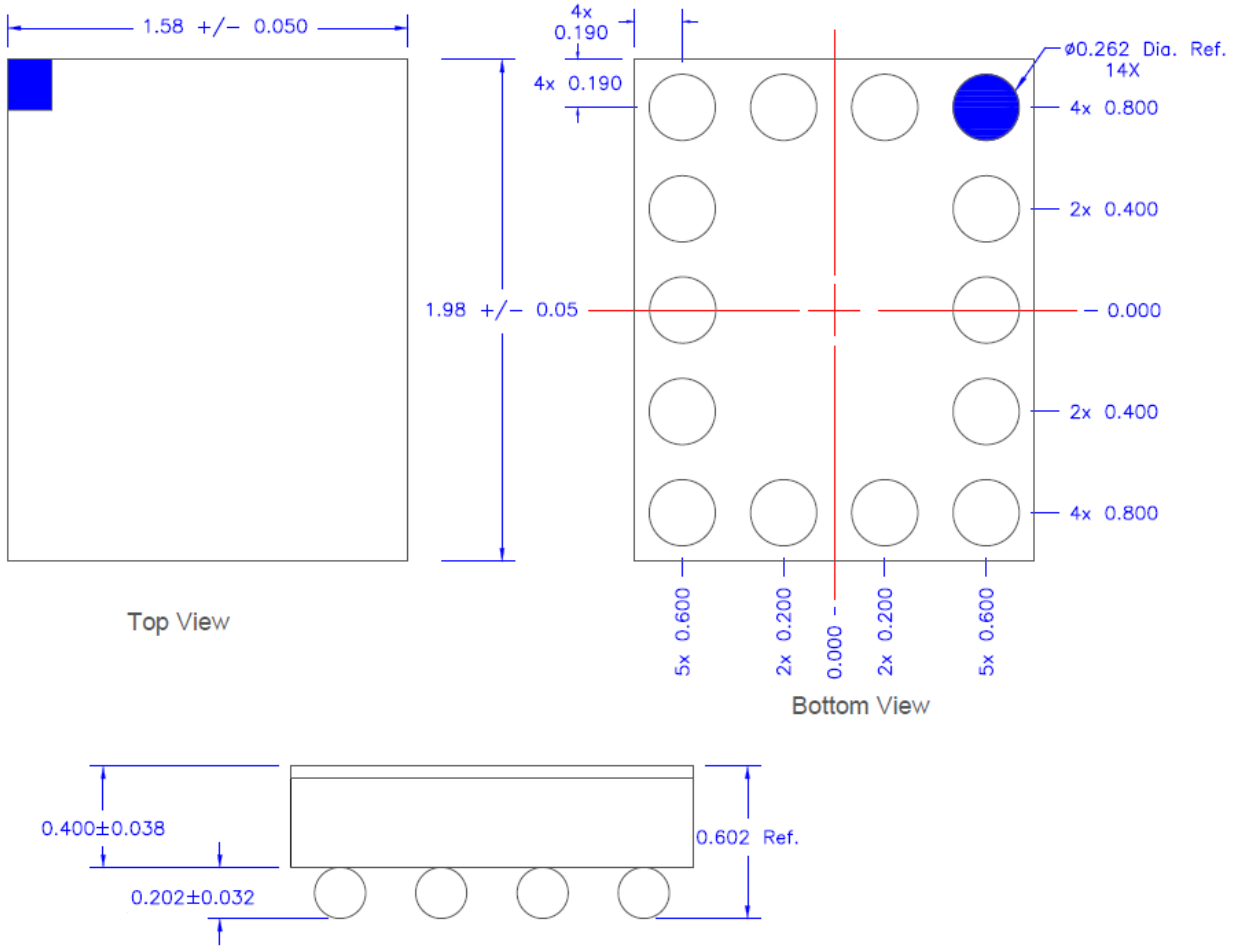
Part Number	Part	Part Description
U1	RF1138	RF1138, 0.6-8.8 pF 5-bit PAC with Switch
J1, J2 & J3	SMA connector	Edge mount 0.068” SMA connector
C1 & C2	100 pF capacitor	(0402) 100 pF de-coupling capacitor
C3 & C4	NP	No placement
R1, R2 & R3	0Ω jumper	(0402) 0Ω resistor
R4	NP or 0Ω jumper	No placement or (0201) 0Ω resistor
P1	2X4 RA header	2X4 right angled header with 0.1” spacing

Application Guidelines

Decoupling Capacitors = Decoupling capacitor on V_{DD} may be used for noise reduction. The value of the de-coupling capacitor should be selected based on the application.

DC Blocking Capacitors = DC blocking capacitor is not required on an RF port if no DC voltage exists on that port.

Package Outline and Branding Drawing (Dimensions in millimeters)



Note:

1. Shaded area represents Pin 1 location.
2. UBM size = 0.220

Figure 4.

Evaluation Board Layout

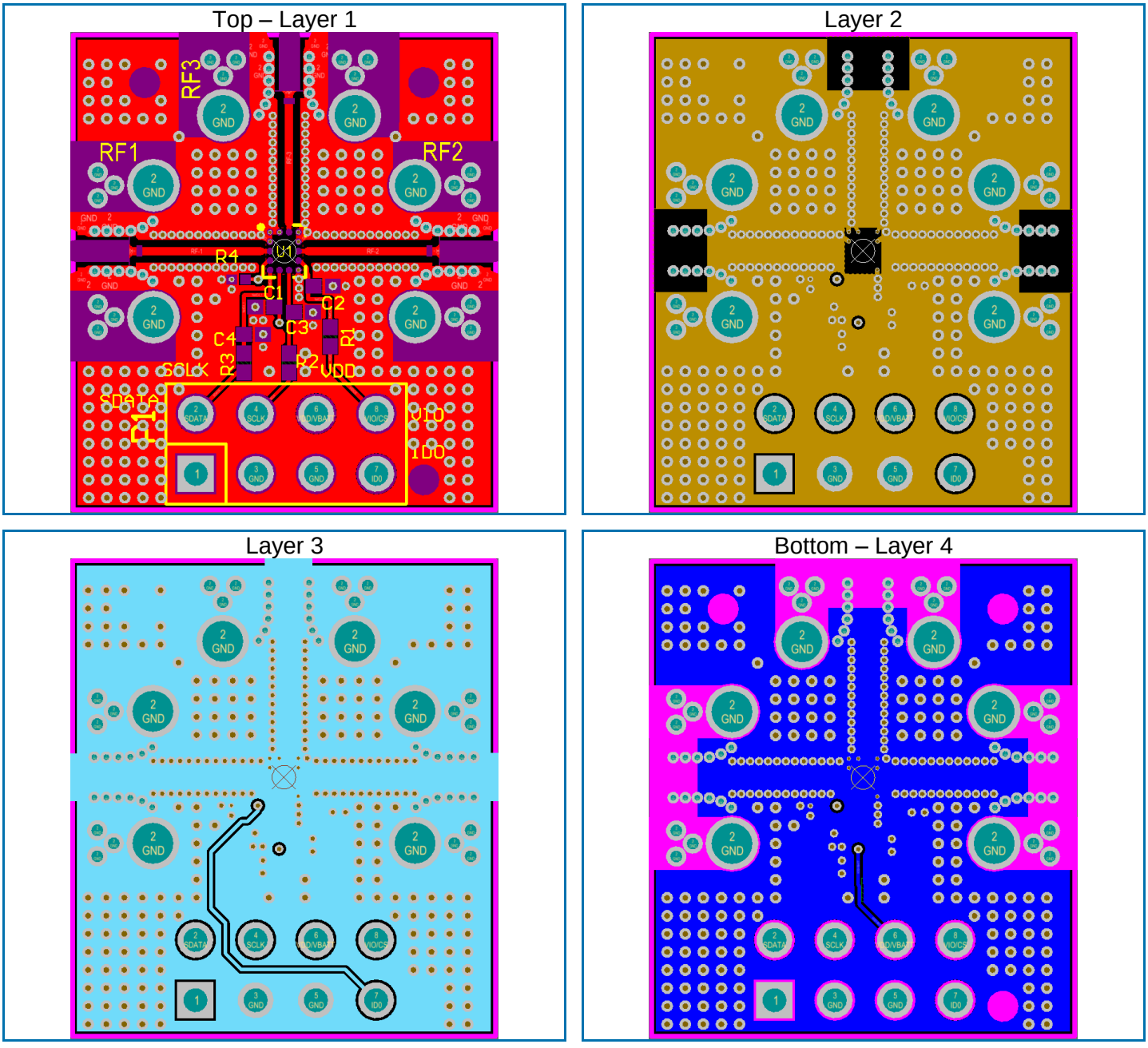


Figure 5.

EVB Layer Information

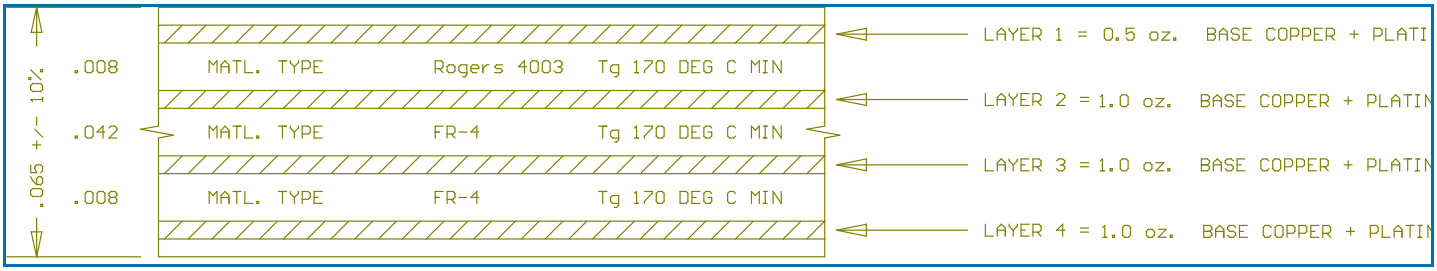


Figure 6.

PCB Design Requirements

PCB Metal Land Pattern

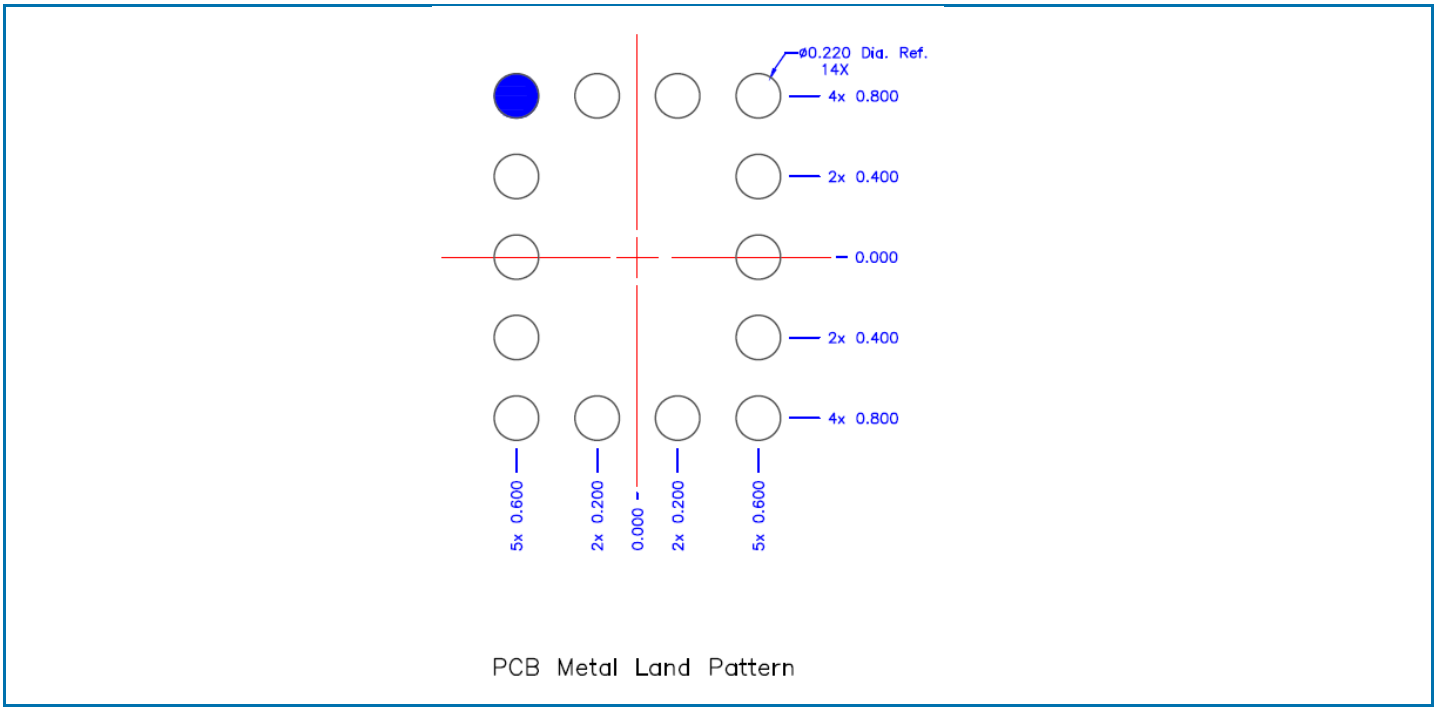


Figure 7.

PCB Solder Mask Pattern

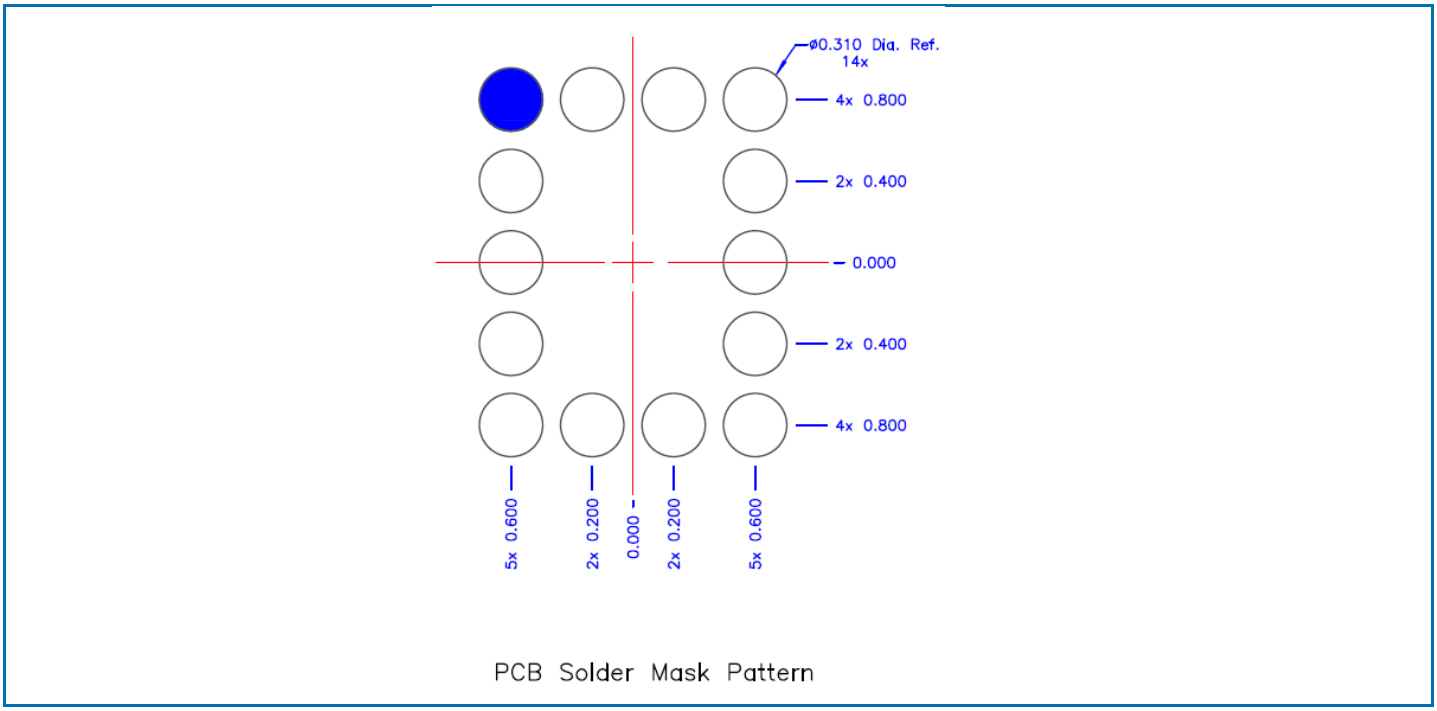


Figure 8.

PCB Stencil Pattern

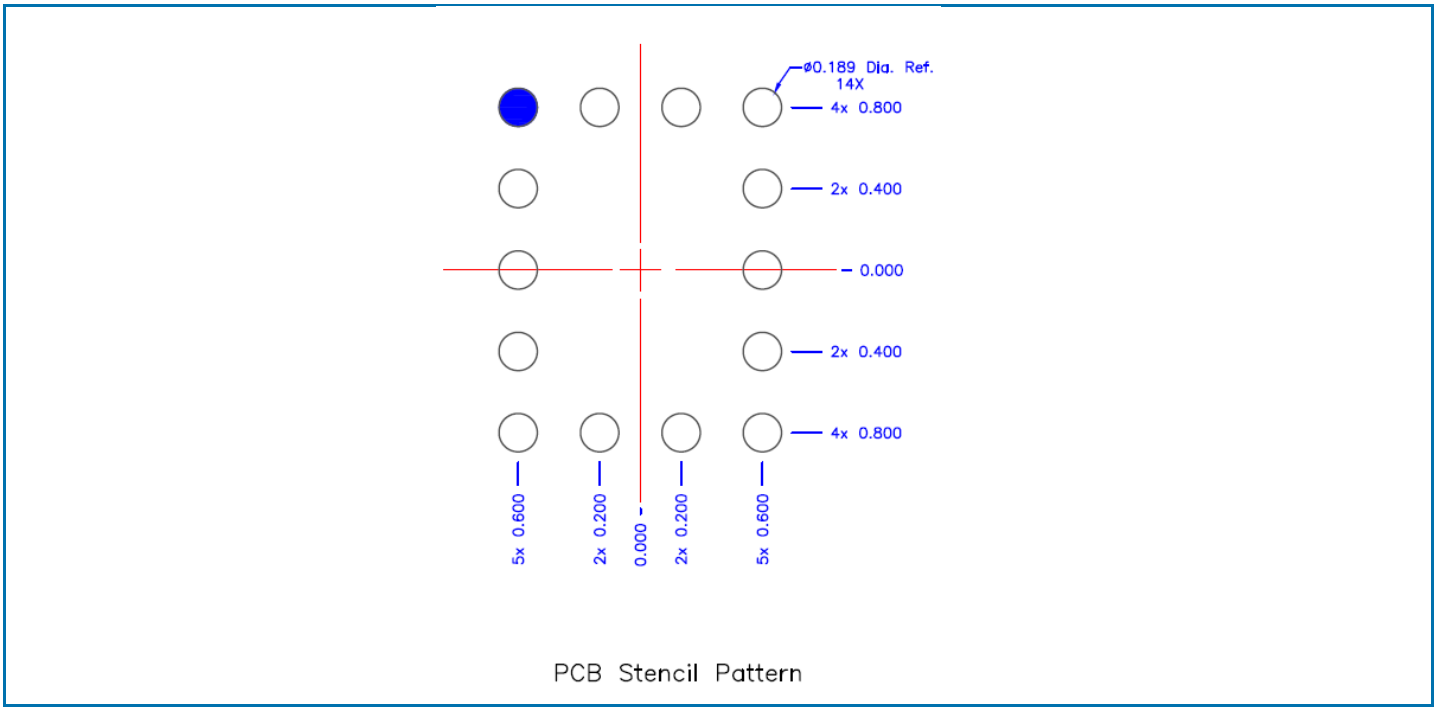


Figure 9.

Timing Diagram

Power ON and OFF sequence

It is very important that the user adheres to the correct power-on/off sequence in order to avoid damaging the device.

Power ON –

1) Apply voltage supply - V_{DD}
2) Apply logic supply - V_{IO}
3) Wait 10µs or greater and then apply RFFE bus signal - SCLK and SDATA
4) Wait 5µs or greater after RFFE bus goes idle and then apply the RF Signal

Power OFF –

1) Remove the RF Signal
2) Remove RFFE bus – SCLK and SDATA
3) Remove logic supply - V_{IO}
4) Remove voltage supply - V_{DD}

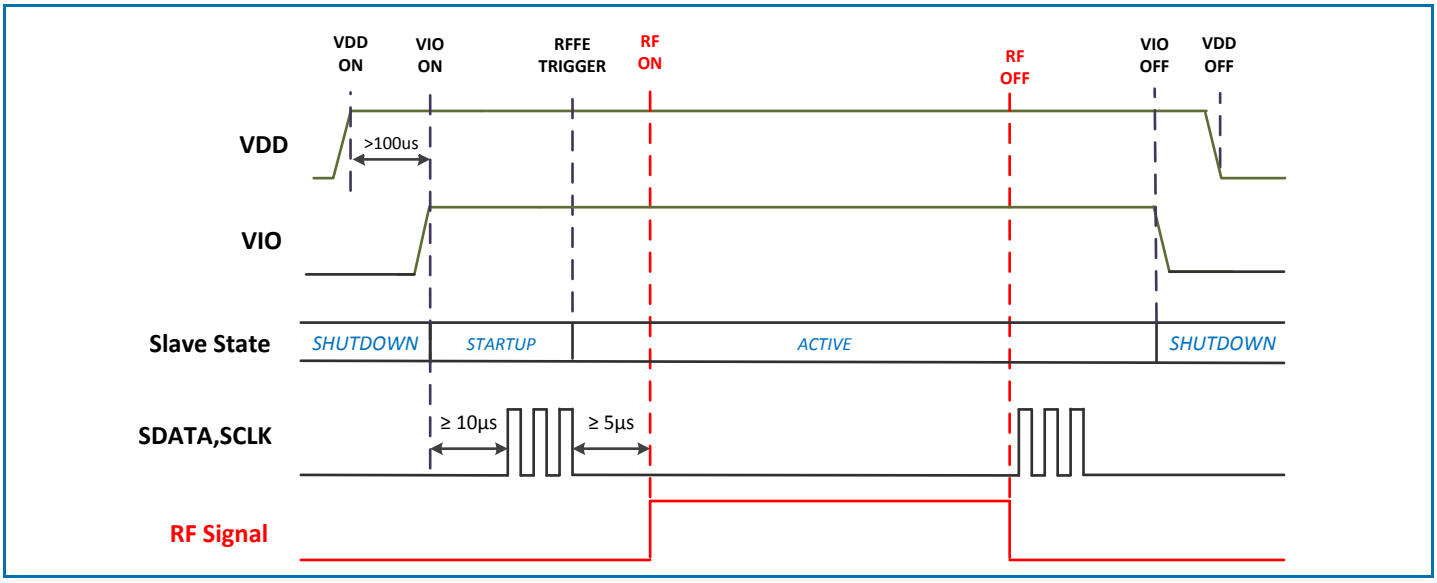


Figure 10.

Revision History

Revision Code	Comments
DS150316	First Draft
DS150317	Inserted Application Note on page 5
DS150318	Updated PID value
DS150327	Updated POD drawing and PID value
DS150624	Updated POD drawing with 60um street & harmonic testing PIN to 35dBm for all states and corresponding limits
DS151125	Updated tables on pgs 2 and 3
DS160212	Updated order information