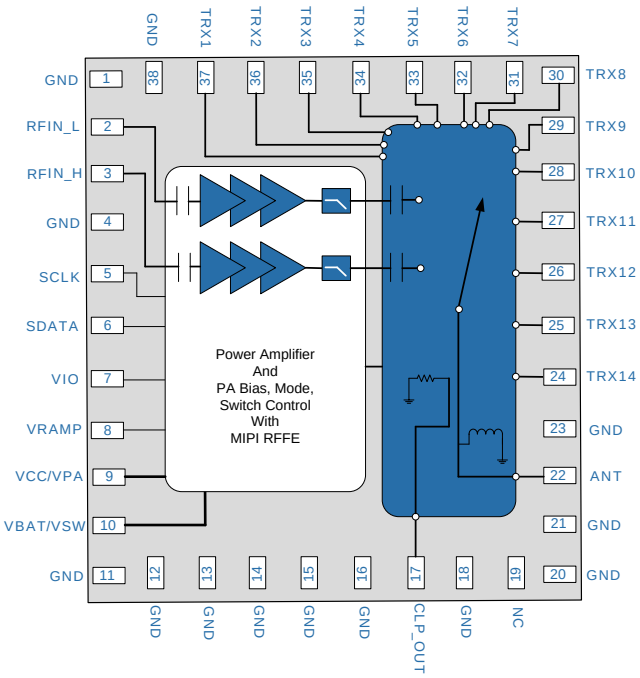
RF5216

Quad-Band GSM, Linear EDGE Transmit Module with Fourteen High Linearity TRX Switch Ports

The RF5216 is a quad-band GSM/GPRS, linear EDGE transmit module with fourteen transmit and receive RF switch ports using a MIPI RFFE interface for PA and switch controls. The power amplifier supports GSM and EDGE Class 12 transmit in the GSM850, GSM900, DCS1800, and PCS1900 bands. The fourteen switch ports are UMTS and LTE transmit and receive capable and may be used for GSM and EDGE receive ports.



Functional Block Diagram

Package: Module, 38-pin, 5.30mm x 5.50mm x 0.78mm

Features

- GSM and Linear EDGE Transmit
- Fourteen High Linearity TRX Ports
- MIPI RFFE Digital Control
- Low RF Switch Port Loss
- Few External Components Required
- 8kV ESD Protection in a Handset Application
- -1dBm to 6dBm Drive Level

Applications

- WEDGE Handsets and Connected Devices
- GSM and Linear EDGE Uplink Plus Multiband 3G and 4G

Ordering Information

RF5216PCK-410	Evaluation Board Sample Kit
RF5216SB	Sample bag with 5 pieces
RF5216TR7	7" Reel with 750 pieces
RF5216TR13-5K	13" Reel with 5000 pieces
RF5216DK	Design Kit, RF5216PCK-410+ RD2000 Communication Board

Basic MIPI RFFE Registers

MIPI Location	Bit Name	Default Value (hex)
Reg. 1D	Product_ID [7:0]	DD
Reg. 1E	Mfr_ID [7:0]	34
Reg. 1F	USID [3:0]	F

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DS20151001

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (VCC, VBATT)	-1.2 to 6.0	V
Control Voltage (VRAMP)	-0.3 to 3.0	V
Digital control signals, SCLK, SDATA, VIO	2.0	V
RF Input Power for 2G PA	10	dBm
RF Input Power for all TRX Ports	31	dBm
Transmit Duty Cycle, Period = 4.6ms	50	%
Output Load VSWR	20:1	
Operating Temperature Range	-30 to +85	°C
Storage Temperature Range	-55 to +150	°C
ESD Rating – Human Body Model (HBM, JESD22-A114)	1000	V
ESD Rating – Charged Device Model (CDM, JESD22-C101C)	500	V
Moisture Sensitivity Level	MSL3	

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Performance Specifications

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Requirements					**T_A = 25°C, unless otherwise specified**
Operating Ambient Temperature (T_A)	-30	25	85	°C	
Supply Voltage, VCC	3.0	3.5	4.6	V	Normal operating range
Supply Voltage, VBATT	2.8	3.5	4.6	V	Normal operating range
Supply Leakage Current			10	µA	
VRAMP Voltage		0.16		V	GSM transmit; minimum RF output power
			1.8	V	GSM transmit; maximum RF output power
	1.65		1.8	V	EDGE transmit
VRAMP Capacitance			10	pF	DC to 200kHz
VRAMP Current			10	µA	
Supply Voltage, VIO	1.65	1.8	2.0	V	MIPI RFFE supply voltage
MIPI RFFE logic low (SCLK, SDATA)	0		0.3*VIO	V	
MIPI RFFE logic high (SCLK, SDATA)	0.7*VIO		VIO	V	
VIO Rise Time			450	µs	Required for device reset
Control Current (MIPI Digital Inputs)			50	µA	
Turn-on Time			20	µs	From application of VBATT and VIO
Switching Speed		2	5	µs	Port to Port
RF Port Impedance		50		Ω	Pins 2, 3, 17, 22, 24 to 37

Parameter		Specification			Unit	Condition
		Min	Typ	Max		
Transmit, GSM, Low Band						**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; VCC=VBATT=3.5V; P_{IN}=3dBm; T_A=+25°C; VRAMP=1.8V; Duty Cycle=25%; Period=4.6ms.**
Frequency		824		849	MHz	GSM800 Band
		880		915	MHz	GSM900 Band
Input Power (P_{IN})		-1	3	6	dBm	
Input VSWR				2.5	X:1	5dBm ≤ P_{OUT} ≤ 33dBm
RF Output Power (P_{OUT}), Maximum		33	34.3		dBm	
		31			dBm	VCC=3.0V to 4.6V; P_{IN}=-1dBm to 6dBm; T_A=-30°C to +85°C
RF Output Power Delivered, VSWR 3:1		30.0			dBm	Load VSWR=3:1; all phase angles; VRAMP adjusted for P_{OUT}=33dBm into 50Ω load
Efficiency (PAE), 33.0dBm	824-849MHz		41		%	VRAMP adjusted for P_{OUT}=33dBm
	880-915MHz		39			
Peak Supply Current, 33.0dBm	824-849MHz		1400		mA	
	880-915MHz		1450		mA	
Harmonic Peak, 2fo			-40	-33	dBm	
Harmonic Peak, 3fo			-40	-33	dBm	
Harmonic Peak, 4fo to 12.75GHz			-40	-33	dBm	
Non-Harmonic Spurious up to 12.75GHz			-40	-36	dBm	5dBm ≤ P_{OUT} ≤ 33dBm
Forward Isolation, PA OFF			-52		dBm	P_{IN}=6dBm; VRAMP=0.16V
Noise Power 736MHz to 757MHz				-83	dBm	VRAMP adjusted for P_{OUT}=33dBm; RBW=100kHz
Noise Power 757MHz to 763MHz				-80	dBm	
Noise Power 869MHz to 894MHz				-88	dBm	
Noise Power 925MHz to 935MHz				-83	dBm	
Noise Power 935MHz to 960MHz				-87	dBm	
Noise Power 1805MHz to 1880MHz				-90	dBm	
Noise Power 1930MHz to 1990MHz				-90	dBm	
Stability (Spurious), VSWR 10:1				-36	dBm	VSWR=10:1; all phase angles; VRAMP adjusted for P_{OUT}=33dBm into 50Ω load; VCC=3.0V to 4.6V; P_{IN}=-1dBm to 6dBm; T_A=-30°C to +85°C; RBW=3MHz
Ruggedness, VSWR 20:1		No damage or permanent degradation to device				VSWR=20:1; all phase angles; VRAMP adjusted for P_{OUT}=33dBm into 50Ω load; VCC=3.0V to 4.6V; P_{IN}=-1dBm to 6dBm; T_A=-30°C to +85°C

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Transmit, EDGE, Low Band					**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; VCC=VBATT=3.5V; P_{OUT}=27.5dBm; T_A=+25°C; Duty Cycle=25%; Period=4.6ms.**
Frequency	824		849	MHz	GSM800 Band
	880		915	MHz	GSM900 Band
Input VSWR			2.5	X:1	
Linear Output Power (P_{OUT})	27.5	28		dBm	
	26			dBm	VCC=3.2V to 4.6V; T_A=-30°C to +85°C
Gain	30	32	34	dB	
Peak Supply Current		775		mA	
Efficiency (PAE)		20		%	
Modulation Spectrum 200kHz offset			-33	dBc	P_{OUT}=27.5dBm
Modulation Spectrum 400kHz offset			-58	dBc	
Modulation Spectrum 600kHz offset			-65	dBc	
EVM Peak			12	%	
EVM RMS		3	5	%	
Noise Power 736MHz to 757MHz			-83	dBm	5dBm ≤ P_{OUT} ≤ 27.5dBm; RBW=100kHz
Noise Power 757MHz to 763MHz			-80	dBm	
Noise Power 869MHz to 894MHz			-83	dBm	
Noise Power 925MHz to 935MHz			-80	dBm	
Noise Power 935MHz to 960MHz			-83	dBm	
Noise Power 1805MHz to 1880MHz			-90	dBm	
Noise Power 1930MHz to 1990MHz			-90	dBm	
Stability (Spurious), VSWR 10:1			-36	dBm	VSWR=10:1; all phase angles; P_{IN} adjusted for P_{OUT}=27.5 dBm into 50Ω load.

Parameter		Specification			Unit	Condition
		Min	Typ	Max		
Transmit, GSM, High Band						**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; VCC=VBATT=3.5V; P_{IN}=3dBm; T_A=+25°C; VRAMP=1.8V; Duty Cycle=25%; Period=4.6ms.**
Frequency		1710		1785	MHz	DCS1800 Band
		1850		1910	MHz	PCS1900 Band
Input Power (P_{IN})		-1	3	6	dBm	
Input VSWR				2.5	X:1	0dBm ≤ P_{OUT} ≤ 31dBm
RF Output Power (P_{OUT}), Maximum		31	32		dBm	
		28.5			dBm	VCC=3.0V to 4.6V; P_{IN}=-1dBm to 6dBm; T_A=-30°C to +85°C
RF Output Power Delivered, VSWR 3:1		27.5			dBm	Load VSWR=3:1; all phase angles; VRAMP adjusted for P_{OUT}=31dBm into 50Ω load
Efficiency (PAE), 31.0dBm	1710-1785MHz		34		%	VRAMP adjusted for P_{OUT}=31dBm
	1850-1910MHz		32			
Peak Supply Current, 31.0dBm	1710-1785MHz		1060		mA	
	1850-1910MHz		1120		mA	
Harmonic Peak, 2fo			-40	-33	dBm	
Harmonic Peak, 3fo			-40	-33	dBm	
Harmonic Peak, 4fo to 12.75GHz			-40	-33	dBm	
Non-Harmonic Spurious up to 12.75GHz			-40	-36	dBm	0dBm ≤ P_{OUT} ≤ 31dBm
Forward Isolation, PA OFF			-50		dBm	P_{IN}=6dBm; VRAMP=0.16V
Noise Power 736MHz to 757MHz				-83	dBm	VRAMP adjusted for P_{OUT}=31dBm; RBW=100kHz
Noise Power 757MHz to 763MHz				-82	dBm	
Noise Power 869MHz to 894MHz				-95	dBm	
Noise Power 925MHz to 935MHz				-95	dBm	
Noise Power 935MHz to 960MHz				-95	dBm	
Noise Power 1805MHz to 1880MHz				-90	dBm	
Noise Power 1930MHz to 1990MHz				-91	dBm	
Stability (Spurious), VSWR 10:1				-36	dBm	VSWR=10:1; all phase angles; VRAMP adjusted for P_{OUT}=31dBm into 50Ω load; VCC=3.0V to 4.6V; P_{IN}=-1dBm to 6dBm; T_A=-30°C to +85°C; RBW=3MHz
Ruggedness, VSWR 20:1		No damage or permanent degradation to device				VSWR=20:1; all phase angles; VRAMP adjusted for P_{OUT}=31dBm into 50Ω load; VCC=3.0V to 4.6V; P_{IN}=-1dBm to 6dBm; T_A=-30°C to +85°C

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Transmit, EDGE, High Band					**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; VCC=VBATT=3.5V; P_{OUT}=26.5dBm; T_A=+25°C; Duty Cycle=25%; Period=4.6ms.**
Frequency	1710		1785	MHz	DCS1800 Band
	1850		1910	MHz	PCS1900 Band
Input VSWR			2.5	X:1	
Linear Output Power (P_{OUT})	26.5	27		dBm	
	25			dBm	VCC=3.2V to 4.6V; T_A=-30°C to +85°C
Gain	30.5	33	34.5	dB	
Peak Supply Current		680		mA	
Efficiency (PAE)		18		%	
Modulation Spectrum 200kHz offset			-33	dBc	P_{OUT}=26.5dBm
Modulation Spectrum 400kHz offset			-58	dBc	
Modulation Spectrum 600kHz offset			-65	dBc	
EVM Peak			12	%	
EVM RMS		3	5	%	
Noise Power 736MHz to 757MHz			-83	dBm	0dBm ≤ P_{OUT} ≤ 26.5dBm; RBW=100kHz
Noise Power 757MHz to 763MHz			-81	dBm	
Noise Power 869MHz to 894MHz			-90	dBm	
Noise Power 925MHz to 935MHz			-90	dBm	
Noise Power 935MHz to 960MHz			-90	dBm	
Noise Power 1805MHz to 1880MHz			-83	dBm	
Noise Power 1930MHz to 1990MHz			-85	dBm	
Stability (Spurious), VSWR 10:1			-36	dBm	VSWR=10:1; all phase angles; P_{IN} adjusted for P_{OUT}=26.5dBm into 50Ω load.

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Switch, Low Bands TRX					**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; Logic State given in condition; VBATT=3.5V; P_{IN}=-6dBm; T_A=+25°C, Duty Cycle=100%.**
Frequency	699		1000	MHz	
Insertion Loss, TRXn - ANT		0.8		dB	Any TRX port except TRX3, TRX4, TRX5, TRX8, TRX9
Input VSWR, TRXn - ANT	1.0	-	1.5	X:1	
Isolation, Any TRX Port	35			dB	from active TRX to any off TRX
Isolation, Any TRX Port	26			dB	from active TRX to any off TRX (adjacent ports)
IMD2, Any TRX Port			-105	dBm	TX=+20dBm, Blocker=-15dBm
IMD3, Any TRX Port			-105	dBm	TX=+20dBm, Blocker=-15dBm
Harmonic, 2fo			-55	dBm	Input Power=27dBm
Harmonic, 3fo			-55	dBm	
Harmonics, B13 2fo			-69	dBm	Freq = 787 MHz, Input Power=25dBm
Triple Beat Ratio	81	85		dBc	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Switch, Mid Bands TRX					**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; Logic State given in condition; VBATT=3.5V; P_{IN}=-6dBm; T_A=+25°C; Duty Cycle=100%.**
Frequency	1420		2300	MHz	
Insertion Loss, TRXn - ANT		1.3		dB	Any TRX port except TRX3, TRX4, TRX5, TRX8, TRX9
Input VSWR, TRXn - ANT	1.0	-	1.5	X:1	
Isolation, Any TRX Port	30			dB	from active TRX to any off TRX
Isolation, Any TRX Port	23			dB	from active TRX to any off TRX (adjacent ports)
IMD2, Any TRX Port			-105	dBm	TX=+20dBm, Blocker=-15dBm
IMD3, Any TRX Port			-105	dBm	TX=+20dBm, Blocker=-15dBm
Harmonic, 2fo			-55	dBm	Input Power=27dBm
Harmonic, 3fo			-55	dBm	
Triple Beat Ratio	81	85		dBc	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Switch, High Bands (ULL-TRX)					**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; Logic State given in condition; VBATT=3.5V; P_{IN}=-6dBm; T_A=+25°C; Duty Cycle=100%.**
Frequency	2300		2690	MHz	
Insertion Loss, TRXn - ANT		1.1		dB	TRX3, TRX4, TRX5, TRX8, TRX9 (See note 1)
Input VSWR, TRXn - ANT	1.0	-	1.5	X:1	
Isolation, Any ULL-TRX Port	25			dB	from active ULL-TRX to any off TRX
Isolation, TRX4 and TRX5	25			dB	from active TRX4 or TRX5 to any off TRX (adjacent ports)
Isolation, Any Other ULL-TRX Port	20			dB	from active ULL-TRX to any off TRX (adjacent ports)
IMD2, Any ULL-TRX Port			-105	dBm	TX=+20dBm, Blocker=-15dBm
IMD3, Any ULL-TRX Port			-105	dBm	TX=+20dBm, Blocker=-15dBm
IMD3, TRX8			-95	dBm	TX (2550MHz) =+24dBm, Blocker (2430MHz) =+2dBm
Harmonic, 2fo			-55	dBm	Input Power=27dBm
Harmonic, 3fo			-55	dBm	
Triple Beat Ratio	81	85		dBc	

Note 1: For optimal Insertion Loss on ULL ports, Input Matching Return Loss must be greater than -20 dB.

Parameter		Specification			Unit	Condition
		Min	Typ	Max		
Directional Coupler						**Nominal test conditions unless otherwise stated; All unused ports terminated in 50Ω; Logic State given in condition; VBATT=3.5V; P_{IN}=-6dBm; T_A=+25°C; Duty Cycle=100%.**
Frequency		699		2690	MHz	
Coupling Factor	699-1300MHz		20-24		dB	At CPL_OUT over temperature and frequency (internally CPL_IN terminated with 50Ω)
	1700-2300MHz		20-24			
	2300-2700MHz		26-28			
(CPL_OUT/P_OUT) power ratio variation over output VSWR			±0.50		dB	2.5:1 VSWR at PA output all phases, -30°C≤T_A ≤+85°C
Coupler Directivity			20		dB	Refer to Pin Names and Descriptions on page 29.
Coupler Impedance			50		Ω	

MIPI RFFE Control Register Logic Tables

Register 00h (00000b): Module Control Logic Definitions

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg00[7:3]	RF_MODE_CTRL	00000	0 0 0 0 0 : Sleep All circuits off 0 0 0 0 1 : TRX1 to ANT path is active. Power amplifier is off. 0 0 0 1 0 : TRX2 to ANT path is active. Power amplifier is off. 0 0 0 1 1 : TRX3 to ANT path is active. Power amplifier is off. 0 0 1 0 0 : TRX4 to ANT path is active. Power amplifier is off. 0 0 1 0 1 : TRX5 to ANT path is active. Power amplifier is off. 0 0 1 1 0 : TRX6 to ANT path is active. Power amplifier is off. 0 0 1 1 1 : TRX7 to ANT path is active. Power amplifier is off. 0 1 0 0 0 : TRX8 to ANT path is active. Power amplifier is off. 0 1 0 0 1 : TRX9 to ANT path is active. Power amplifier is off. 0 1 0 1 0 : TRX10 to ANT path is active. Power amplifier is off. 0 1 0 1 1 : TRX11 to ANT path is active. Power amplifier is off. 0 1 1 0 0 : TRX12 to ANT path is active. Power amplifier is off. 0 1 1 0 1 : TRX13 to ANT path is active. Power amplifier is off. 0 1 1 1 0 : TRX14 to ANT path is active. Power amplifier is off. 1 0 0 0 0 : TX_LB_GSM Low Band power amplifier active, Saturated mode (VRAMP power control). 1 0 0 0 1 : TX_HB_GSM High Band power amplifier active, Saturated mode (VRAMP power control). 1 0 0 1 0 : TX_LB_EDGE Low Band power amplifier active, Linear mode (RFIN power control). 1 0 1 0 0 : TX_HB_EDGE High Band power amplifier active, Linear mode (RFIN power control). All other settings : Sleep All circuits off.	R/W	N	T012
Reg00[2]	ENABLE	0	1: PA and/or switch enabled depending on RF_MODE_CTRL 0: PA and switch power supplies disabled; low-power mode	R/W	N	T012
Reg00[1:0]	FREQ	00	Frequency control of the switch and coupler. 11: HB 10: MB 01: LB 00: Coupler Off	R/W	N	T012

Register 1Ah (11010b) – RFFE Status

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg1A[7]	SOFTWARE RESET	0	Setting this bit initiates a software reset Note: On software reset, this register and all configurable registers are reset except for USID, GSID, and PM_TRIG. This bit will always read as 0.	R/W	N	N
Reg1A[6]	COMMAND_FRAME_PARITY_ERR	0	Command sequence received with parity error – discard command	R/W	N	N
Reg1A[5]	COMMAND_LENGTH_ERR	0	Command Sequence received with an incorrect length	R/W	N	N
Reg1A[4]	ADDRESS_FRAME_PARITY_ERR	0	Address Frame received with a parity error	R/W	N	N

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg1A[3]	DATA_FRAME_PARITY_ERR	0	Data Frame received with a parity error	R/W	N	N
Reg1A[2]	READ_UNUSED_REG	0	Read Command Sequence received with an invalid address	R/W	N	N
Reg1A[1]	WRITE_UNUSED_REG	0	Write Command Sequence received with an invalid address	R/W	N	N
Reg1A[0]	BID_GID_ERR	0	Read Command Sequence received with a BROADCAST_ID or GROUP_SID.	R/W	N	N

Register 1Bh (11011b) – Group Slave ID

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg1B[7:4]	RESERVED	0000	Reserved	R	N	N
Reg1B[3:0]	GSID[3:0]	0000	Group Slave ID	R/W	N	N

Register 1Ch (11100b) – Power Mode Trigger

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg1C[7:6]	PWR_MODE[7:6]	00	00: ACTIVE – Normal Operation 01: STARTUP – Reset all registers to default settings 10: LOW POWER – Retain register values, Band-Gap off 11: Reserved Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.	R/W	Y	N
Reg1C[5]	Trigger_Mask_2	0	If this bit is set, trigger 2 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 2, the data goes directly to the destination register.	R/W	N	N
Reg1C[4]	Trigger_Mask_1	0	If this bit is set, trigger 1 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 1, the data goes directly to the destination register.	R/W	N	N
Reg1C[3]	Trigger_Mask_0	0	If this bit is set, trigger 0 is disabled. When all triggers are disabled, if writing to a register that is associated with trigger 0, the data goes directly to the destination register.	R/W	N	N
Reg1C[2]	Trigger_2	0	A write of a 1 to this bit loads trigger 2's registers.	R/W	Y	N
Reg1C[1]	Trigger_1	0	A write of a 1 to this bit loads trigger 1's registers.	R/W	Y	N
Reg1C[0]	Trigger_0	0	A write of a 1 to this bit loads trigger 0's registers.	R/W	Y	N

Register 1Dh (11101b) – Product ID

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg1D[7:0]	PRODUCT_ID[7:0]	DDh	Read only. During programming of USID, a write command sequence is performed on this register but does not change its value.	R	N	N

Register 1Eh (11110b) – Manufacturer ID

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg1E[7:0]	MANUFACTURER_ID[7:0]	34h	Read only. During programming of USID, a write command sequence is performed on this register but does not change its value.	R	N	N

Register 1Fh (11111b) – Manufacturer ID and USID

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg1F[7:6]	RESERVED	00	Reserved	R	N	N
Reg1F[5:4]	MANUFACTURER_ID[9:8]	01	Read only. During programming of USID, a write command sequence is performed on this register but does not change its value.	R	N	N
Reg1F[3:0]	USID[3:0]	1111	USID of the device = “PA Module 1”. Only writeable using the USID write sequence.	R/W	N	N

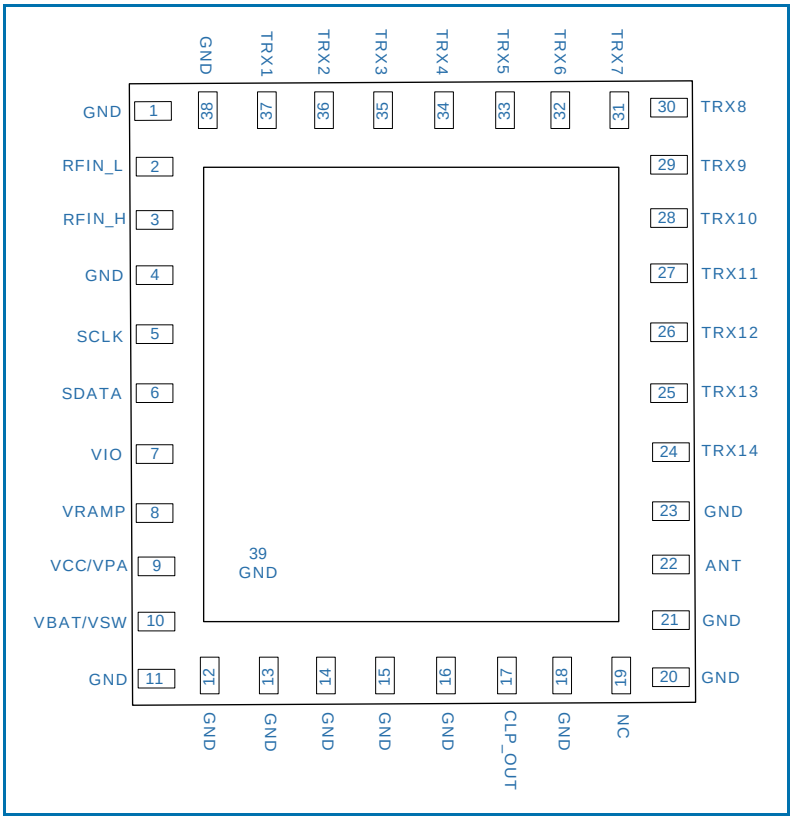
Register 21h (100001b) – CMOS Version ID

MIPI Location	Bit Name	Default	Description	R/W	Broadcast ID support	Trigger support
Reg21[7:0]	VERSION_ID[7:0]		CMOS version ID	R	N	N

Pin Names and Descriptions

Pin	Name	Description
1	GND	Pin connected to module ground.
2	RFIN_L	RF input to the GSM850/EGSM900 bands. This is a 50 Ω input.
3	RFIN_H	RF input to the DCS1800/PCS1900 bands. This is a 50Ω input.
4	GND	Pin connected to module ground.
5	SCLK	Serial interface clock input signal, an R/C filter of 100ohm/20pF is required for better noise performance.
6	SDATA	Serial interface data I/O signal.
7	VIO	Supply voltage for the MIPI RFFE serial interface.
8	VRAMP	Power control signal from DAC. A simple RC filter is integrated and may not require additional filtering depending on the baseband selected.
9	VCC	Main DC power supply for the power amplifier circuitry in the module. Traces running to this pin will have high current pulses during transmit operation. Proper decoupling and routing to handle this condition should be observed.
10	VBATT	Supply voltage for bias circuitry.
11,12,13,14,15,16	GND	Pin connected to module ground.
17	CPL_O	Coupler output port.
18	GND	Pin connected to module ground.
19	NC	Pin not connected.
20,21	GND	Pin connected to module ground.
22	ANT	Bidirectional RF port. This is the common port of the antenna switch. An inductor makes this port appear as a DC short to ground.
23	GND	Pin connected to module ground.
24	TRX14	External circuitry must maintain zero volts on this port.
25	TRX13	External circuitry must maintain zero volts on this port.
26	TRX12	External circuitry must maintain zero volts on this port.
27	TRX11	External circuitry must maintain zero volts on this port.
28	TRX10	External circuitry must maintain zero volts on this port.
29	TRX9	Recommended for High Bands (ULL-TRX). External circuitry must maintain zero volts on this port.
30	TRX8	Recommended for High Bands (ULL-TRX). External circuitry must maintain zero volts on this port.
31	TRX7	External circuitry must maintain zero volts on this port.
32	TRX6	External circuitry must maintain zero volts on this port.
33	TRX5	Recommended for High Bands (ULL-TRX). External circuitry must maintain zero volts on this port.
34	TRX4	Recommended for High Bands (ULL-TRX). External circuitry must maintain zero volts on this port.
35	TRX3	Recommended for High Bands (ULL-TRX). External circuitry must maintain zero volts on this port.
36	TRX2	External circuitry must maintain zero volts on this port.
37	TRX1	External circuitry must maintain zero volts on this port.
38	GND	Pin connected to module ground.
39	GND	Module ground pad

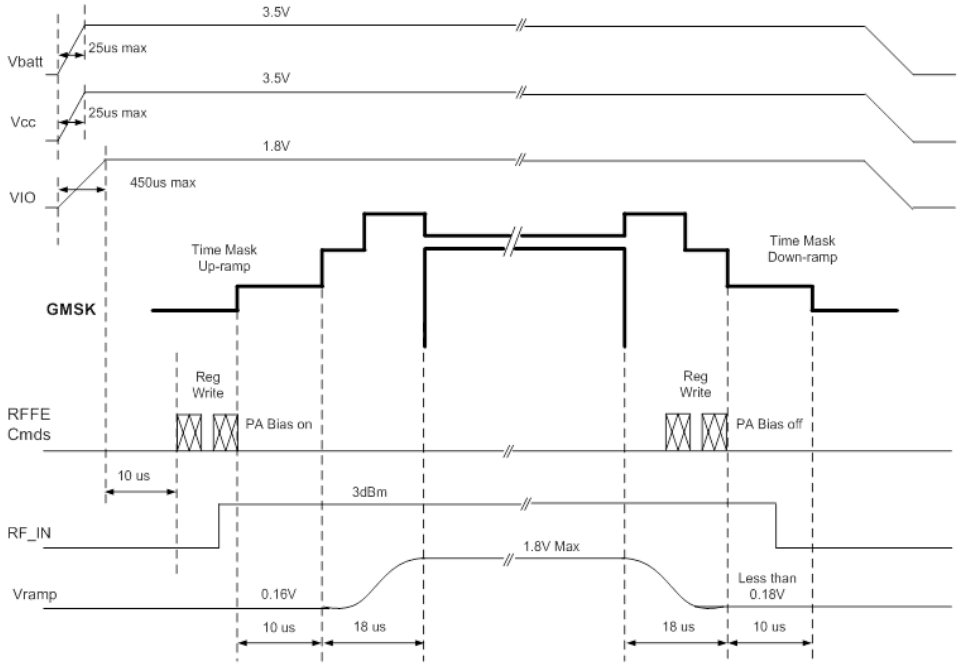
Pin Out



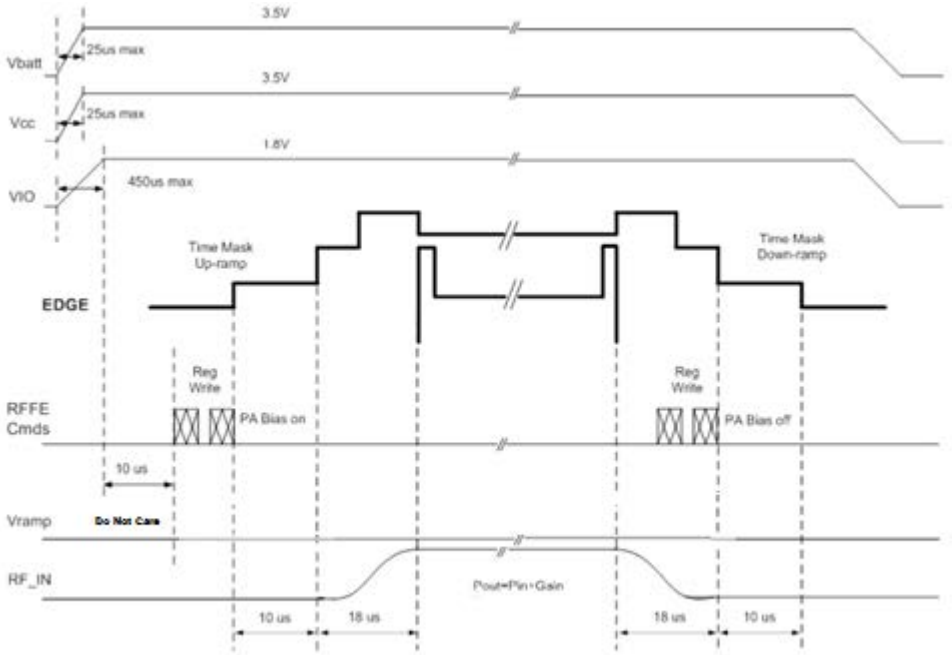
Timing Diagram

GSM Transmit

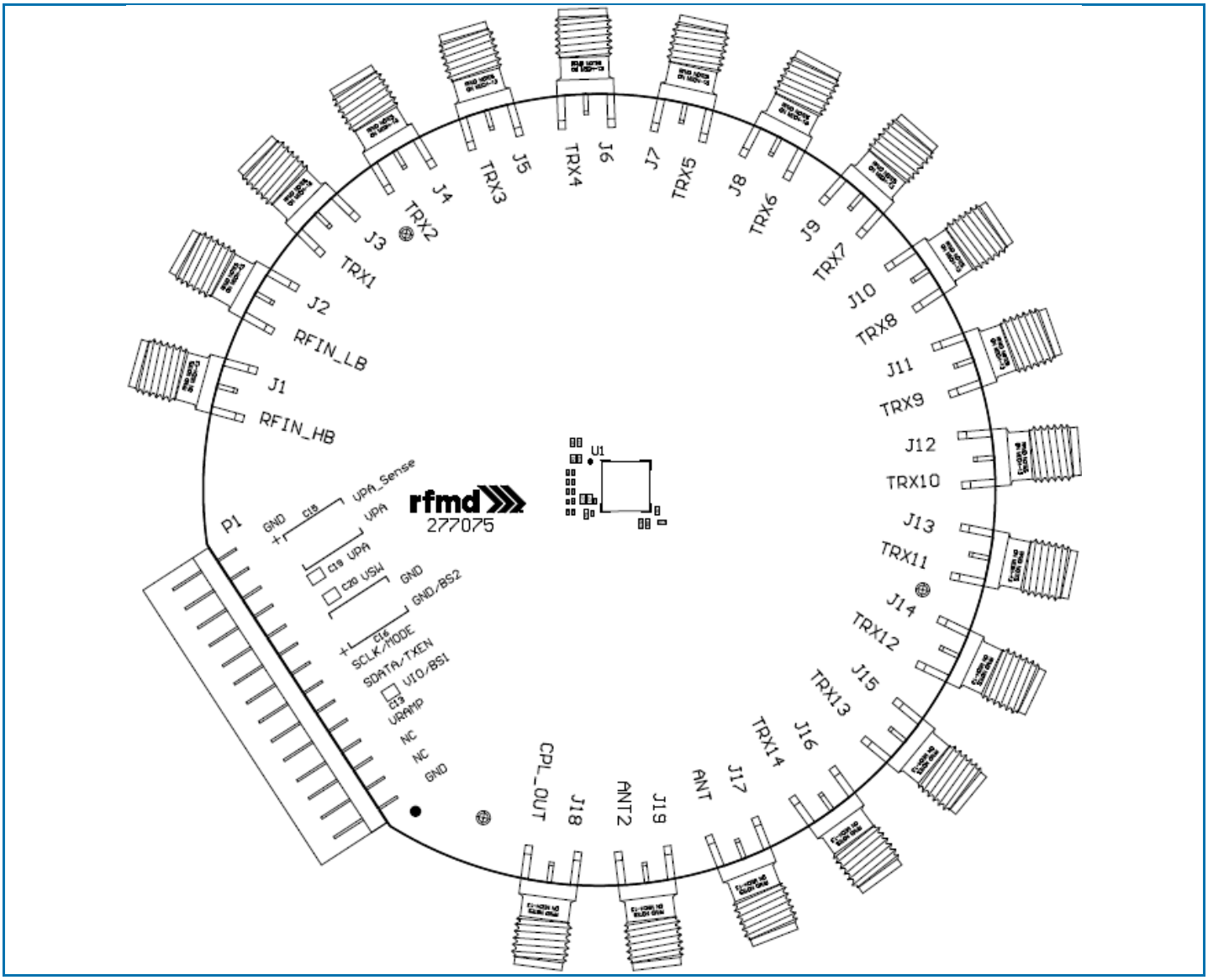
NOT TO SCALE



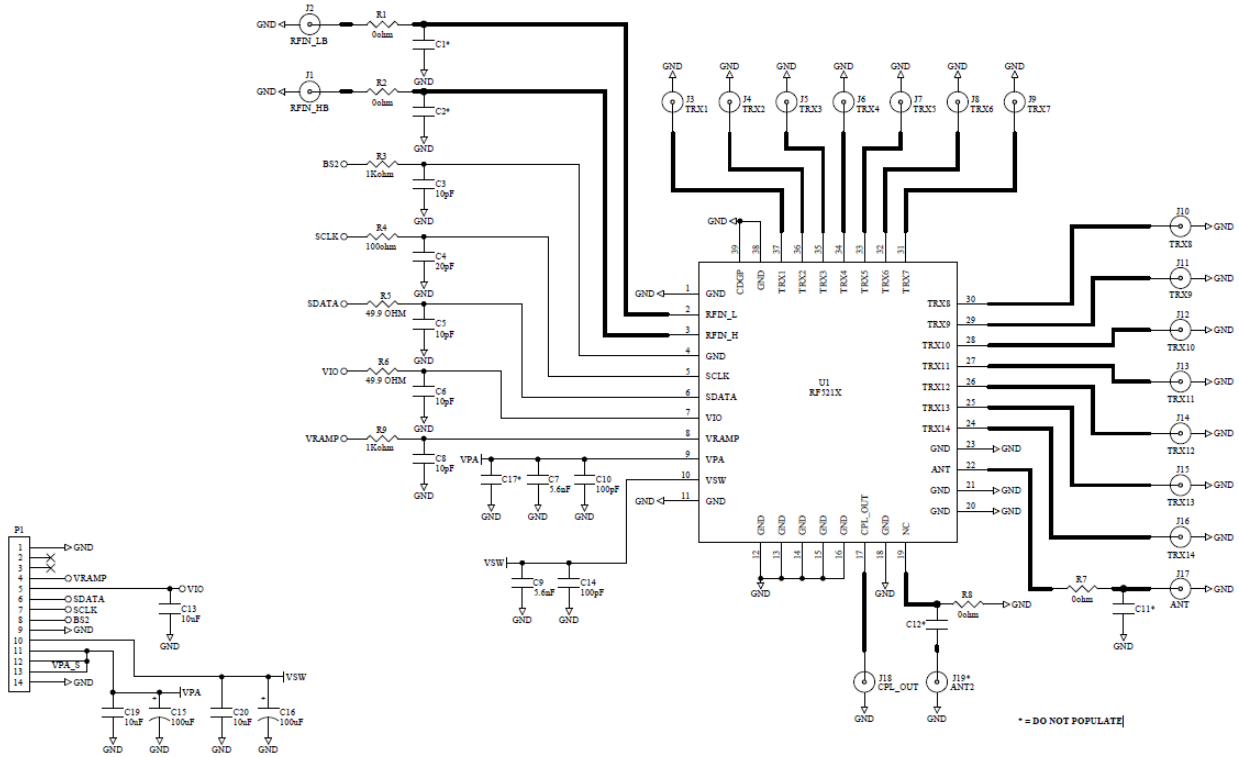
EDGE Transmit



Evaluation Board Drawing



Evaluation Board Schematic

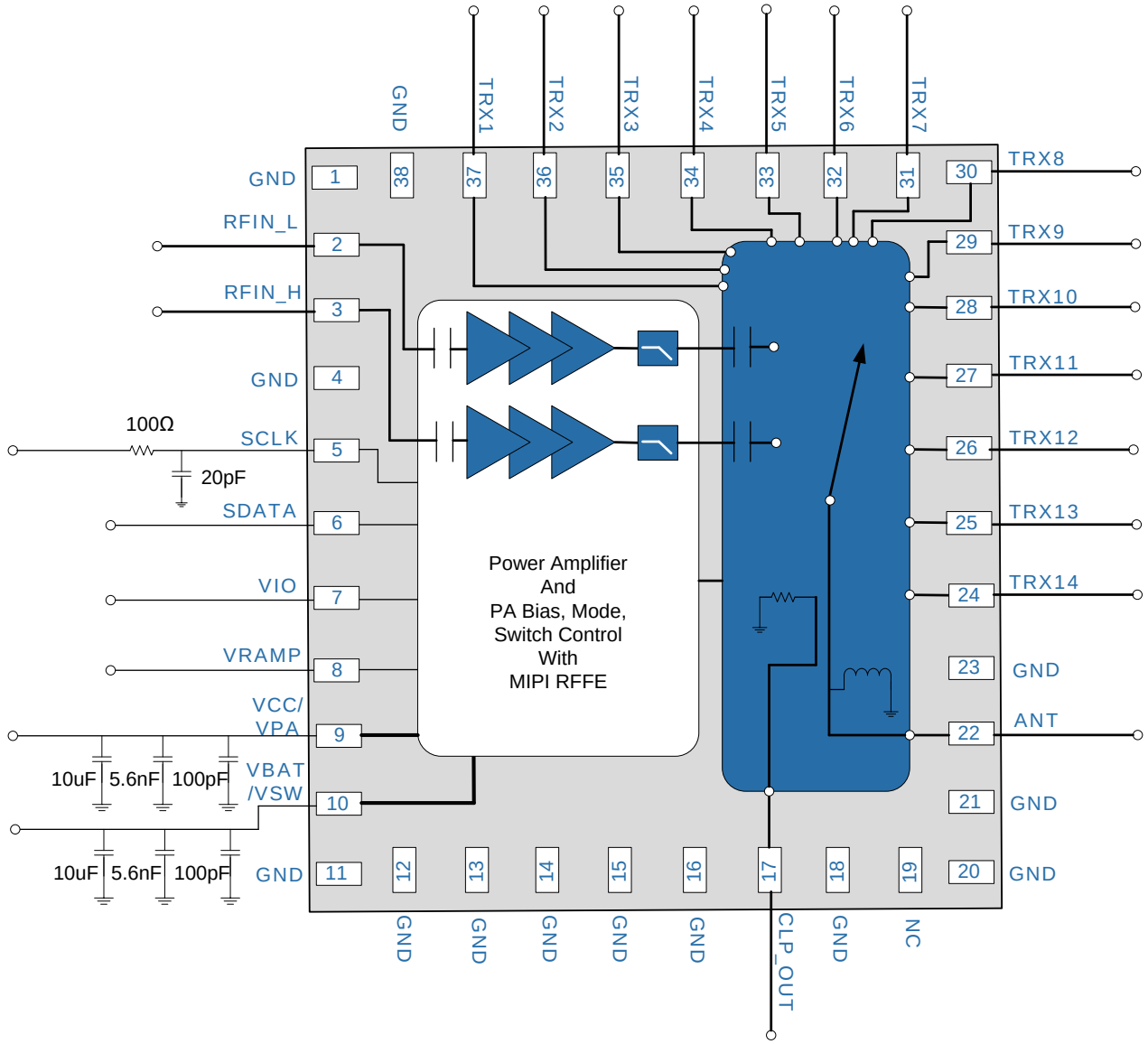


Note: EVB is for general applications. For RF5216, Pin4 is a GND pin and Pin19 is an NC/GND pin.

Evaluation Board Bill of Materials (BOM)

Description	Reference Designator	Manufacturer	Manufacturer's P/N
CAP, 10pF, 5%, 25V, C0G, 0201	C3, C5, C6, C8	AVX/KYOCERA ASIA LTD.	02013A100JAT2A
CAP, 20pF, 5%, 25V, C0G, 0201	C4	TDK Corporation of America	C0603C0G1E200JT00NN
5600 PF,10%,X7R,LF,0402, 25V	C7, C9	Murata Electronics	GRM155R71E562KA01D
CAP, 100pF, 5%, 25V, C0G, 0201	C10, C14	Taiyo Yuden (USA), Inc.	RM TMK063 CG101JT-F
CAP, 10uF, 10%, 6.3V, X5R, 0805	C13	Taiyo Yuden (USA), Inc.	CE JMK212BJ106KG-T
CAP, 100uF, 20%, 10V, TANT-D	C15, C16	AVX Corporation	TAJD107M010RNJ
CAP, 10uF, 10%, 10V, X5R, 0805	C19, C20	Murata Electronics	GRM21BR61A106KE19L
CONN, SMA, EL FLT VIPER, MAT-21-1038	J1 thru J18	Amphenol RF Asia Corp	901-10425
CONN, HDR, ST, PLRZD, 14-PIN	P1	ITW Pancon	MPSS100-7-C
RES, 0 OHM, 0402	R1, R2, R7, R8	Kamaya, Inc	RMC1/16SJPTH
RES, 1K, 5%, 1/20W, 0201	R3, R9	Kamaya, Inc	RMC1/20-102JPA15
RES, 100 OHM, 5%, 1/20W, 0201	R4	Kamaya, Inc	RMC1/20-101JPA15
RES, 49.9 OHM, 1%, 1/20W, 0201	R5, R6	Kamaya, Inc	RMC1/20-49R9FPA15
DUT	U1	RFMD, Inc.	RF5216

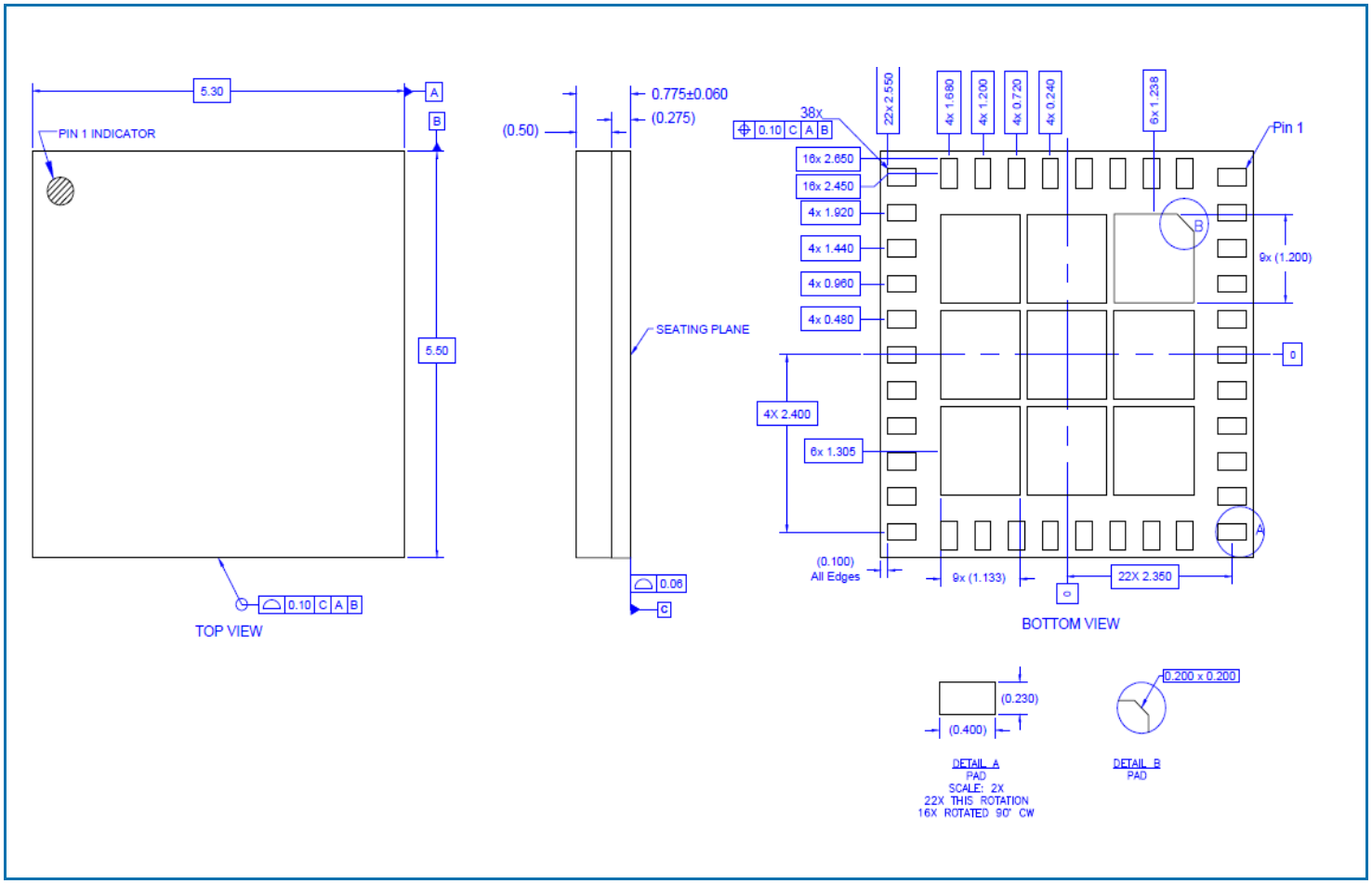
Application Schematic



Notes:

- Suggested decoupling values. Actual requirements may vary with application.
- An R/C filter of 100ohm/20pF is required on SCLK line for better MIPI noise performance, and place them close to SCLK pin.
- All RF paths should be designed as 50 ohm microstrip or stripline.

Package Outline and Branding Drawing (Dimensions in millimeters)



PCB Design Guidelines

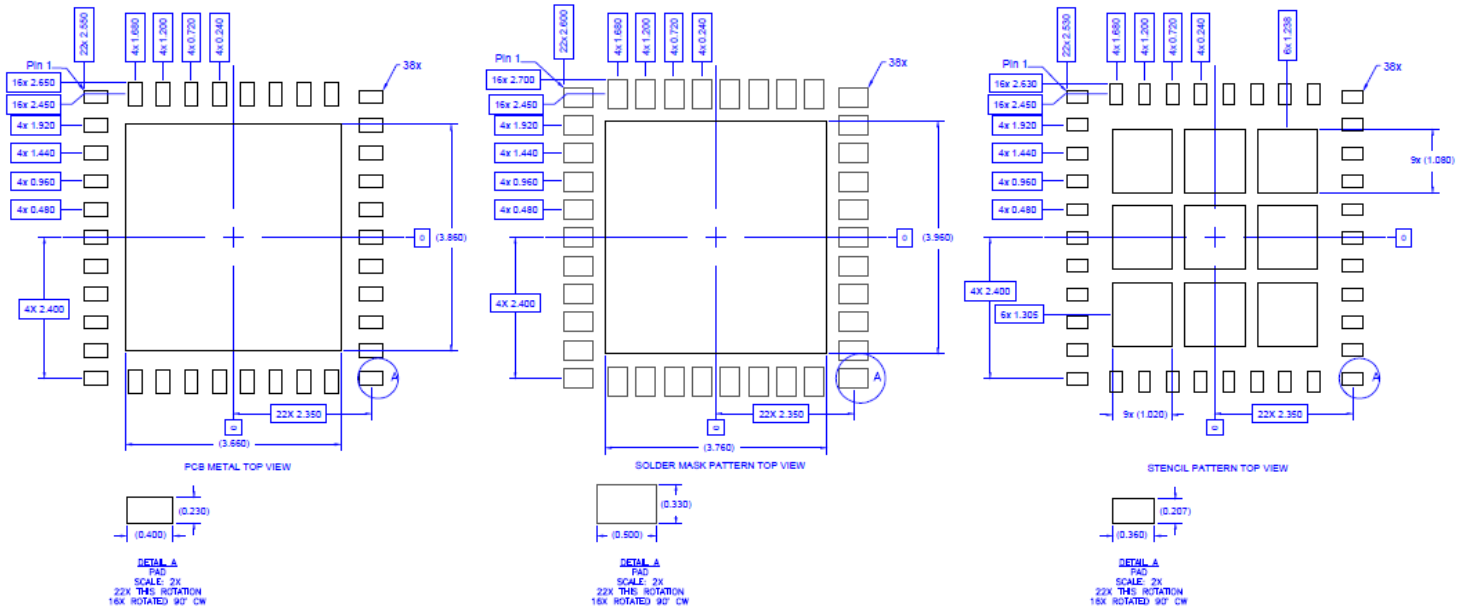
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 2 to 5 µinch gold over 180 µinch nickel.

PCB Land Pattern

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



Revision History

Revision	Release Date	Description
DS20141006	October 2014	Initial release
DS20141030	October 2014	Update isolation spec for HB ULL-TRX4 and TRX5
DS20141208	December 2014	Add note to EVB schematic about Pin4 and Pin19
DS20141216	December 2014	Update VCC and VBATT normal operating range
DS20150126	January 2015	Update T/R order information, and R/C filter for SCLK in EVB schematic, BOM and application schematic
DS20150312	March 2015	Update EDGE power levels.
DS20150327	March 2015	Updated miscellaneous specs based on final sample data
DS20150829	August 2015	Updated RXBN section and updated with current specs.
DS20151001	October 2015	Updated EDGE PAE and ICC. B13 2fo.