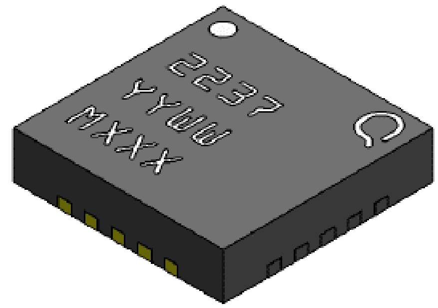
Product Description

Qorvo's QPA2237 is a wideband amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. The QPA2237 operates from 0.03 – 2.5 GHz and provides 10W of saturated output power with 13 dB of large signal gain and 52% power-added efficiency.

The QPA2237 is available in a low-cost, surface-mount, 20 lead, 4x4 OVM QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The QPA2237 is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.



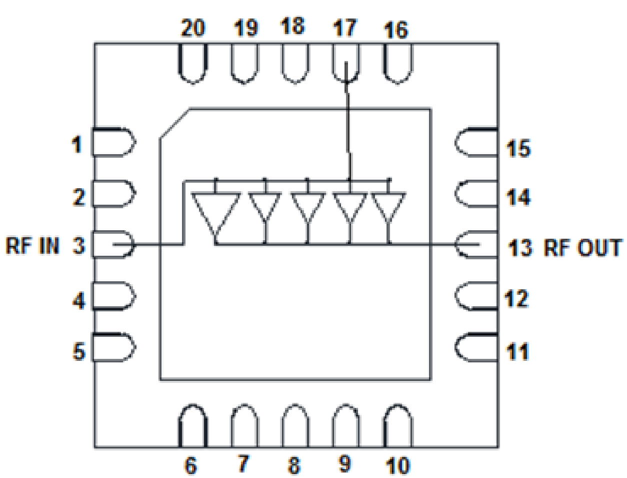
QFN 4x4 mm 20L

Product Features

- Frequency Range: 0.03 – 2.5 GHz
- P_{SAT}: 40 dBm at P_{IN} = 27 dBm
- PAE: 52%
- Large Signal Gain: 13 dB
- Small Signal Gain: 18.5 dB
- Input Return Loss: 9 dB
- Output Return Loss: 9.5 dB
- Bias: V_D = 32 V, I_{DQ} = 360 mA
- Wideband Flat Power
- Package Dimensions: 4.0 x 4.0 x 0.85 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Commercial and military radar
- Communications
- Electronic Warfare

Ordering Information

Part	Description
1131921	0.03 – 2.5 GHz 10 W GaN Power Amplifier, Qty 100
1131925	Evaluation Board, Qty 1.

Recommended Operating Conditions

Parameter	Value / Range
Drain Voltage (V_D)	+32 V
Drain Current (I_{DQ})	360 mA
Temperature (T_{BASE})	−40 to 85 °C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

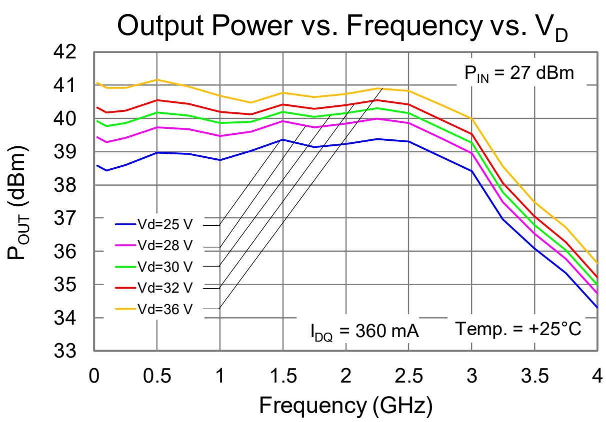
Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.

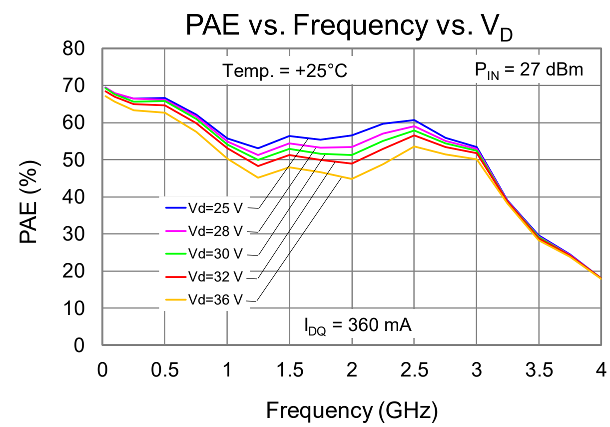
Parameter [1, 2]		Min	Typ	Max	Units
Operational Frequency Range		0.03	–	2.5	GHz
Output Power @ P_{IN} = 27 dBm	Frequency = 0.05 GHz	39.5	40.5	–	dBm
	Frequency = 1.25 GHz	39.5	40.1	–	
	Frequency = 2.5 GHz	39.5	40.4	–	
Power Added Efficiency @ P_{IN} = 27 dBm	Frequency = 0.05 GHz	48	65	–	%
	Frequency = 1.25 GHz	48	48.5	–	
	Frequency = 2.5 GHz	48	57	–	
Small Signal Gain	Frequency = 0.05 GHz	–	22.5	–	dB
	Frequency = 1.25 GHz	–	20	–	
	Frequency = 2.5 GHz	–	19	–	
Input Return Loss	Frequency = 0.05 GHz	–	9	–	dB
	Frequency = 1.25 GHz	–	13	–	
	Frequency = 2.5 GHz	–	13	–	
Output Return Loss	Frequency = 0.05 GHz	–	10	–	dB
	Frequency = 1.25 GHz	–	11	–	
	Frequency = 2.5 GHz	–	16	–	
Gate Leakage (V_D=30V, V_G=−5.0V)		−2.4	–	–	mA
Small Signal Gain Temperature Coefficient		–	−0.017	–	dB/°C
Output Power Temperature Coefficient		–	−0.004	–	dBm/°C
Recommended Operating Voltage:		–	32	36	V

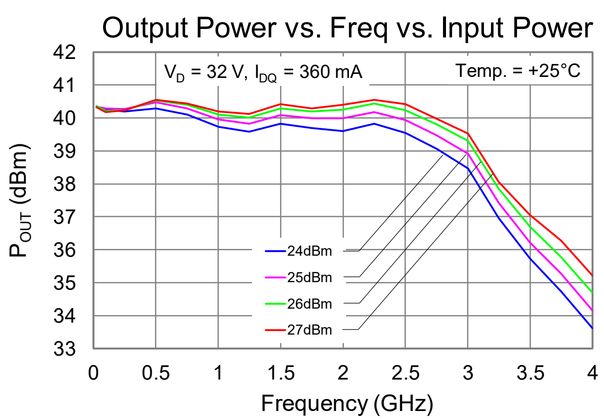
1. Test data shown are de-embedded of blocking cap and bias-tee effects.
2. DVT test employed external coaxial bias-tee, not on-board version which uses L1 choke as shown in EVB and application circuit.

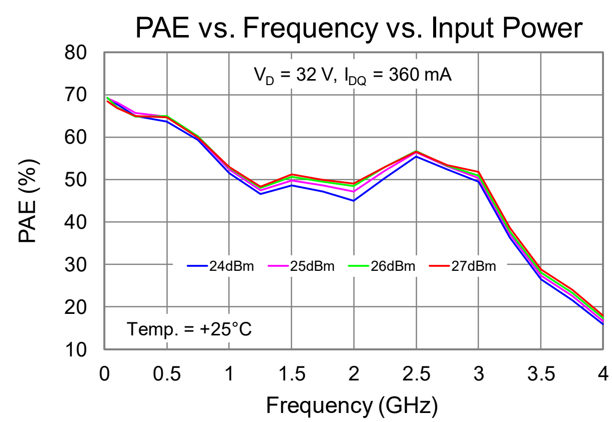
Performance Plots – Large Signal (CW)

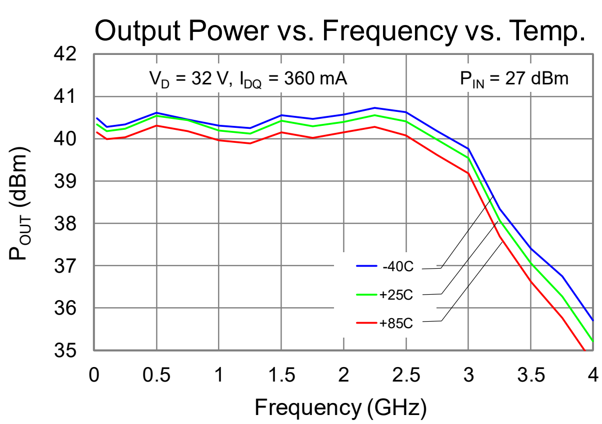
Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.

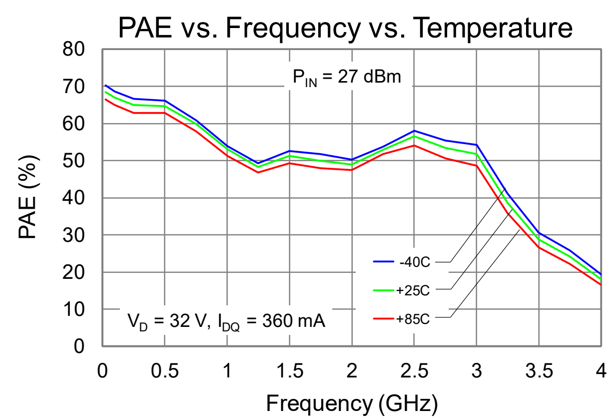






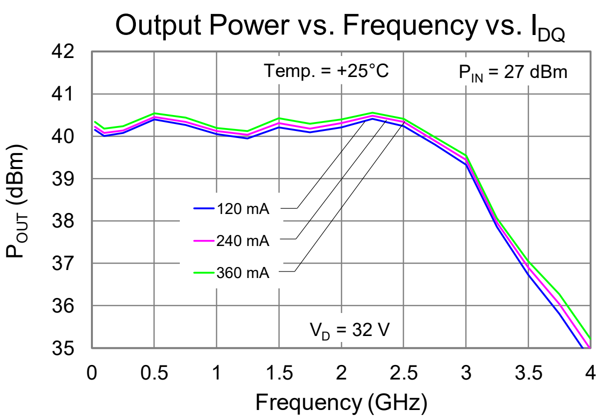


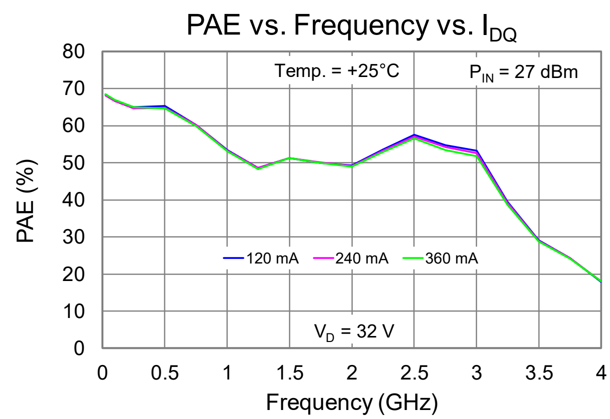


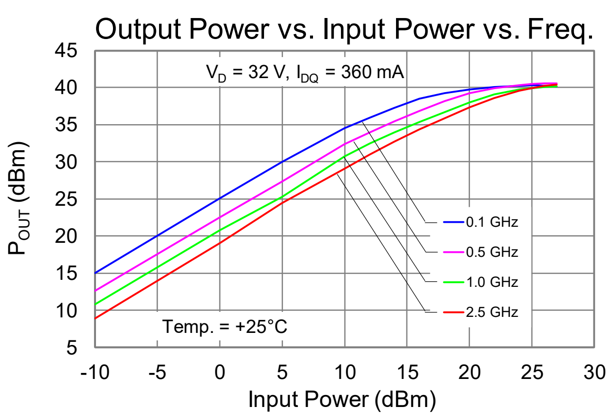


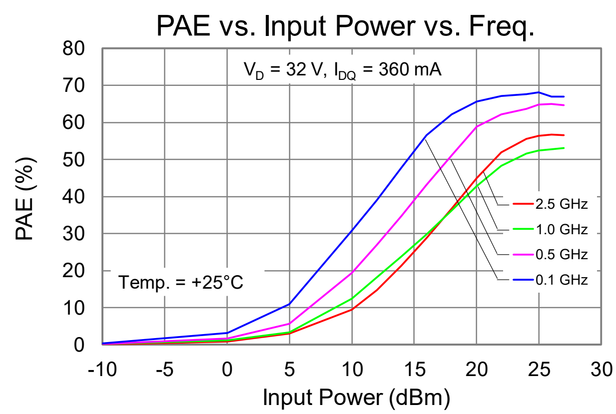
Performance Plots – Large Signal (CW)

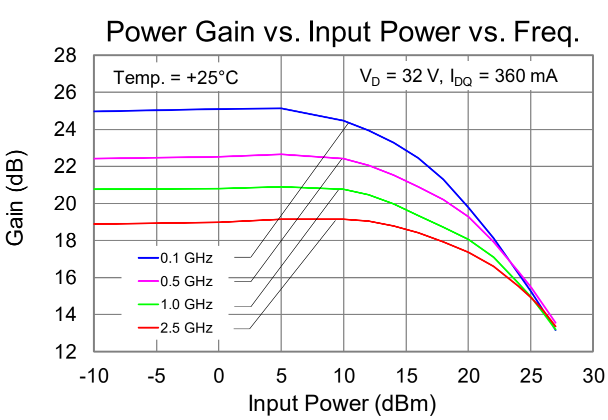
Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.

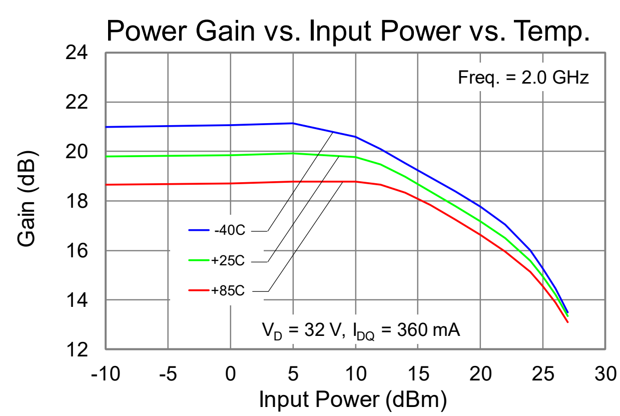






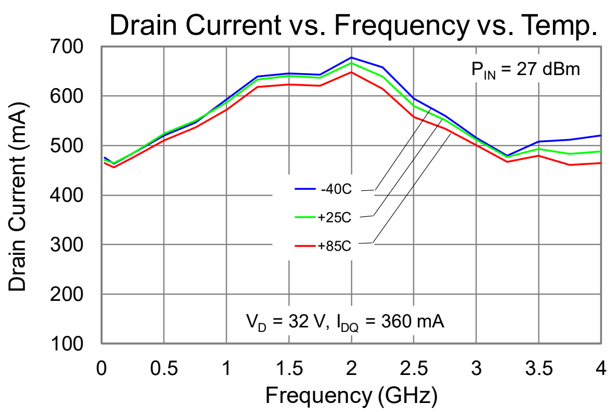


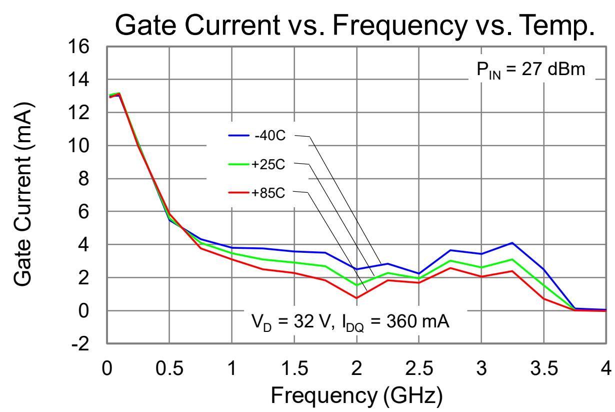


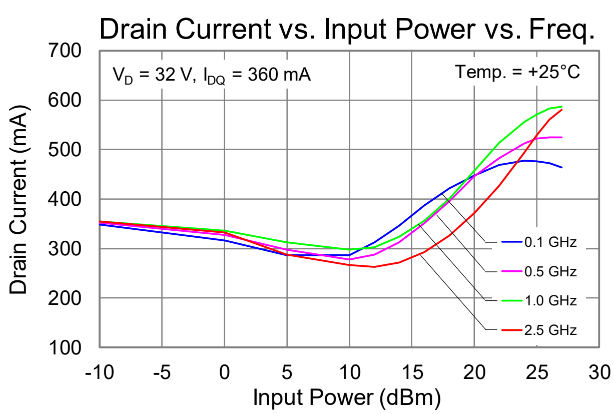


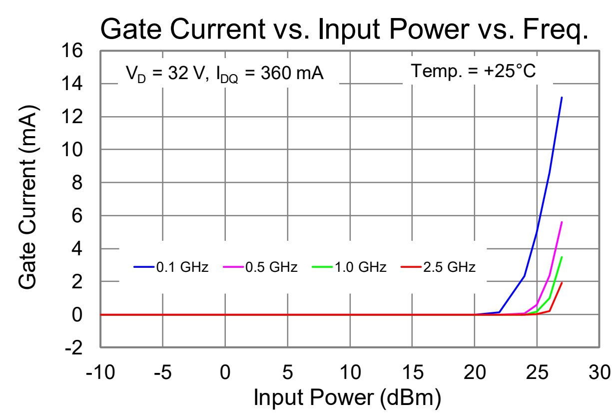
Performance Plots – Large Signal (CW)

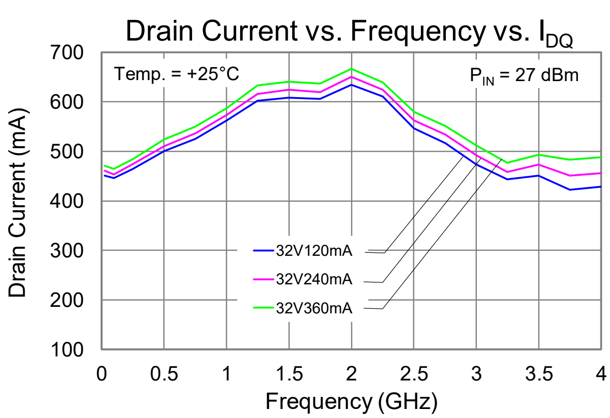
Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.

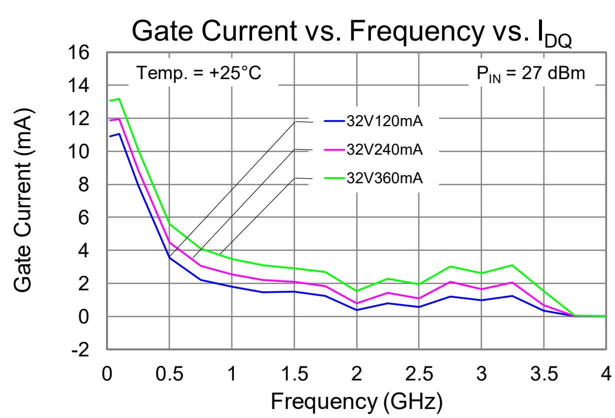






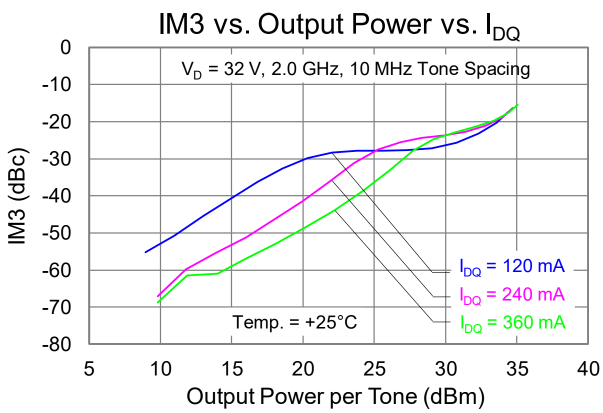


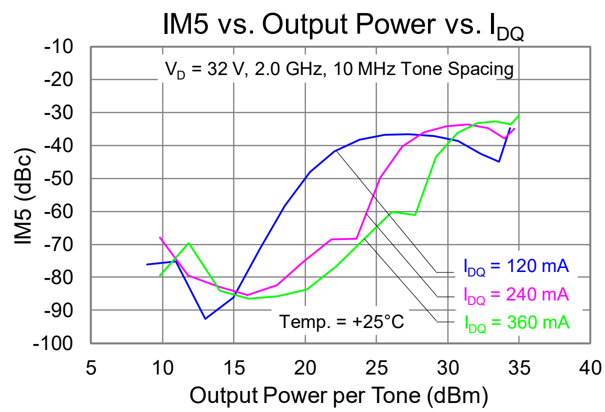


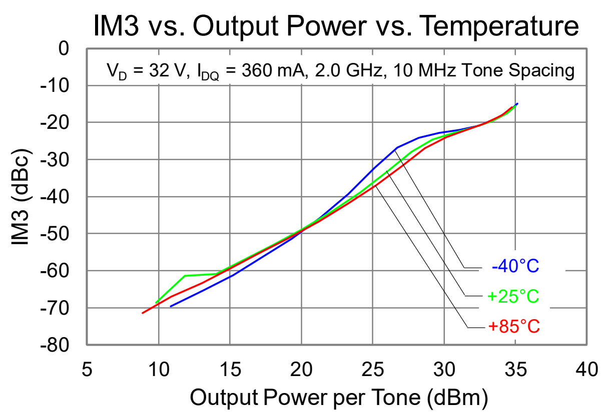


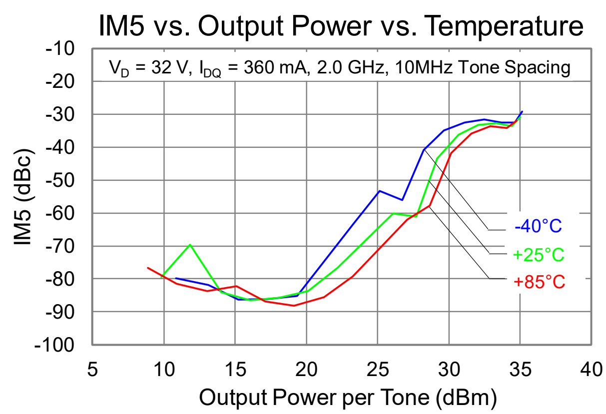
Performance Plots – Linearity

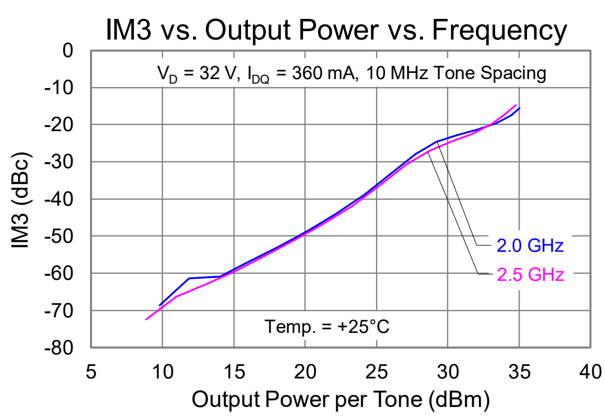
Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.

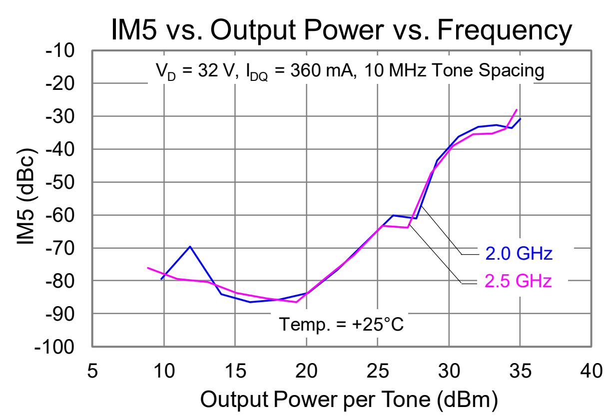








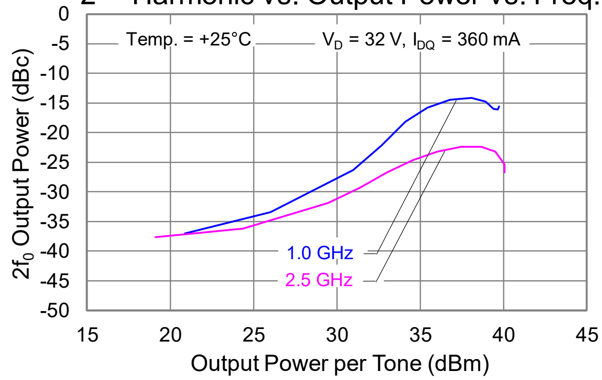




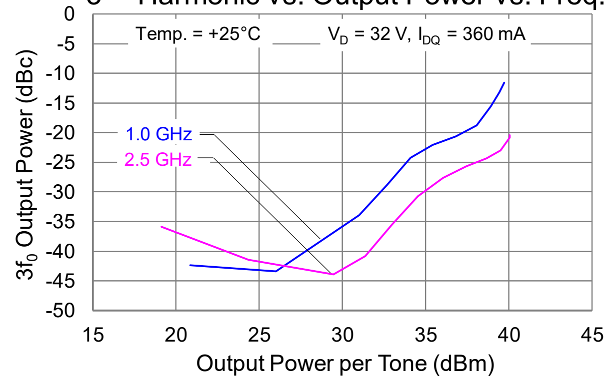
Performance Plots – Linearity

Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.

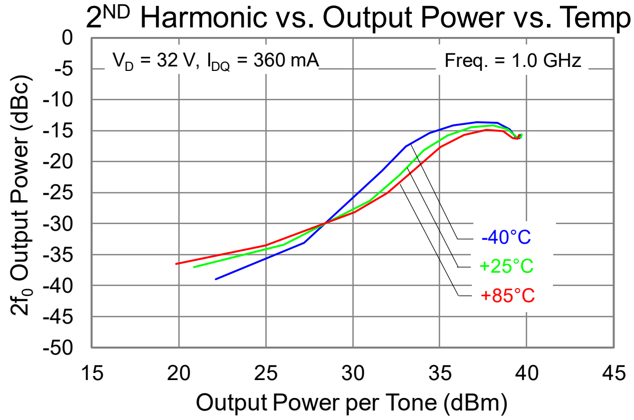
2^{ND} Harmonic vs. Output Power vs. Freq.



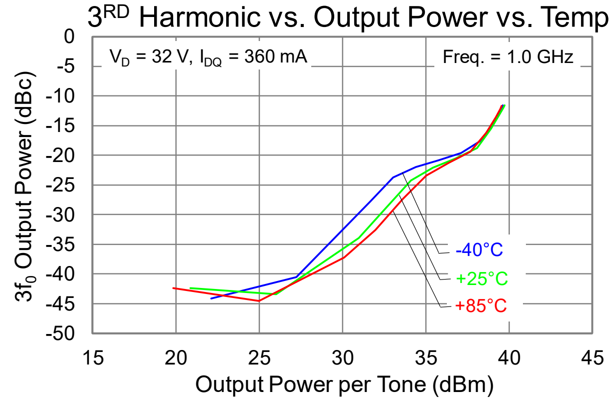
3^{RD} Harmonic vs. Output Power vs. Freq.



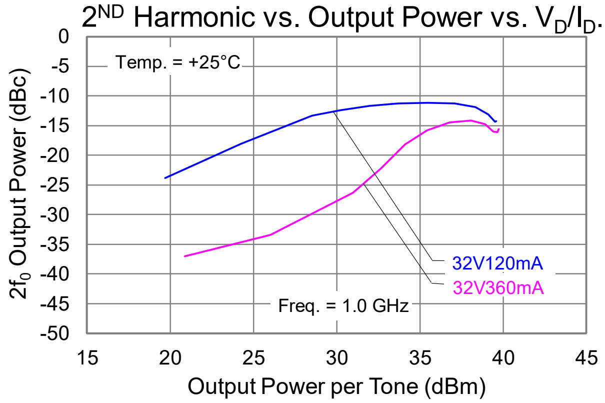
2^{ND} Harmonic vs. Output Power vs. Temp.



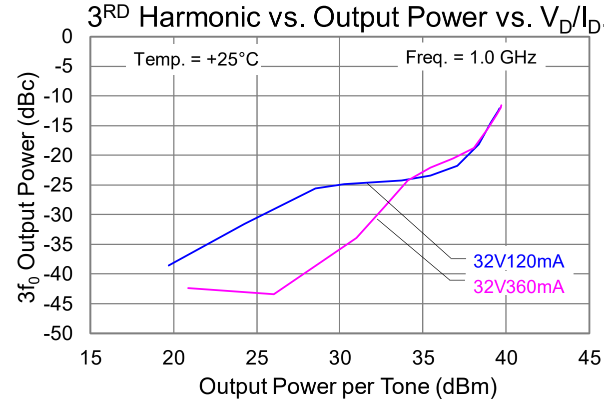
3^{RD} Harmonic vs. Output Power vs. Temp.



2^{ND} Harmonic vs. Output Power vs. V_D/I_D.

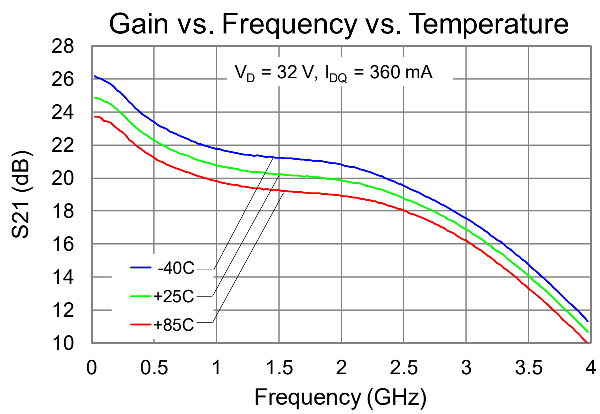


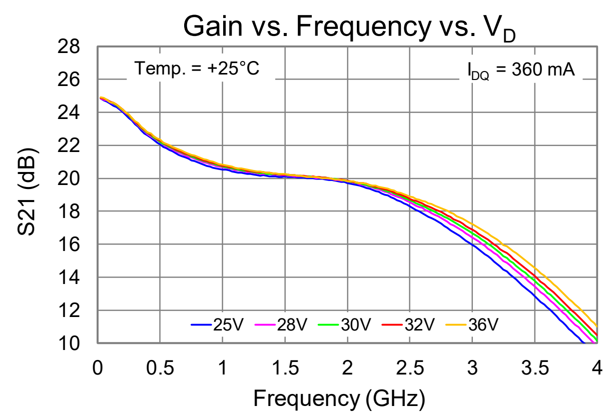
3^{RD} Harmonic vs. Output Power vs. V_D/I_D.

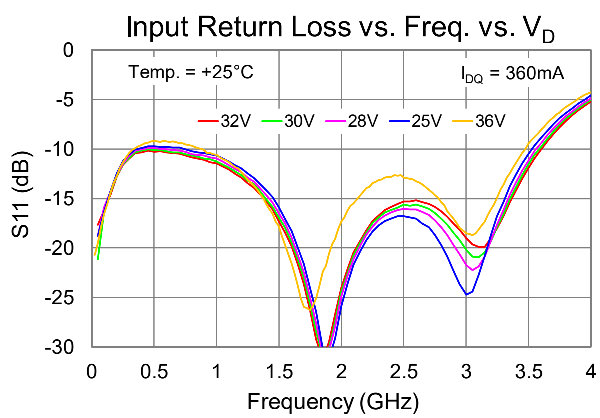


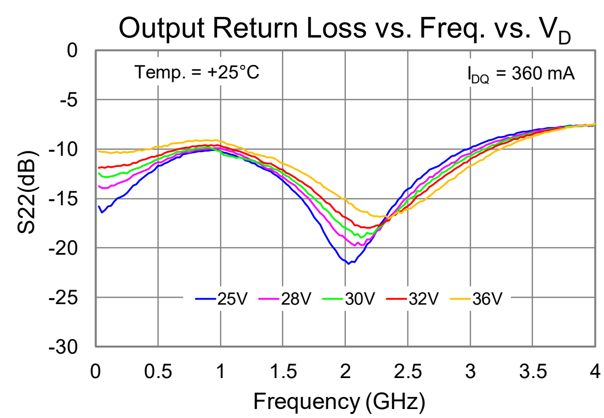
Performance Plots – Small Signal

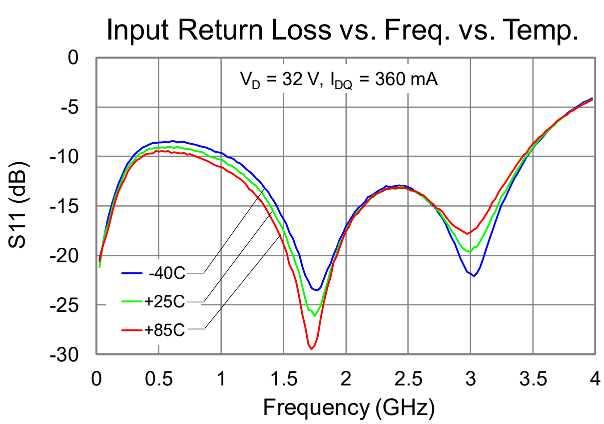
Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.

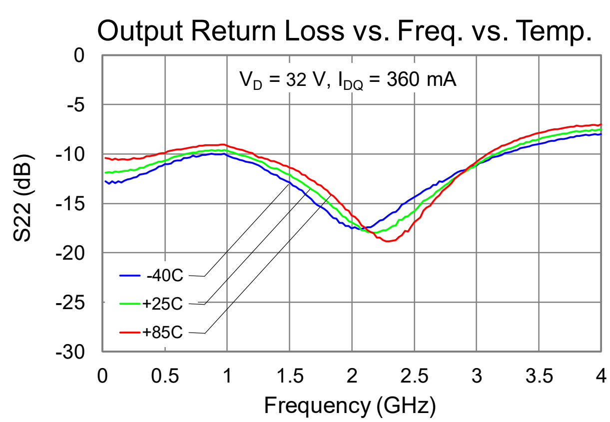






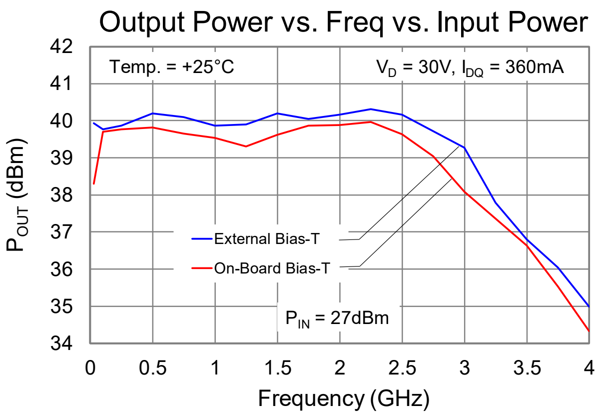


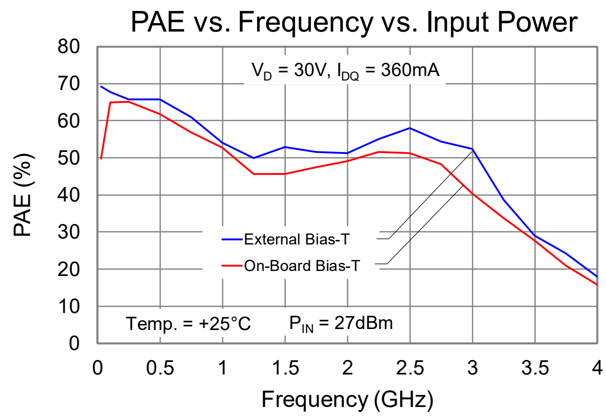




Performance Plots – Large Signal (CW), On-board vs External Coaxial Bias-Tee

Test conditions unless otherwise noted: V_D = +32 V, I_{DQ} = 360 mA, CW, 25 °C.





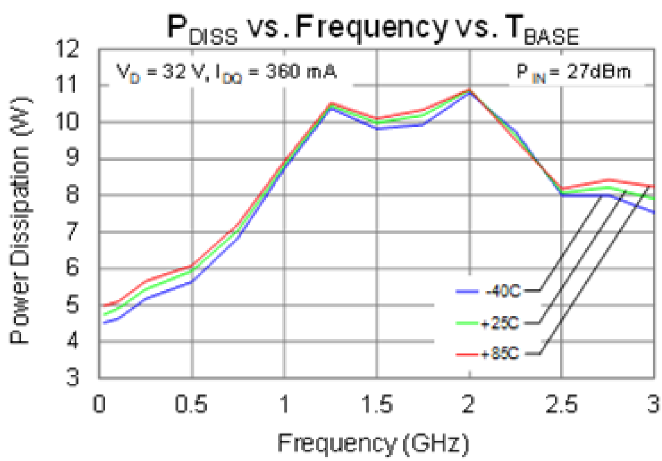
Thermal and Reliability Information

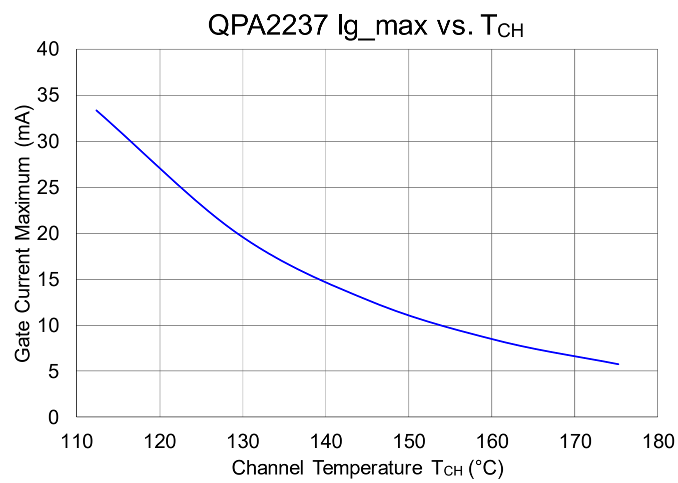
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) [1]	T_{BASE} = 85 °C, V_D = +32 V (CW), Freq = 2.0 GHz, P_{IN} = 27 dBm, I_{DQ} = 360 mA, I_{D_Drive} = 648 mA, P_{OUT} = 40 dBm, P_{DISS} = 10.9 W	5.948	°C/W
Channel Temperature (T_{CH}) (Under RF drive) [2]		149.8	°C

Notes:

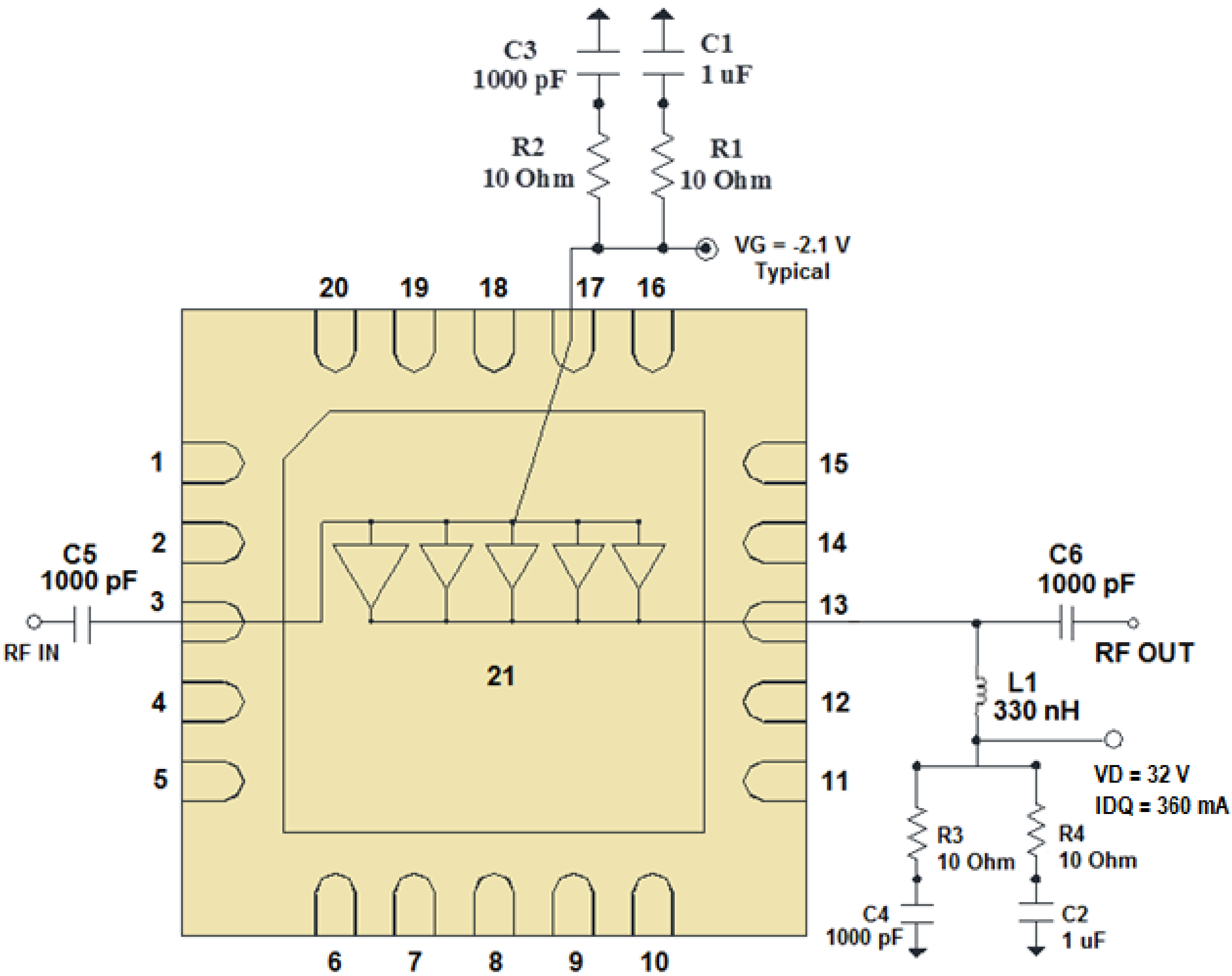
1. Thermal resistance referenced to back of package with base temperature at 85 °C.
2. IR scan equivalent channel temperature. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Maximum Gate Current





Application Circuit



Notes:

1. There is DC voltage at RF ports, if this causes issue, DC blocks (C5 and C6) should be used.
2. Test data shown are captured using external coaxial bias-tee, data de-embedded of bias-tee and blocking cap effects.
3. The EVB employed an on-board bias-tee at the output port. Performance of the DUT with DC blocks and bias-tee components may be degraded, these components should be optimized for the desired operational bandwidth.

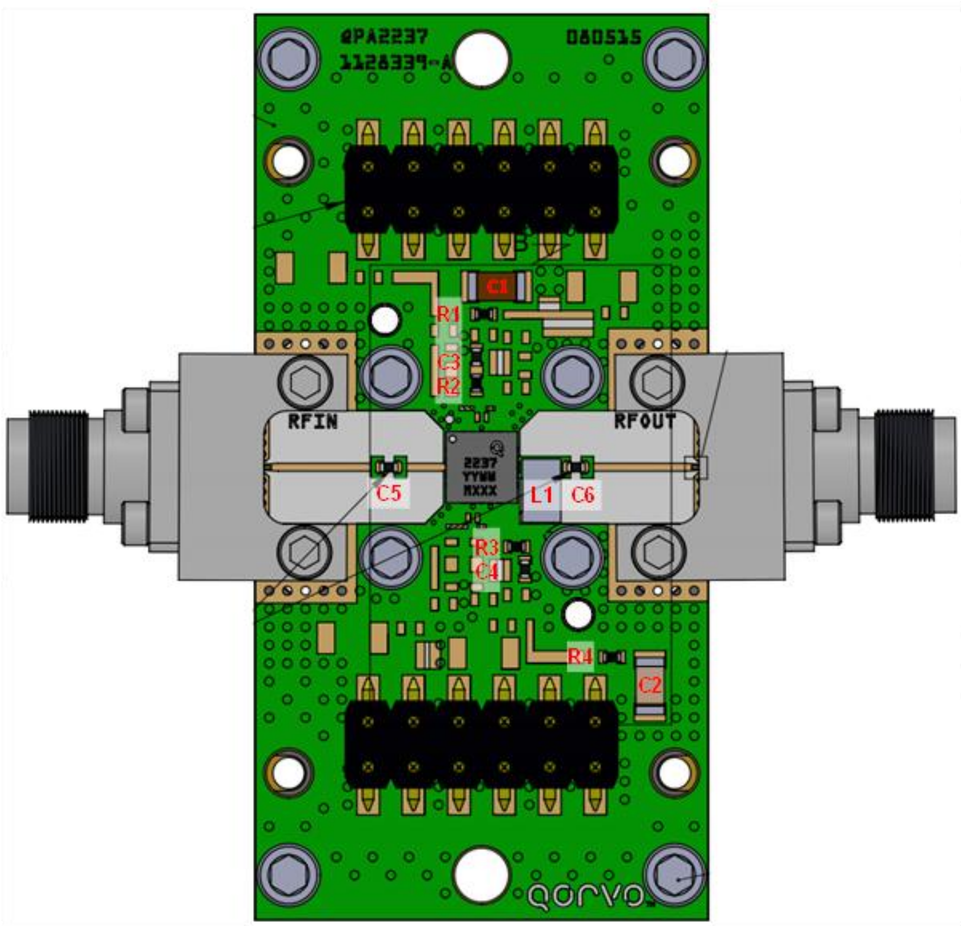
Bias Up Procedure

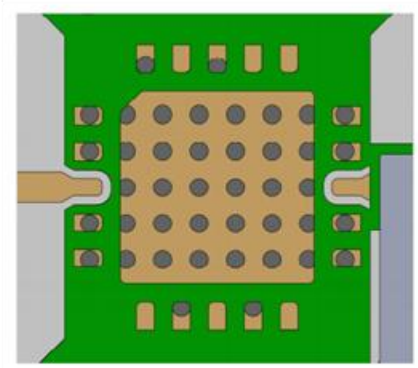
1. Set I_D limit to 700mA, I_G limit to 15mA
2. Set V_G to -5.0V
3. Set V_D +32V
4. Adjust V_G more positive until I_{DQ} = 360mA (V_G ~ -2.1V Typical)
5. Apply RF signal

Bias Down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

EVB Layout (with On-Board DC Blocks and Bias-Tee)



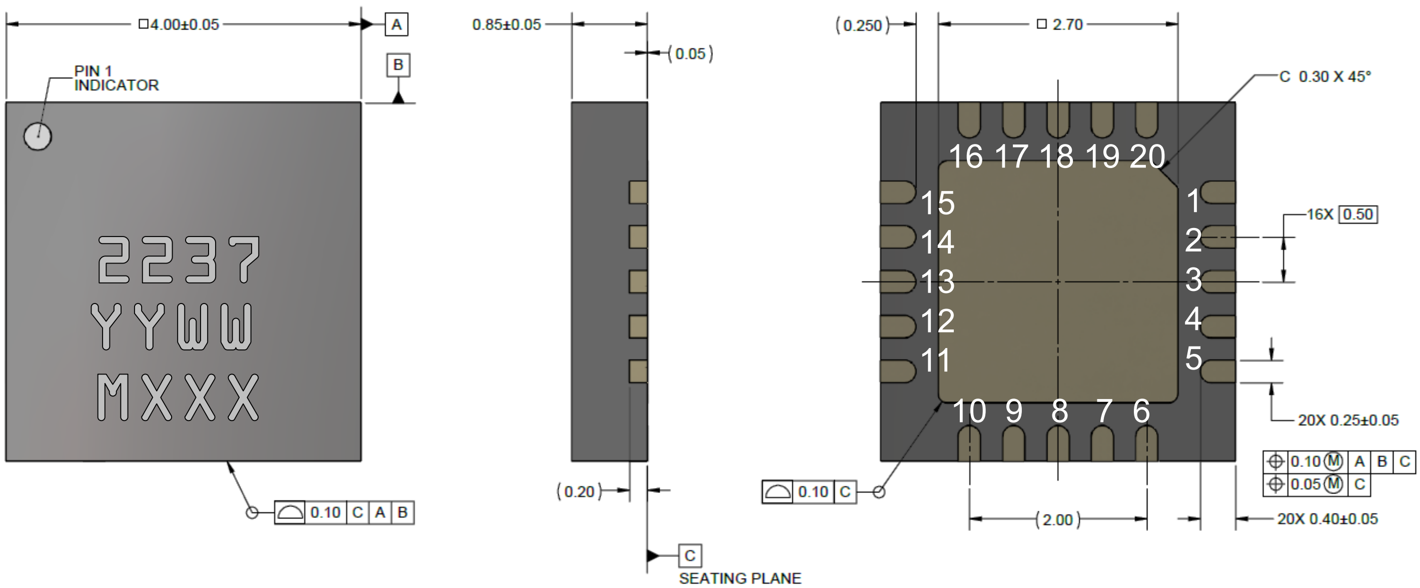


Package Pad Landing Area

Bill of Materials for EVB

Reference Des.	Value	Description	Manuf.	Part Number
C1, C2	1 uF	Cap, 1206, 50V, 5%, X7R	Various	–
C3 – C6	1000 pF	Cap, 0402, 100V, 10%, X7R	Various	–
L1	330 nH	Ind, 1206, 850mA, 5%	Various	–
R1 – R4	10Ω	Res, 0402, 5%, SMD	Various	–

Mechanical Information



NOTES (UNLESS OTHERWISE SPECIFIED):
1. ALL DIMENSIONS ARE IN MM
2. PACKAGE LEADS ARE GOLD PLATED
3. PART IS MOLD ENCAPSULATED
4. PART MARKING
   - 2237: PART NUMBER
   - YY: PART ASSEMBLY YEAR
   - WW: PART ASSEMBLY WEEK
   - XXX: BATCH ID

TOLERANCES
.XX = ± .25
.XXX = ± .127
.XXXX = ± .0254

Pin Description

Pin No.	Symbol	Description
1, 2, 4 – 12, 14 – 16, 18 – 20	N/C	No connection
3	RF IN	RF Input; matched to 50 Ω, DC coupled.
13	RF OUT / V_D	RF Output and Drain Voltage; matched to 50 Ω, DC coupled.
17	V_G	Gate Voltage, bias network is required; see recommended Application Information on page 11
21	GND	Ground Paddle. Multiple vias should be employed on the PCB to minimize inductance and thermal resistance.

Absolute Maximum Ratings

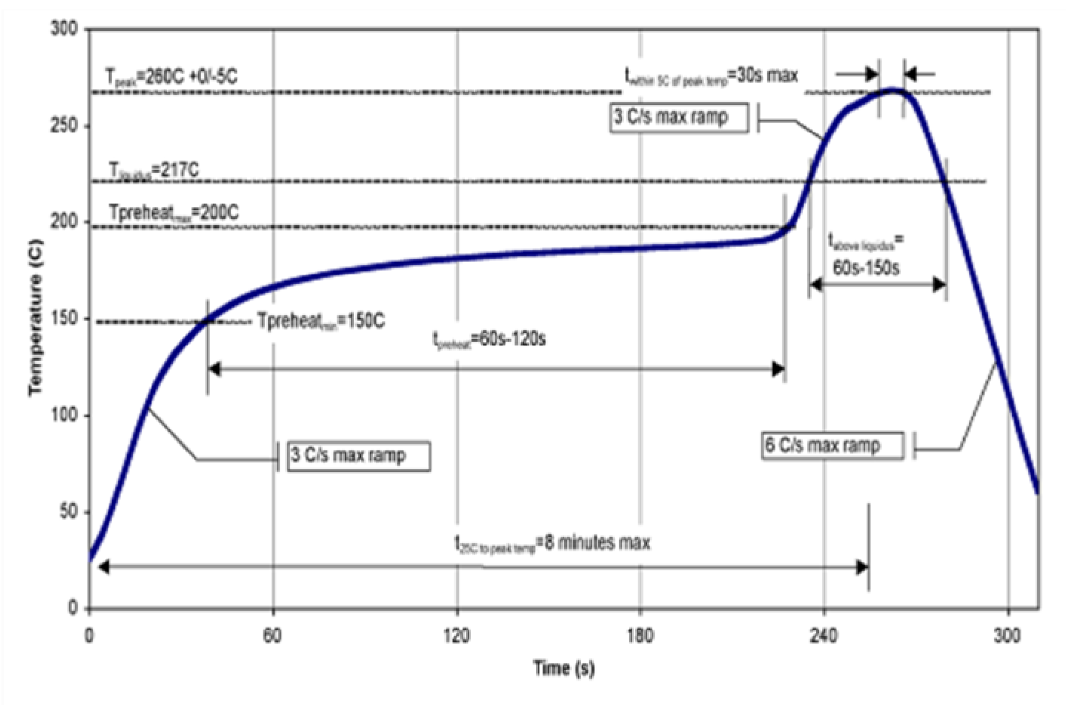
Parameter	Min	Max	Units
Drain Voltage (V_D)	-	40	V
Gate Voltage Range (V_G)	-8	0	V
Drain Current (I_D)	--	1.2	A
Gate Current (I_G)	See plot page 10		
Power Dissipation (P_{DISS}), 85 °C	-	19	W
Input Power (P_{IN}), CW, 50 Ω, 85 °C	-	33	dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 32 V, 85 °C	-	33	dBm
Max VSWR, CW, P_{IN} = 27 dBm, V_D = 32 V, 85 °C (Load)	-	10:1	N.A.
Storage Temperature	-55	150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

Contact plating: NiPdAu.



Recommended Soldering Temperature Profile

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 3A	JEDEC Standard JESD22-A114
ESD – Charge Device Model (CDM)	Class C3	JESD22-C101
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU. This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notices

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