

Design Rules Verification Report

Filename : C:\Users\labyrne\My Projects\4082_PCB_QPM1000_Space_121515\Design-PCB_QPM1000\PCB_QPM1000_1139256-A.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (OnLayer('Keep-Out Layer'),(InNet('GND') And OnLayer('Metal1_Top'))	0
Clearance Constraint (Gap=10mil) (OnLayer('Keep-Out Layer'),(InNet('GND') And OnLayer('METAL2_BOTTOM'))	0
Clearance Constraint (Gap=10mil) ((InComponent('U1') AND IsPad)),(InNet('GND'))	0
Clearance Constraint (Gap=5mil) (OnLayer('Keep-Out Layer'),(InNetClass('RF'))	0
Clearance Constraint (Gap=5mil) (OnLayer('Metal1_Top'),(InNetClass('RF'))	0
Clearance Constraint (Gap=10mil) (All),(All)	0
Width Constraint (Min=6mil) (Max=100mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0mil) (Conductor Width=0mil) (Air Gap=0mil) (Entries=4) (All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All))	0
Minimum Annular Ring (Minimum=0mil) ((IsVia AND InNet('GND')))	0
Hole Size Constraint (Min=1mil) (Max=300mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Preferred=500mil) (All)	0
Hole To Hole Clearance (Gap=5mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=3mil) (All),(All)	0
Silk To Solder Mask (Clearance=3mil) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=0mil) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Total	0