1.0 Introduction

The third generation (3G) of cellular networks requires a high linearity from the power devices to ensure minimum spectrum growth in the adjacent bands. As a result they have to operate in deep power back off mode from the P_{1dB} power level, where efficiency is poor. This is especially true for system standards like WCDMA, TDS-CDMA and CDMA2K where the PAR, peak-to-average power ratio, is typically above 10dB. Those numbers are valid for single carriers and adding more carriers the PAR increases by a factor of log(n), where n = number of carriers. The industry now is showing a trend in the use of multi-carrier systems and the power amplifiers are required to handle the extra power and still offering a good tradeoff between linearity and efficiency.

The efforts to push the InGaP/GaAs HBT technology towards high power density is finally showing results that qualify this technology to compete with traditional HFET, PHEMT and LDMOS technologies in the range of 1W to 10W. A new series of high voltage HBT devices were recently developed by WJ Communications to provide CW power at the 1dB gain compression point in the range 33dBm (AP601), 36dBm (AP602) and 38.5dBm (AP603) all showing over 50% of collector efficiency. Tuning the AP601 device for linear operation and driving it with a single carrier WCDMA signal and a PAR of 8.6dB, it provides an output power of 24dBm, 18% efficiency and an ACLR of -50dBc. The performance of the other devices in the series are similar, they roughly provides 3dB and 6dB more power compared to the AP601. These test results are very significant improvements in efficiency and linearity over published results from other technologies.

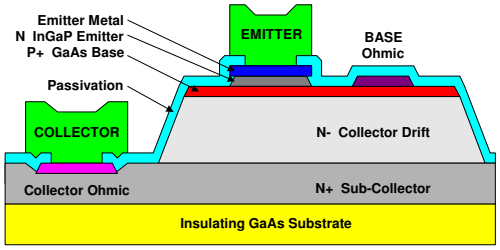
2.0 HV InGaP HBT Technology

2.1 InGaP HBT vs. LDMOS

InGaP/GaAs HBT (hetero-junction bipolar transistor) has emerged as the candidate for future high frequency power devices to address high linearity application. In the past, LDMOS has been the incumbent RF power amplifier technology. As the requirements of high frequency and high linearity become the trend of the future wireless communication systems, LDMOS is gradually running out of steam. InGaP HBT emerges.

As shown in Fig. 1, InGaP HBT is a bipolar device produced on GaAs substrate. It inherits basic properties of bipolar transistors as tabulated in Table I. With hetero-junction of InGaP and GaAs epilayer as emitter and base layers respectively, InGaP HBT provides a much lower base resistance with thinner base with higher doping level in the base region. As a result, it offers a much higher frequency performance. Benefit from the cancellation of higher order harmonics terms, InGaP HBT exhibits a better performance in linearity than other technology available in the market. As a result, it is a natural candidate for the driver stage in a power amplifier, which requires a very highly linear pre-driver or driver stages. But, due to the electrical/thermal properties of a bipolar device, InGaP HBT also needs ballasting resistors in

either emitter or base to stabilize its operation at high temperature operation. With an optimized ballasting scheme in the transistor design, bipolar devices are as stable as LDMOS devices in high temperature operation.



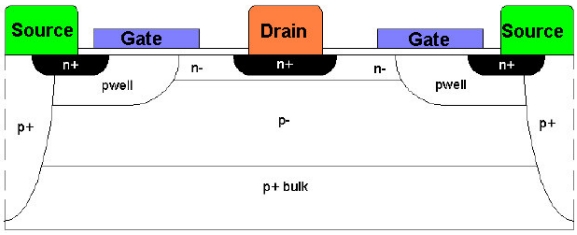


Fig 1 - InGaP/GaAs HBT Structure Fig 2 - LDMOS Transistor Structure

As shown in Fig 2, LDMOS is a field effect transistor device produced on silicon substrate. In order to optimize the trans-conductance of the device, the channel doping level and thickness is limited. As a result, the current density in the channel is lower than that of a HBT device. Due to the continuous advance in LDMOS technology in the past two decades, it has maintained the mainstream technology for the RF power devices. However, it will reach its limit in increasing operating frequency. This provides an opportunity for the competing technologies, such as InGaP HBT and GaN HEMT as the emerging technology for the future.

Table I. Comparison between InGaP HBT and LDMOS

	InGaP HBT	LDMOS
Output Current Source	Current-Controlled	Voltage-Controlled
Primary Current Flow	Vertical	Horizontal
Input Impedance	High Capacitance	High Capacitance
Output Admittance	Low Conductance	High Capacitance
Input Bias Circuit	Current Mirror	Voltage Divider
Intrinsic Gain at 2 GHz and 28V	20-23 dB	13-16 dB
Device Thermal Stability	need ballasting	Stable
Substrate Thermal Conductivity	Lower	Good
Substrate RF Isolation	Good	Poor
Die Integration Level	Multi-Stage	Multi-stage

2.2 InGaP HBT I-V Characteristics

A typical I-V characteristics of an InGaP HBT is shown in Fig. 3. Similar to silicon bipolar transistor, it has a very flat DC current gain (beta) over a wide range of collector current. The current gain will only start to drop when its collector current reaches a high range where Kirk effect starts to be meaninful. This flatness of beta provides a good linear behavior over a wide range of current. But, it can also cause a damage to the junction if a sudden high input voltage pulse drives the collector current into thermal runaway due to the positive temperature coefficient of the Vbe of a InGaP HBT. These characteristics are well known in the old Si bipolar technology. Several thermal ballasting techniques have been developed in the past to stabilize the Si bipolar circuits. Similar techniques are applicable to InGaP HBT. A carefully designed InGaP HBT will incorporate adequate ballasting scheme to stabilize itself in the operation range defined by the maximum operating condition. However, any unwanted over-stressed operation can cause a permanent damage of the device.

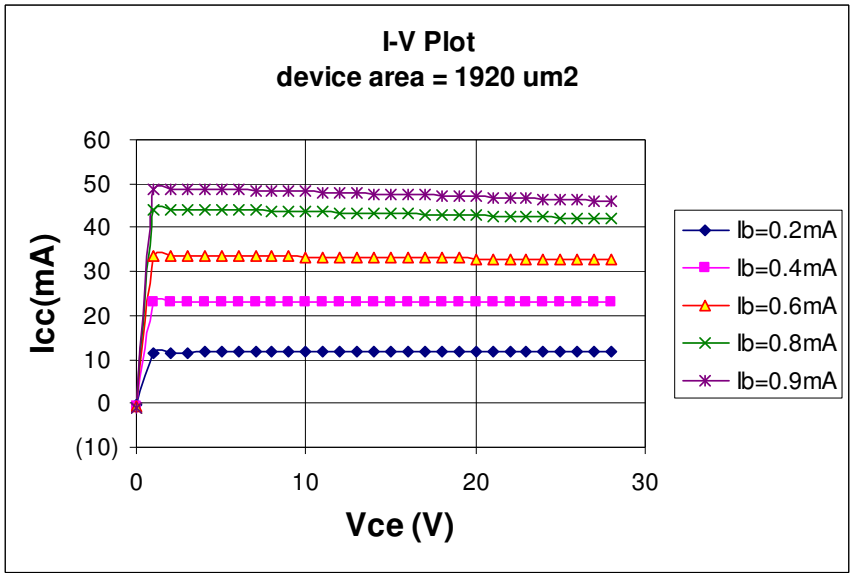


Fig 3 - A typical InGaP HBT I-V plot

2.3 InGaP HBT Operation

With an active biasing circuit connected to the base of an InGaP HBT, we can drive the device from a class A to class AB operations and still obtain a very good linearity performance. As shown in Fig. 4, the ACLR of device tested at class AB condition and under WCDMA modulation at 2.14GHz can drop to below -55dBc. By adjusting the biasing current to class A condition, this ACLR performance can be further improved.

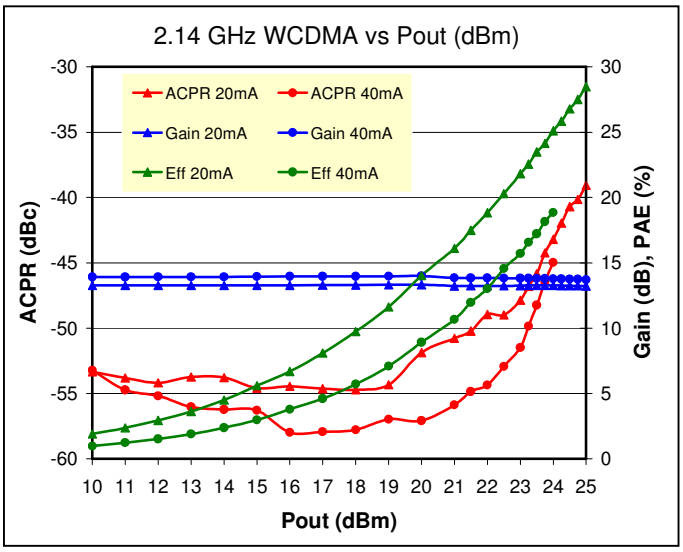


Fig 4 - ACLR Performance of an InGaP HBT amplifier tested at 2.14 GHz under WCDMA test method

With a proprietary dynamic active biasing circuit, we can further improve the ACLR of an InGaP HBT amplifier even with a class AB operation. This improvement gives us a design margin to trade-off ACLR against efficiency of an amplifier. This unique advantage on the linearity performance makes InGaP HBT the best candidate for the driver stage in a highly linear amplifier design.

2.4 WJ's High Power, 28V HBT Technology

WJ's 28V HBT technology has already been published in several publications. The epi-wafer is grown exactly the same as that of a 5V InGaP HBT except that collector layer is much thicker. As a result, the wafer process requires a very unique process to take care of a highly non-planar surface. The thick collector is designed to a give high breakdown voltage across the base-collector (BC) junction. Typical values of VB_{CB0} > 70V and VB_{CE0} > 40V are consistently obtained. A cascade probable device measuring $3x8\mu m^2$ was characterized and showed an f_T of 6.4GHz and f_{max} of 25GHz at V_{CC}=28V and J_C=5.5 kA/cm^2.

A photo of a device layout containing 32 fingers measuring $3x20\mu m^2$ is shown in figure 5. Each one of the fingers incorporates an integrated emitter ballast resistor to minimize the possibility of thermal runaway and the base current is supplied by a current mirror circuit. The basic block contains a low pass pre-matching circuit connected at the base, which is used to raise the input impedance to a level that is easier to match with external components. The high power performance was obtained by paralleling 8 units of such basic cell on the same die. A careful thermal analysis was carried out to determine the minimum distance, which the cells can be placed on the die to minimize thermal coupling problems. In order to maintain a low current density and guarantee a high reliability, the power density of the device was set to 1.25W/mm^2 at 2.2GHz.

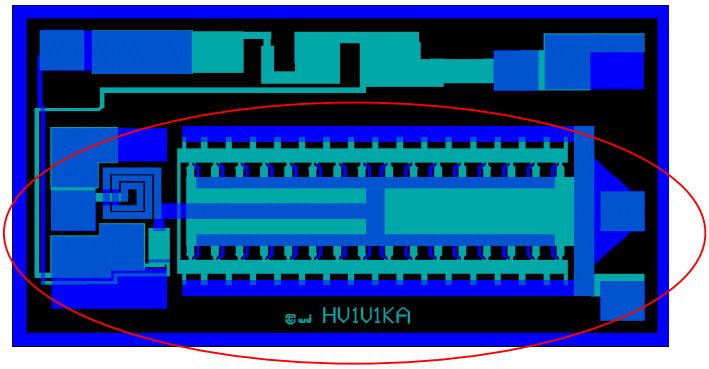


Fig 5 - Schematic for basic cell depicting the pre-matching circuit.

2.5 28V HBT Reliability

The epi-wafer of a 28V HBT is grown exactly the same as that of a typical 5V InGaP HBT except that collector thickness is thicker. Thus, the dominant failure mode of the device is the same as 5V HBT, that is beta degradation. Reliability test results show longer lifetime for High Voltage 28V HBT (HV HBT) than a conventional 5V HBT at similar junction temperatures. The main reason is the low current density given by design, which is in the order of J_C=5.2kA/cm^2 as opposite to a typical J_C=25kA/cm^2 used in a 5V HBT technology. In Fig. 6, we show a DC stress test performed on two batches of 16 devices in each batch. After 3691 hours of stress test at the condition of V_{CE}=28V, J_C=5.2 kA/cm^2, $T_{Ambient}$=230°C, and T_J~310°C, none of the 32 devices change currents. Gummel plots measured before and after the stress test are shown in Fig. 9. Combining with previously reported ruggedness and linearity performance of the same technology, the 28V InGaP HBT is a mature technology for high linearity power amplification.

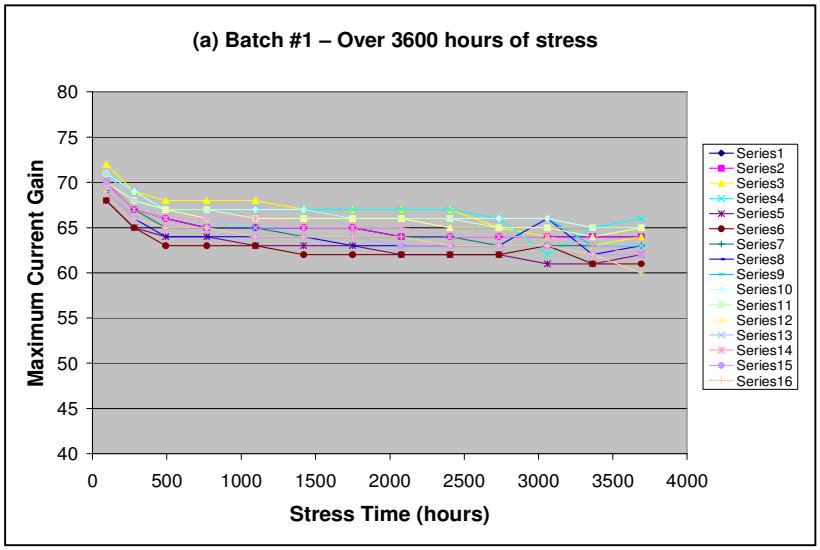


Fig 6 - DC stress test result of first batch of 16 devices after 3691 hours

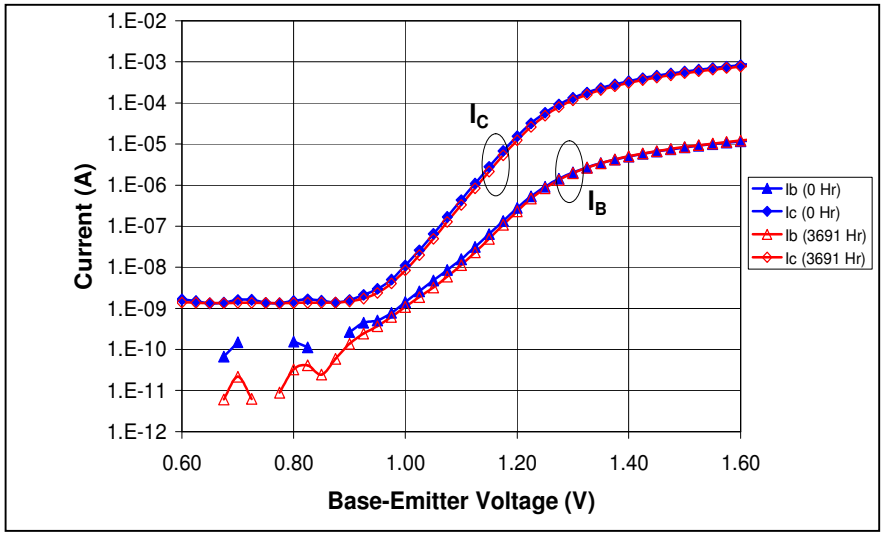


Fig 7 - Gummel plots of device before and after DC stress test

3.0 Power Amplifier Design

Any semiconductor device is irreversible modified if their temperature is increased beyond some critical limit. In bipolar devices the temperature problem is enhanced due to the thermal runaway effect and in the particular case of HBT- Heterojunction Bipolar Transistors, self heating effects takes place. Another common problem is the breakdown of the junctions in particular the collector to base, submitted to very high voltage. Therefore, it is important to design the external circuit in such a way it will prevent the current and voltages to exceed the maximum ratings. Otherwise a partial or complete burnout of the active area will be observed resulting in a catastrophic destruction. This failure mechanism is the result of a combination of factors causing an increase in power dissipation in localized areas or burnout due to avalanche breakdown. The objective of this section is to provide information on how to design, do the tuning and test of AP60x devices and avoid device destruction due to wrong handling.

3.1 SOA – Safe Operating Area

The limits on device operation for conventional bipolar devices, are given by the breakdown voltages (Collector-base, Base-emitter and Collector-emitter junctions) by the maximum collector current and the maximum power the device can dissipate. An additional limiting factor is the kirk effect that reduces the amount of allowable current on HBTs. Those limits are used to build the so called SOA – Safe Operating Area. The dynamic current and voltage at the collector must be within the safe operating area, which is illustrated in figure 8. That plot was obtained from computer simulations and corrected with some experimental data taken on AP601 device. Besides the breakdown voltages it takes account of both thermal and Kirk effects. The Safe operating area for the AP602 and AP603 can be scaled from the AP601 depicted in the figure.

The I_{CE} current should be doubled for AP602 and multiplied by four for the AP603 for the same collector voltages.

Designers using AP601 should apply bias in association with a load that prevents I, V to exceed the SOA limits. From the designers point of view the correct use of these limits can only be done with the use of a non-linear model which can predict for a particular load, which is the I, V trajectory. An example of computer simulation employing a Gummel Poon model was applied to an AP601 device, using an output impedance load determined for optimum ACLR performance for a WCDMA waveform operating at 2.14GHz. The "Ideal" load line for this class AB operation (V_{CQ}=28V; I_{CQ}=40mA) is depicted in figure 8 by a black straight line.

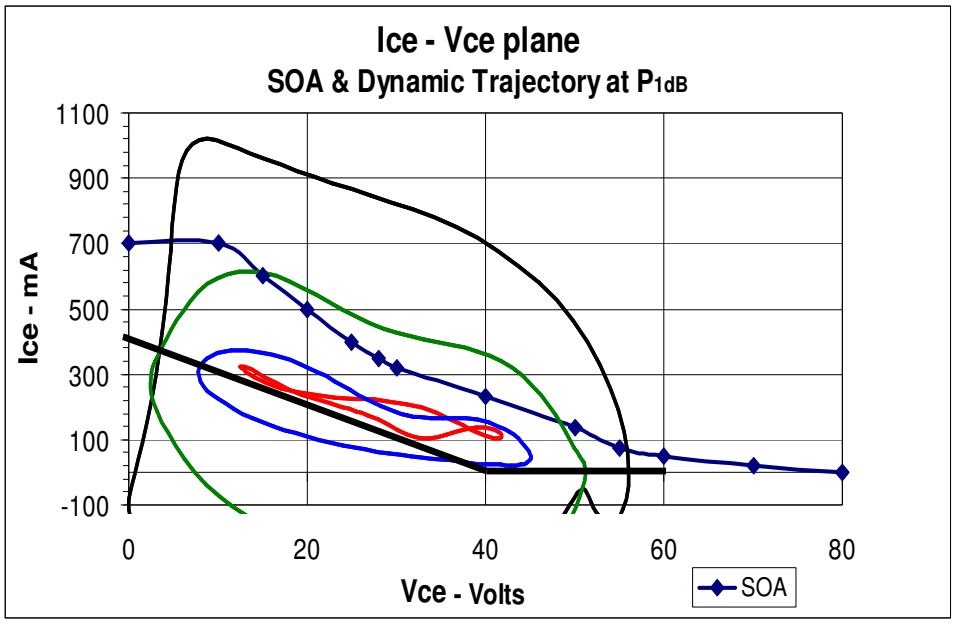


Fig 8 - SOA and dynamic trajectories near the P_{1dB} power level

The I, V trajectories were simulated for an output power near the P_{1dB} compression point by changing the device load impedance from optimum condition capacitive to inductive line. The quarter wave bias line was used for this purpose and the corresponding compression powers are in figure 9. The best condition is the blue trajectory corresponding to a smooth compression shown in figure 9.

The measured results falls right on top of the simulated gain performance. Making the bias line shorter we observe an increase in overall gain and in the gain expansion, depicted by the green plot. The trajectory on figure 8 already exceeds the SOA, with potential device damage. Making the line even there is a dramatic change in the load line with more aggression to the SOA (black contour). On the other hand, making the line longer, the trajectory is far away from the SOA limit and shows good power performance, the only degradation is on the gain.

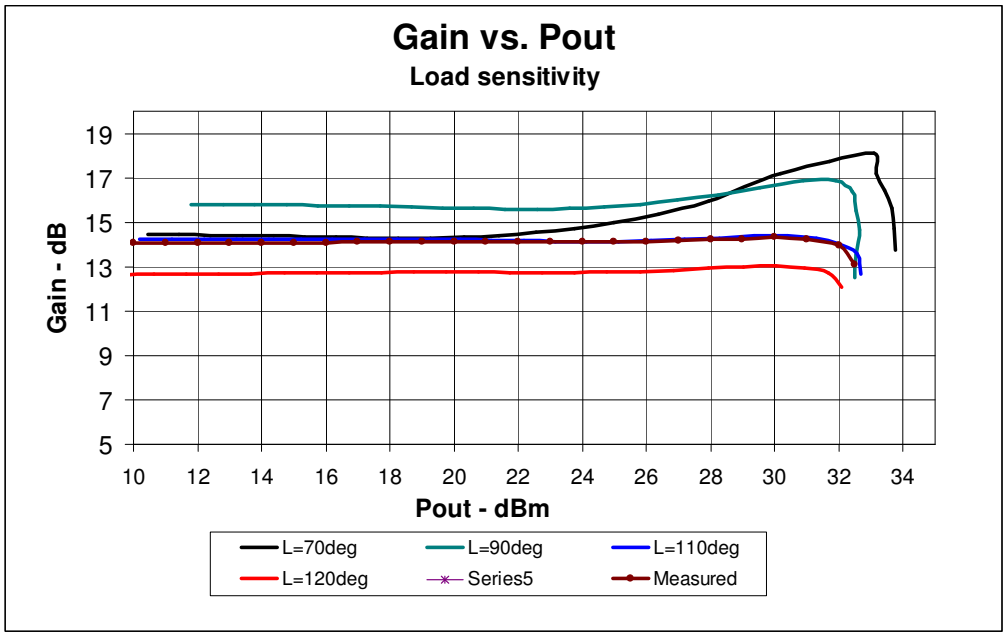


Figure 9. Gain as a function of output power.

Adjusting the circuit tuning for optimum conditions and driving the device into 6dB power gain compression, the I-V trajectory slight exceeds the SOA at 15V, 22V and 30V depicted in figure 10. This limiting value is consistent with experimental findings, i.e., the device operated safely when driven up to this compression point. The corresponding output power is 33dBm. Practical experiments show the device will be destroyed driving the input power into higher compression levels.

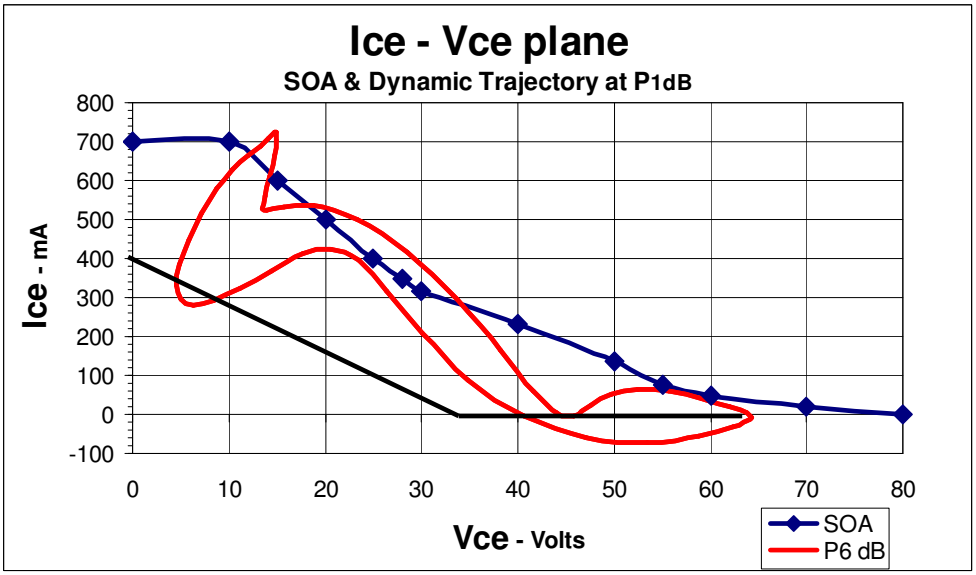


Figure 10. SOA and dynamic trajectories at P_{6dB} power level

In spite of poor power prediction of Gummel – Poon model it provided the following insights, useful for the design: a – When tuning the device near the P_{1dB} point, look for minimum gain expansion for it degrades linearity and robustness; b – Avoid saturating the amplifier before correctly tuning the load for good performance.

A particular case of interest is the submission of the device to load mismatch to determine ruggedness. Maintaining the input drive set for P_{1dB} in 50ohms load and mismatching the load with a line stretcher, there are certain phases where the trajectory will violate the safe operating area, causing burnout of device. The AP60x can sustain up to 7:1 VSWR at all phases.

3.2 Bias Circuitry

The AP60x device uses a current mirror to bias the base and an additional dynamic bias to improve linearity and efficiency. The current mirror is quite conventional and the dynamic bias uses the emitter-base junction of an emitter follower stage to act as a RF rectifier, figure 11. With higher power level the emitter base conduction change providing the extra amount of current to be supplied to the base of RF device. The amount of extra current is determined by the series resistor and the parallel capacitor. Therefore, the dynamic bias provides an increase in the base current supply at higher power levels, which improves linearity performance.

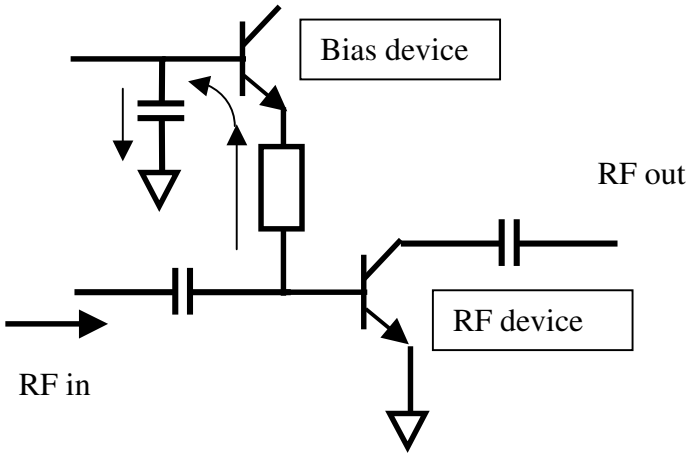


Figure 11. Simplified bias circuitry.

Up to the P_{6dB} point this circuit operates safely under a wide range of temperature range. However, exceeding this limit the extra linearization current can drive the device into thermal runaway and consequent self destruction. The RF base bias is controlled externally by the V_{PD} voltage – power down voltage and the collector is usually biased by a voltage supply connected to the device by means of a quarter wave long transmission line.

3.3 Circuit Design

The amplifier design starts with the optimum load impedance for an objective performance, either best efficiency, higher output power or best ACLR. The load impedances that determine those conditions were measured on a load pull system and the results for best ACLR for the AP601 device are on table II in terms of series equivalent for typical frequencies. Fortunately, the load value that provides the best linearity performance coincides with the load that best fits within the safe operating area. The input impedance can be obtained from S-parameters with output terminated by the load impedance from table I. At this point it is good practice to use S-parameters to generate stability circles and observe if the load and source impedances falls within those areas. If they do the circuit has to be stabilized before continuing the design. There two simple solutions to stabilization: a – move the load impedance to a stable area. This procedure is OK if the new impedance still provides reasonable linearity; b – add a small value resistor in series with the base. The effect of adding base resistance is more on gain, and minor effect on linearity. An output and input circuit is then designed to transform the load and source impedance to 50ohms. In general, at 2.14GHz, the matching circuits can be obtained with a transmission line and parallel lumped capacitors. The capacitors used in the output match are required to be of very low loss, a condition to obtain high efficiency operation.

Table II. Large signal impedance

Device type	Z_{Load} (940 MHz)	Z_{Load} (1900 MHz)	Z_{Load} (2100 MHz)
AP601	50 + j80	14 + j40	11.0 + j41.0
AP602	43 + j20.8	12.7 + j5.4	4.3 + j13.3
AP603	2.4 + j21.88	4.47 + j3.46	1.96 + j11.36

4.0 Tuning Methodology

4.1 Preparing the Test Bench

The preferred measurement set-up for tuning purposes with CW signal, is the use of a sweeper generator, a scalar network analyzer and a dual channel power meter. The evaluation of system amplifier parameters requires in the set-up the additional equipments: an E634 Signal generator loaded with the WCDMA or other complex waveform and a Transmitter tester or spectrum analyzer. When preparing your measurement set-up be sure you have a good source match, which can be obtained by adding either a 3dB pad or an isolator right at the input terminal of the DUT - device under test. The load match usually consists of a high power attenuator and a power meter or coupler included for sampling a signal for spectrum analyzer. The AP60x devices will operate safely if they are properly terminated. However, if open and short impedances are connected at the device terminals it may operate abnormally resulting in device

destruction. The connection of such terminations require an analysis of input and output stability circles from low frequencies up to around 2.5GHz to confirm if there is no risk of oscillations.

4.2 Tuning operation

Initially set the power level of your sweeper generator at small signal to start the tuning process. After you applied bias on the device avoid disconnecting the cables without turning off bias. This operation creates impedance levels during the disconnection that may drive the device into the unstable regions, resulting in its destruction. When it is time to put hands on work, it is recommended to follow the following approach: Attach the output tuning capacitor at the output transmission line. Initially use a capacitor value lower than the value determined by the load pull. Insert at the input transmission line the input capacitor and slide it from the device towards the generator, looking for best input match and gain flatness. Next drive the amplifier near the P_{1dB} power level and tune the output capacitor for best power and efficiency within the frequency band. Always turn RF power down when moving the output capacitor to avoid creating undesirable loads and RF spikes with consequent device destruction. This action will mismatch the input circuit, which will have to be retuned at small signal level. Repeat iteratively this procedure until device provides the desired performance. At this point is good practice to take the amplifier to the network analyzer and determine input and output return loss to check if the resulting impedances within the band are less than -10dB for the input match and less than -6dB for the output match.

The next step is to switch to the WCDMA generator and the Spectrum analyzer measurements. Be sure to apply the power and PAR – Peak to Average Ratio that maintains the device within safe operating region. The values on table III serves as reference for maximum power to apply to the device. The maximum power level obtained from the AP601 device is 23dBm with a PAR of 10dB. Clipping the waveform peaks to a value of 8.6dB, the output power can be extended to 24dBm.

Table III. Power compliance for the AP60x devices

Device Type	P_{1dB} (dBm)	P_{sat} (dBm)	Gain (dB)	Gain Compression (dB)	PAR (dB)	P_{IN} Maximum (dBm)
AP601	32.5	33	13	6	10	16
AP602	36.0	37	13	6	10	20
AP603	38.5	39	12	5	10	22

4.3 Drive Waveforms

CW drive: When the device is compressed with a CW waveform, its gain compression should be limited to 6dB. Exceeding this limit there is a high risk of device destruction; *RF pulse drive*: In the case of pulsed RF drive, the device will operate at a lower temperature resulting in a slight increase of output power capability. The device can tolerate RF pulses down to 10µs as long the pulse generator plus amplifier provides a clean pulsed RF. Evaluations showed gain compression higher than 4dB under pulsed mode with no destruction; *Complex Waveforms:* The various communication systems using multi-carriers generate different PAR and different shapes of peak, which in general are very narrow. Several tests were carried out for WCDMA signal and no degradation in performance was observed for the peak power a few dB into compression.

4.4 Memory Effect of an Amplifier

"Memory effect" of an amplifier circuit is defined as "the output of the amplifier depends on the past and current input signal". In terms of device transfer function the memory effect shows up as hysteresis in the dynamic AM/AM and AM/PM of an amplifier as shown in figure 12 and as asymmetrical IMD (inter-modulation distortion), figure 13, and spectral re-growth in the frequency domain. This is very undesirable in the circuits employing digital pre-distortion (DPD) technique.

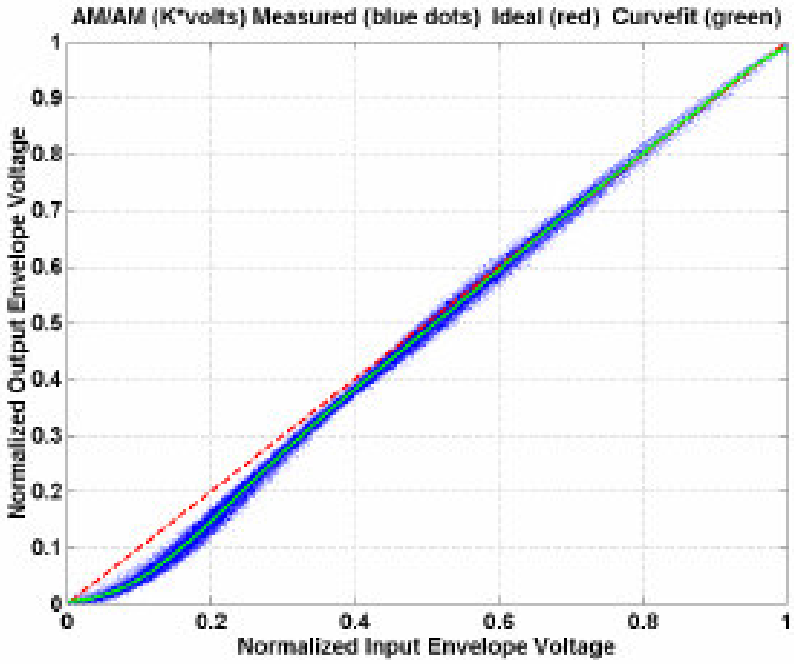


Fig. 12 AM/AM behavior of a device with memory effect. [6]

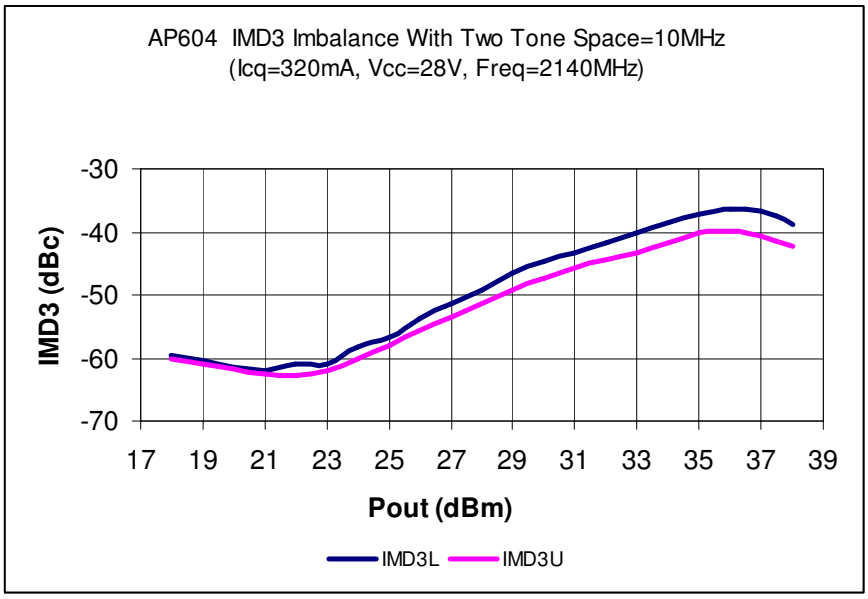


Fig 13 - A typical asymmetric IMD3 of a device with memory effect

The fundamental reason of the memory effect is due to a device I-V characteristics dependence of physical mechanisms associated with time constants close to the bandwidth of interest. Thus, possible reasons give rise to the memory effect of an amplifier are:

- RF frequency responses in main signal path
- Non-constant impedance in DC bias circuits
- Self heating effects at the device level

There are various models to characterize the memory effect. The most rigorous and complex analysis is based on Volterra series model. With simplified RC circuits with time constants close to the bandwidth of operation, Volterra model can project the IMD variation vs. tone spacing between two tones with good accuracy. Due to its complexity and time consuming in the computer simulation, this model is only used to understand the effect and is not commonly used in the circuit simulation. In Fig. 14, we show an ADS simulation result of IMD3 vs. two-tone spacing frequency on ADS system with a thermal time constant of 3µs and a trap time constant of 3ns.

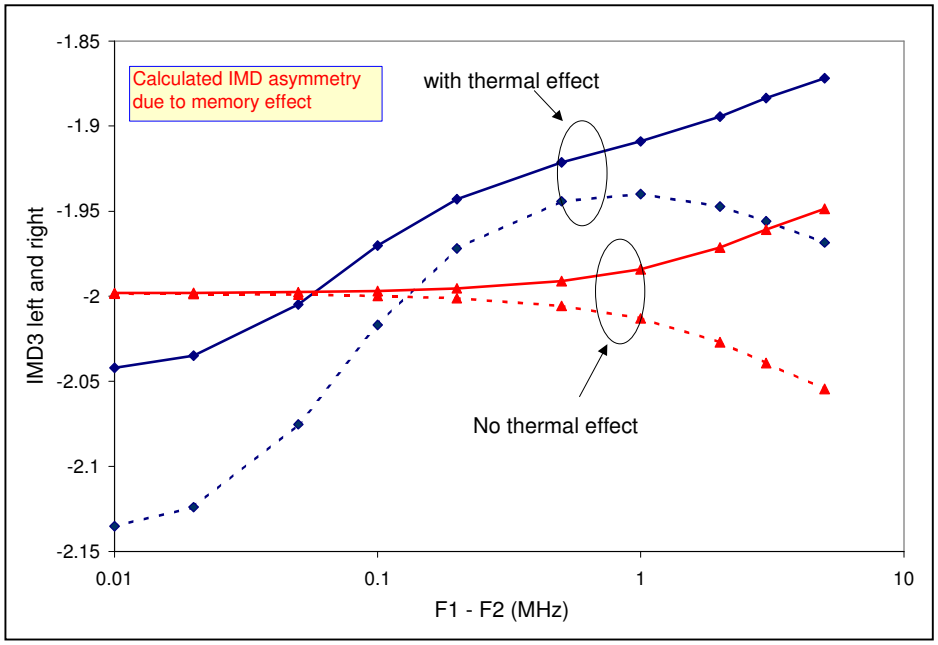


Fig 14 - ADS simulation result of IMD3 vs. two-tone spacing frequency

Instead, Memory Polynomial Model (MPM) {7,8} and Parallel Wiener Model are more commonly used in the linearizer design to quantify the memory effect. A detailed discussion on the figure of merit to quantify the memory effect can be found in references [9].

From device point of view, the physical mechanisms, which can induce memory effect, are device thermal effects, surface or bulk traps, or DC bias effects. However, to show a noticeable memory effect, the time constants of these effects should be in the range of interested bandwidth. Thus, the most effective way to minimize the memory effect of a device is to "design out" these effects by changing the time constants, such as adjusting the DC biasing circuits, reducing traps on the surface of the device or in the bulk, minimizing the thermal effect of the device in operation.

Fortunately, InGaP HBT exhibits a better memory effect in device level than other FET based technologies due to its low "surface trap effects" if the thermal effects can be minimized by a well budgeted thermal design of the device. This unique advantage can be observed in the experimental result published by J. P. Martins et. al. in Ref [10].

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