TGA2624-SM

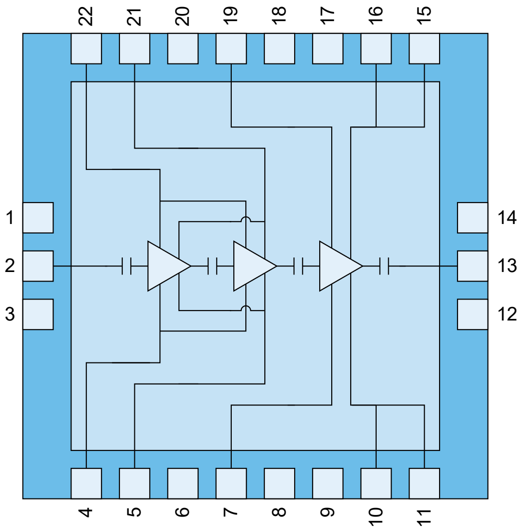
9–10 GHz 20 W GaN Power Amplifier

General Description

Qorvo's TGA2624-SM is a packaged, high power X-Band amplifier fabricated on Qorvo's production 0.25 um GaN on SiC process. Operating from 9-10 GHz, the TGA2624-SM typically generates 20 W of saturated output power with a power-added efficiency greater than 40% and 25 dB of large signal gain.

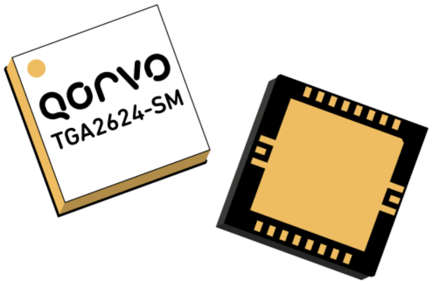
The TGA2624-SM is packaged in a 7 x 7 mm air-cavity, laminate based QFN. Both RF ports are internally DC blocked and matched to 50 ohms enabling simple system integration. Ideally suited for pulsed applications, the TGA2624-SM offers excellent power, PAE and gain performance that can save costs on existing platforms while enabling the development of future systems.

Functional Block Diagram



Applications

- Weather and Marine Radar



Product Features

- Frequency Range: 9–10 GHz
- P_{SAT}: 43 dBm @ P_{IN} = 18 dBm
- PAE: >40% @ P_{IN} = 18 dBm
- Power Gain: 25 dB @ P_{IN} = 18 dBm
- Bias: V_D = 28 V, I_{DQ} = 365 mA (Pulsed $V_{D:}$ PW = 100 us and DC = 10 %)
- Package Dimensions: 7 x 7 x 1.64 mm

Ordering Information

Part	Description
TGA2624-SM	9–10 GHz 20 W GaN Power Amplifier
TGA2624-SM EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Min Value	Max Value	Units
Drain Voltage (V_D)	-	40	V
Gate Voltage Range (V_G)	-8	0	V
Drain Current (I_D)	-	3.8	A
Gate Current (I_G)	See thermal section plot		
Power Dissipation (P_{DISS}), 85 °C, CW	-	44	W
Input Power (P_{IN}), Pulsed, 50 Ω, V_D = 28 V, 85 °C	-	25	dBm
Input Power (P_{IN}), Pulsed, VSWR 6:1, V_D = 28 V, 85 °C	-	19	dBm
Mounting Temperature (30 seconds)	-	260	°C
Storage Temperature	-55	150	°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied. Extended application of Absolute Maximum Rating conditions may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D): Pulsed		28		V
Drain Current (I_{DQ})		365		mA
Gate Voltage Range (V_G)	−2.8	-2.5	-2	V
Temperature (T_{BASE})	-40		85	°C

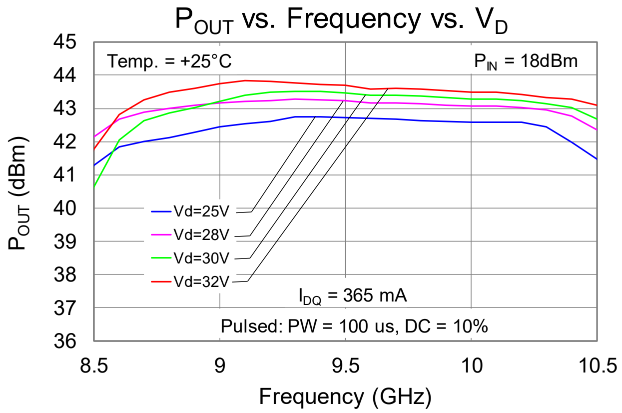
Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

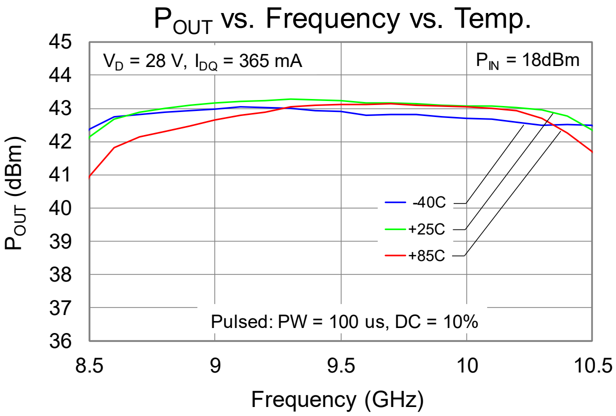
Electrical Specifications

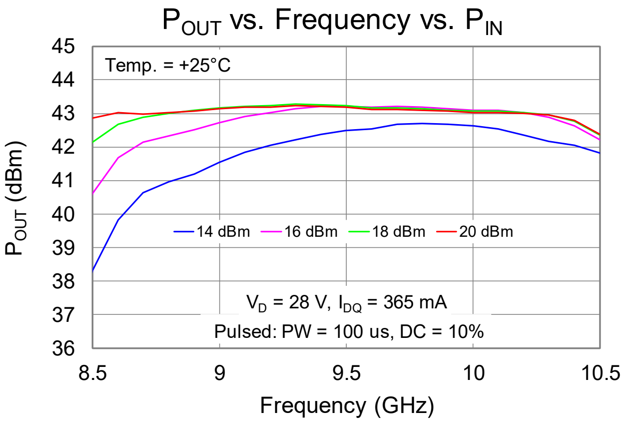
Test conditions unless otherwise noted: 25 °C, V_D = 28 V, I_{DQ} = 365 mA, Pulsed V_D: PW = 100 us, DC = 10 %

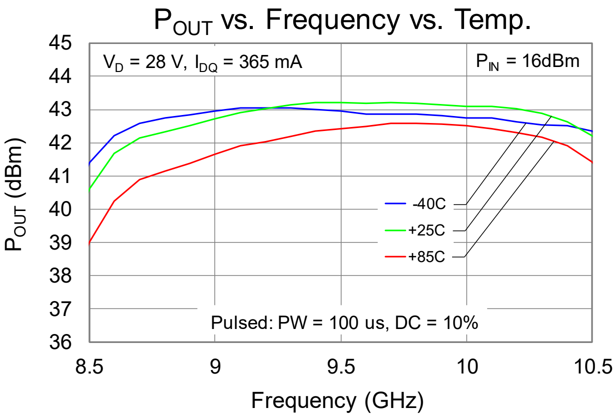
Parameter	Min	Typical	Max	Units
Operational Frequency Range	9		10	GHz
Small Signal Gain		>34		dB
Input Return Loss		>9		dB
Output Return Loss		>8.5		dB
Output Power (P_{IN} = 18 dBm)	42	43		dBm
Power Added Efficiency (P_{IN} = 18 dBm)	30	>40		%
Power Gain (P_{IN} = 18 dBm)		25		dB
Output Power Temperature Coefficient From 25 °C to 85 °C (P_{IN} = 18 dBm)		-0.02		dBm/°C
Recommended Operating Voltage:	20	28	32	V
Gate Leakage (V_D = 10 V, V_G = −3.7 V)	−8.3			mA

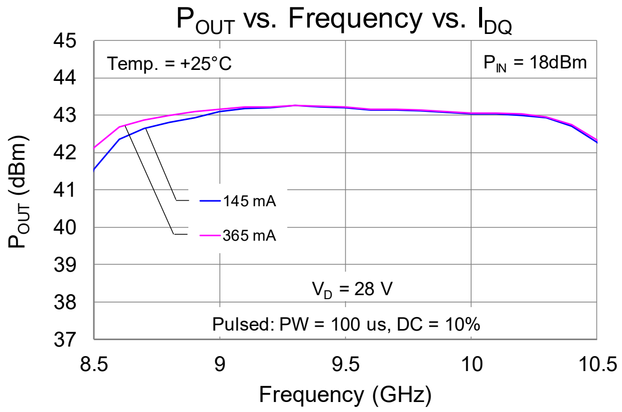
Typical Performance: Large Signal (Pulsed Operation)

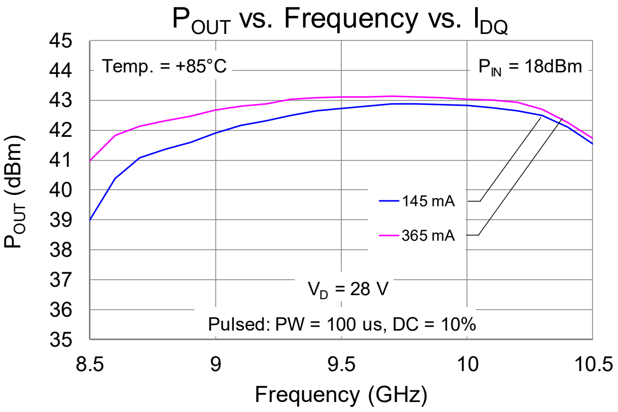




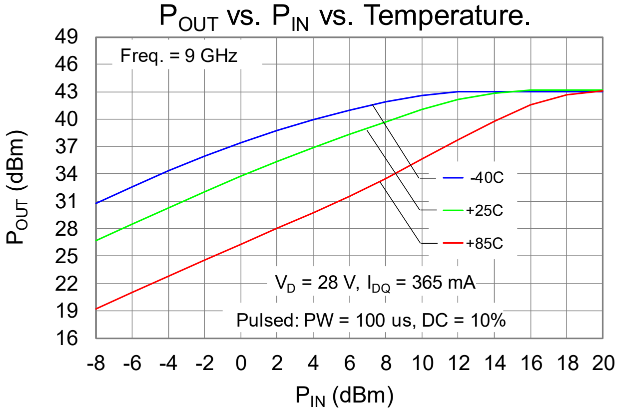


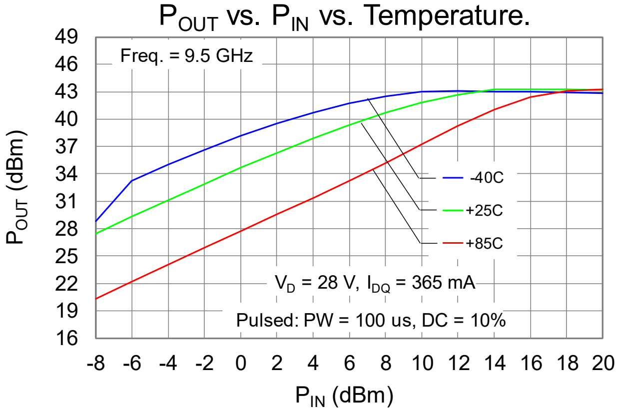


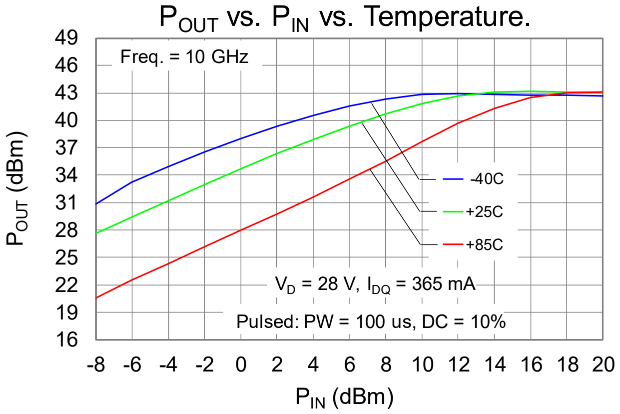


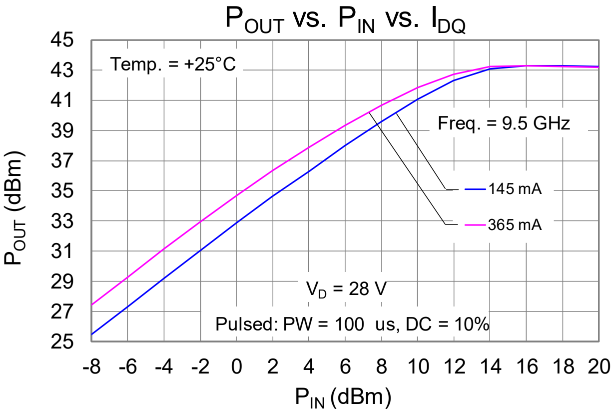


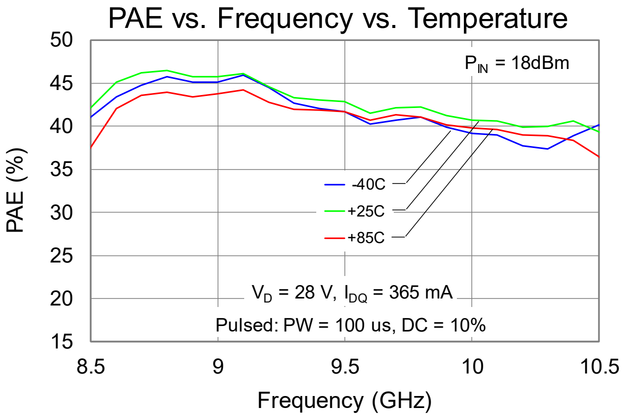
Typical Performance: Large Signal (Pulsed Operation)

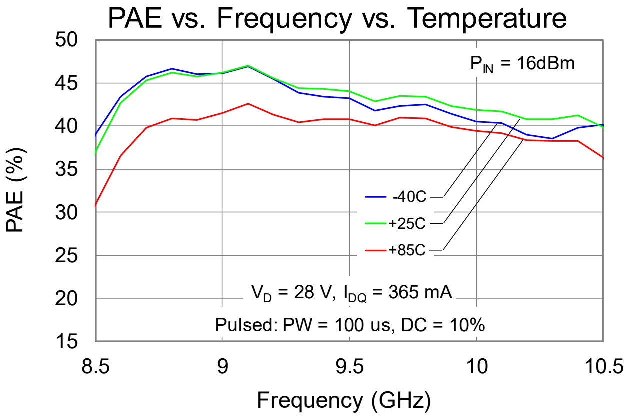

P_{OUT} vs. P_{IN} vs. Temperature.


P_{OUT} vs. P_{IN} vs. Temperature.


P_{OUT} vs. P_{IN} vs. Temperature.

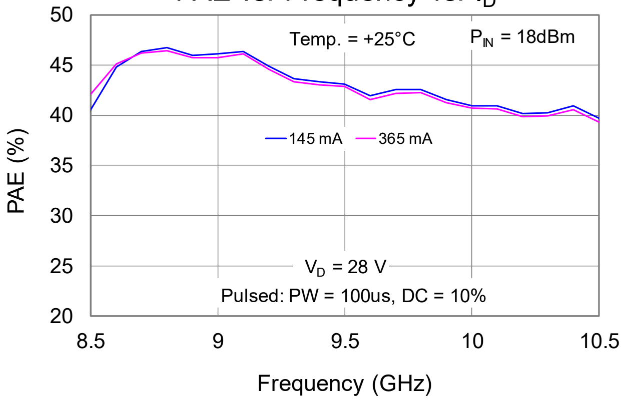

P_{OUT} vs. P_{IN} vs. I_{DQ}


PAE vs. Frequency vs. Temperature

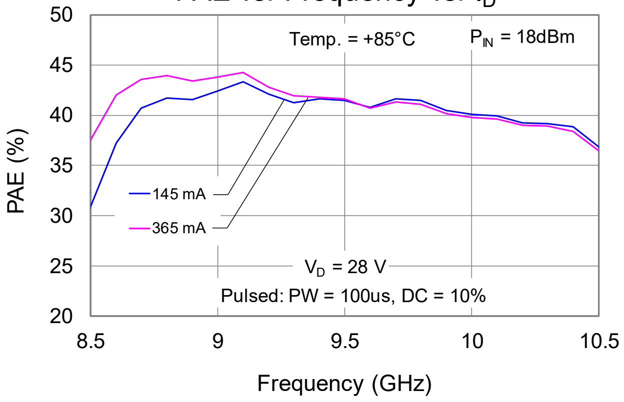

PAE vs. Frequency vs. Temperature

Typical Performance: Large Signal (Pulsed Operation)

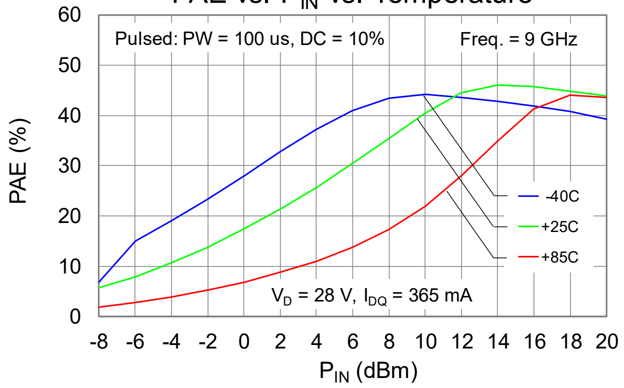
PAE vs. Frequency vs. I_D



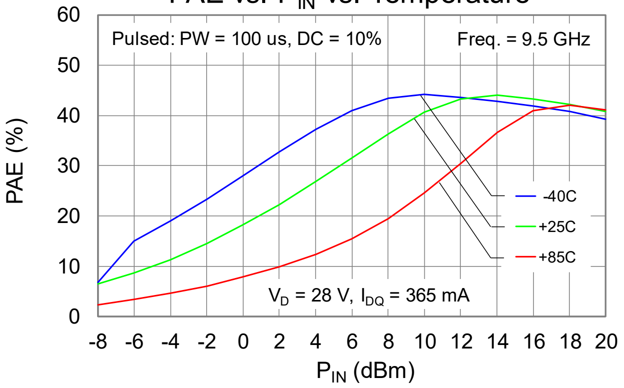
PAE vs. Frequency vs. I_D



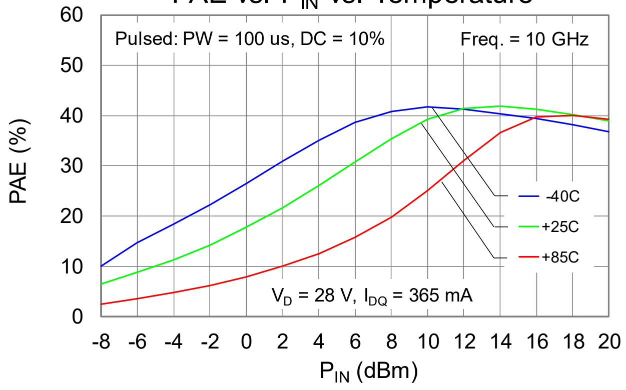
PAE vs. P_{IN} vs. Temperature



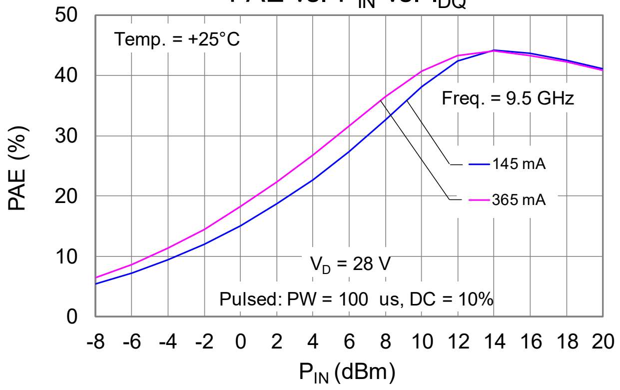
PAE vs. P_{IN} vs. Temperature



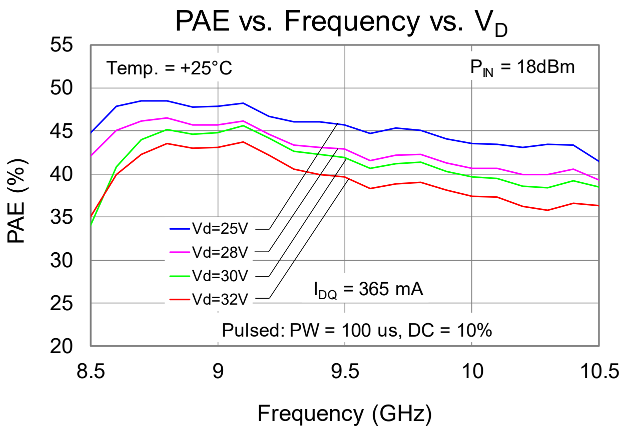
PAE vs. P_{IN} vs. Temperature

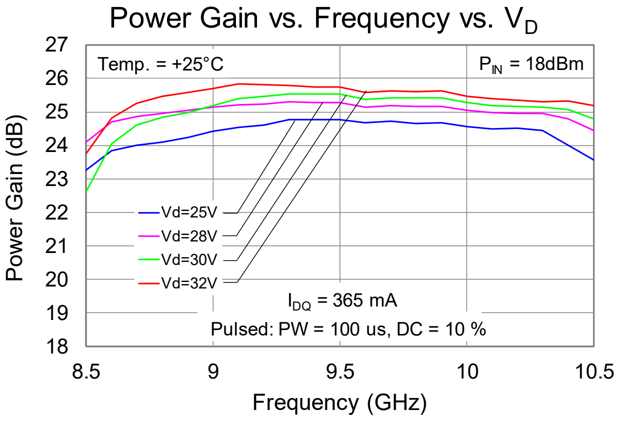


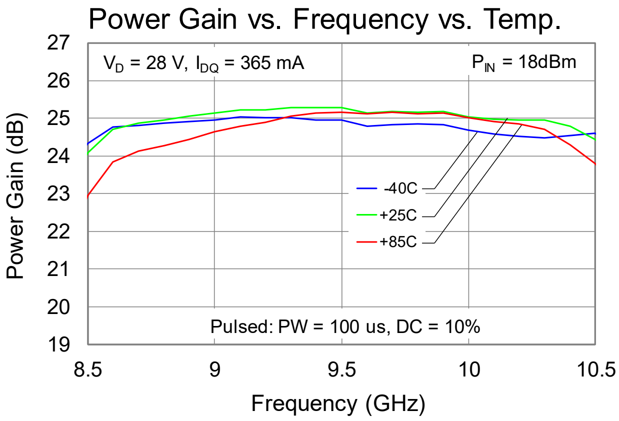
PAE vs. P_{IN} vs. I_{DQ}

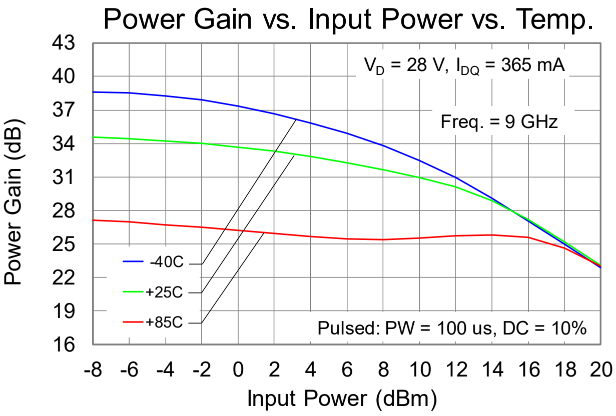


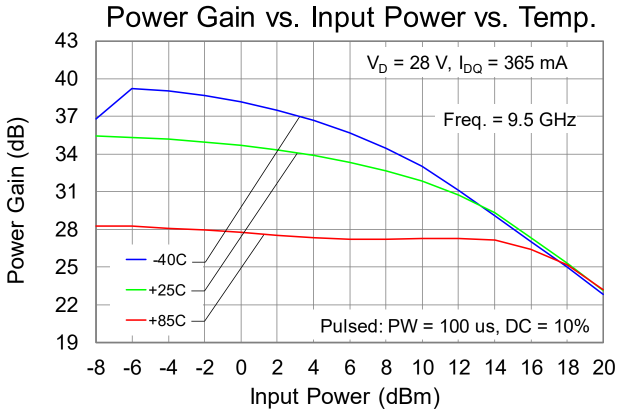
Typical Performance: Large Signal (Pulsed Operation)

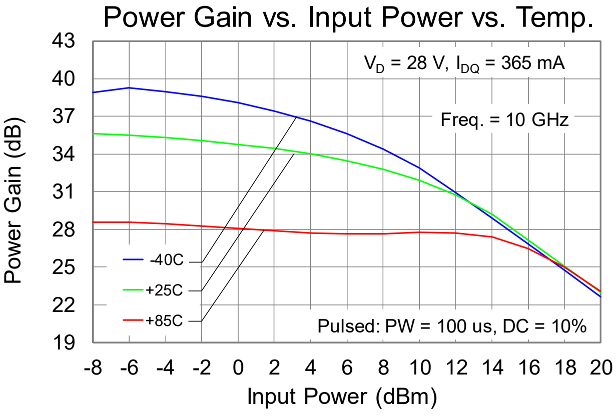

PAE vs. Frequency vs. V_D


Power Gain vs. Frequency vs. V_D

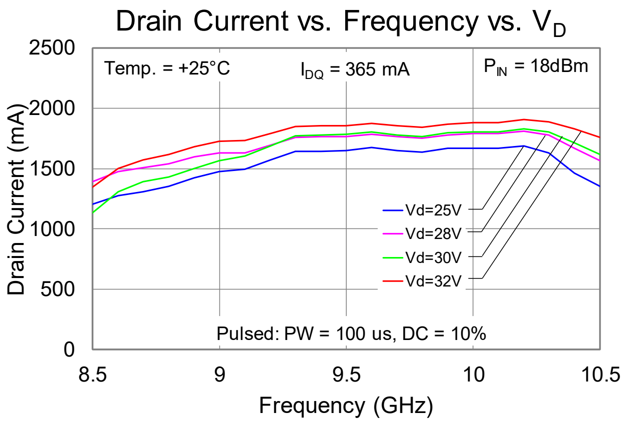

Power Gain vs. Frequency vs. Temp.

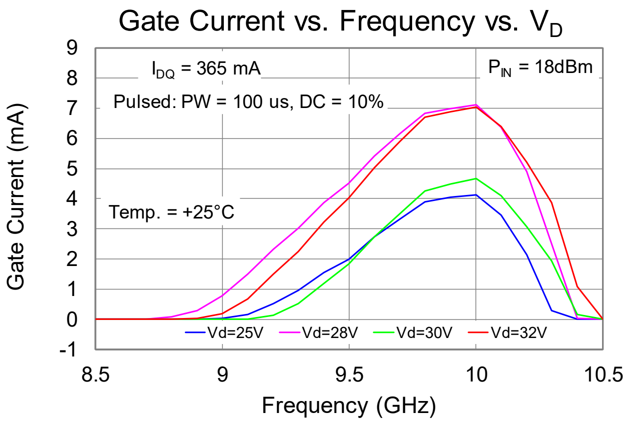

Power Gain vs. Input Power vs. Temp.

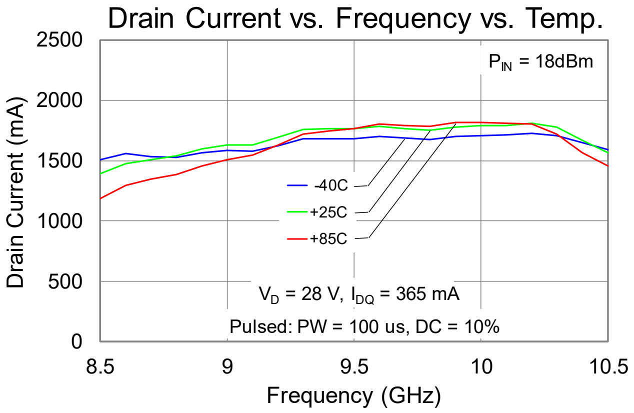

Power Gain vs. Input Power vs. Temp.

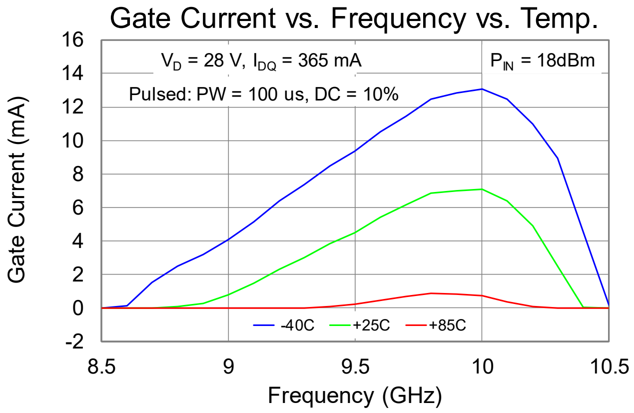

Power Gain vs. Input Power vs. Temp.

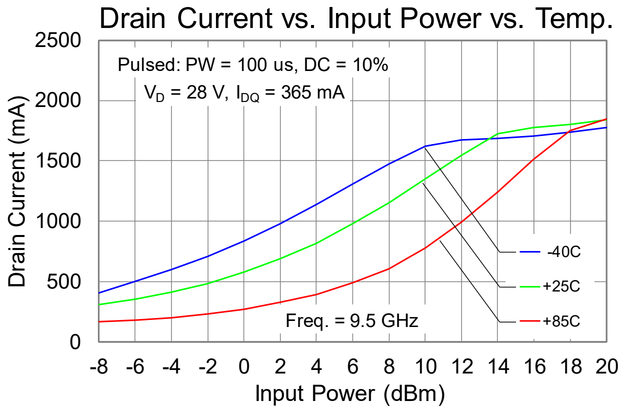
Typical Performance: Large Signal (Pulsed Operation)

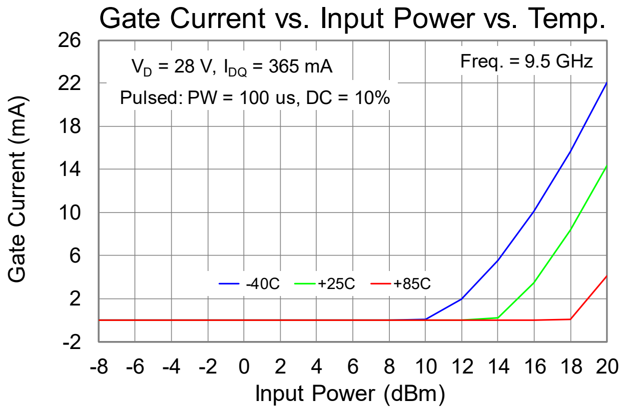

Drain Current vs. Frequency vs. V_D


Gate Current vs. Frequency vs. V_D

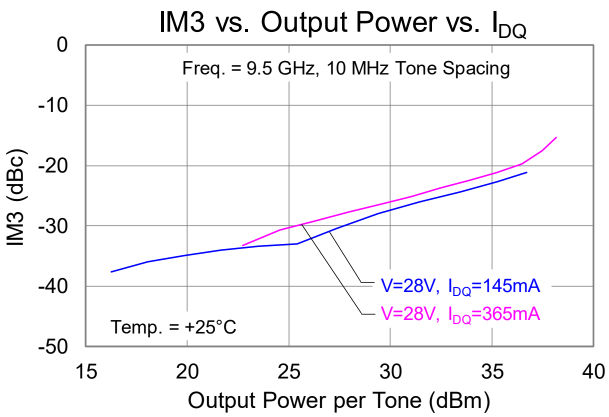

Drain Current vs. Frequency vs. Temp.

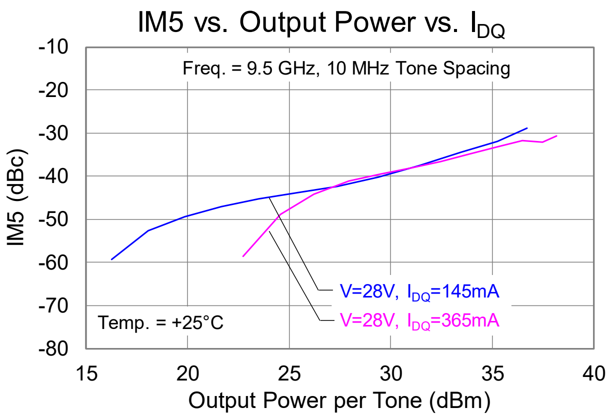

Gate Current vs. Frequency vs. Temp.

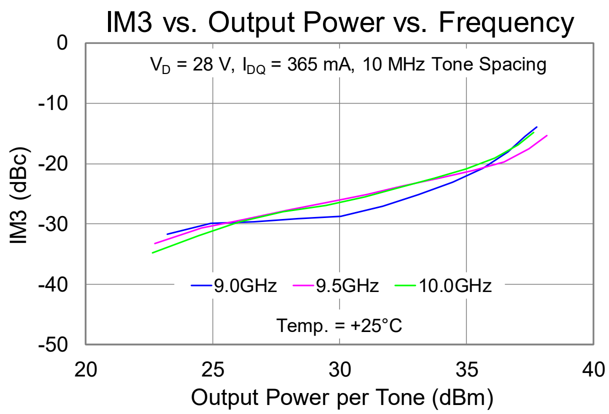

Drain Current vs. Input Power vs. Temp.

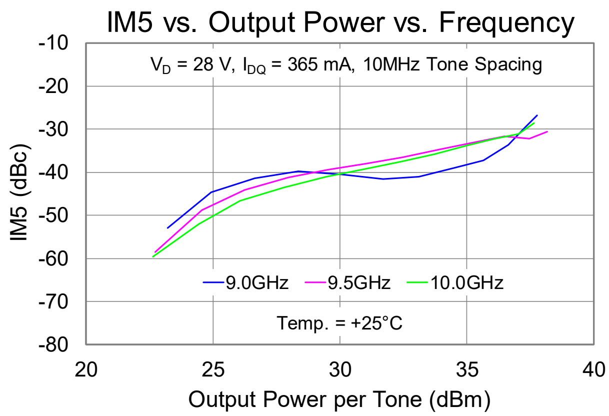

Gate Current vs. Input Power vs. Temp.

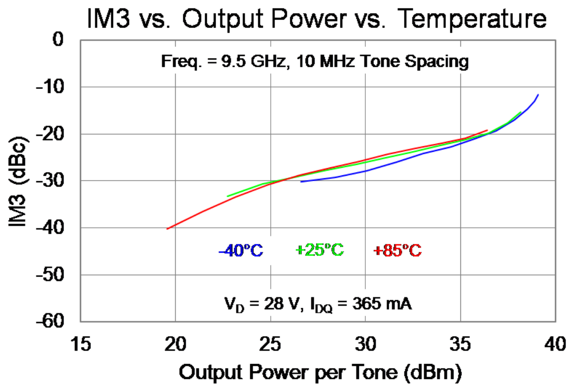
Typical Performance: Linearity (CW Operation)

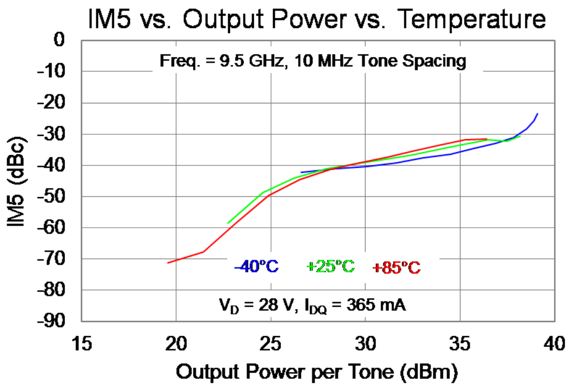




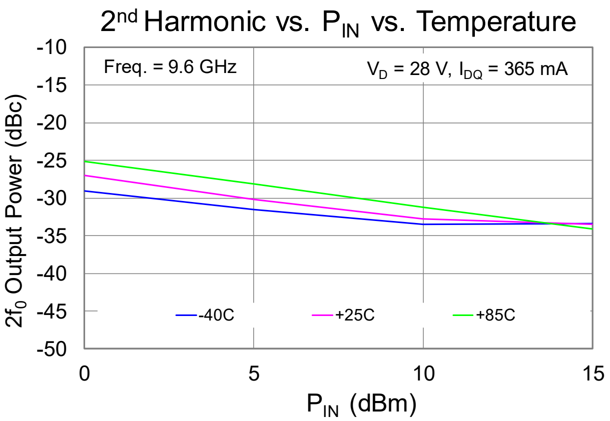


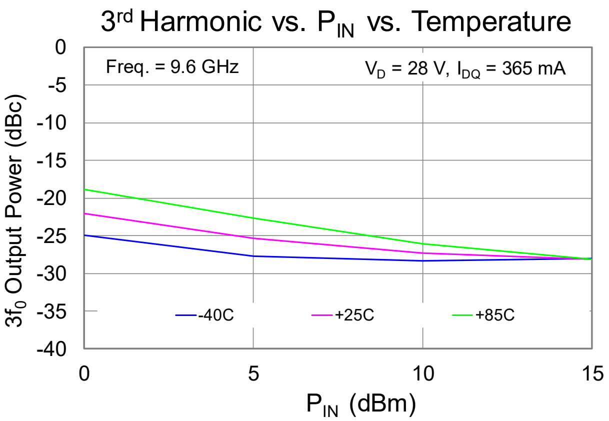


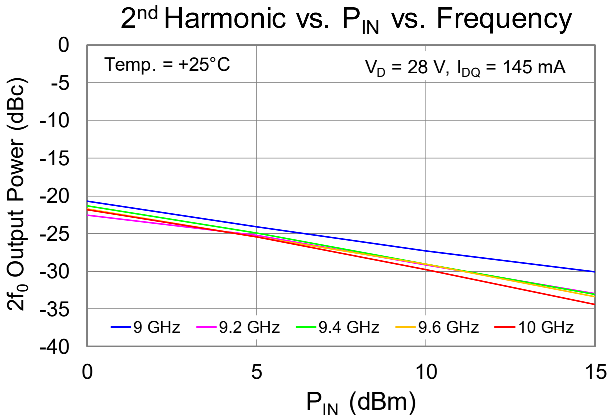


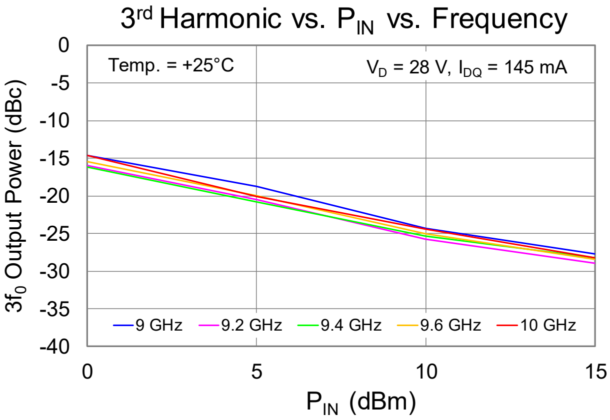


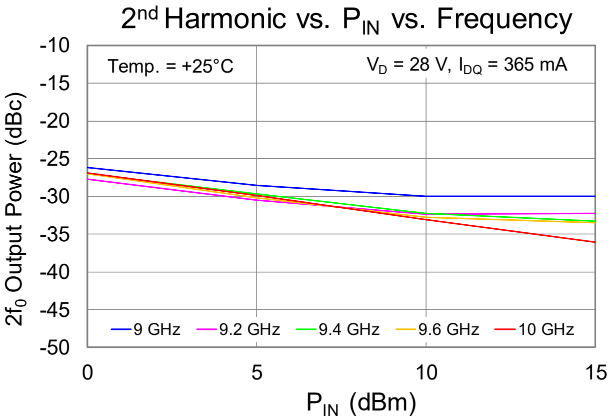
Typical Performance: Linearity (CW Operation)

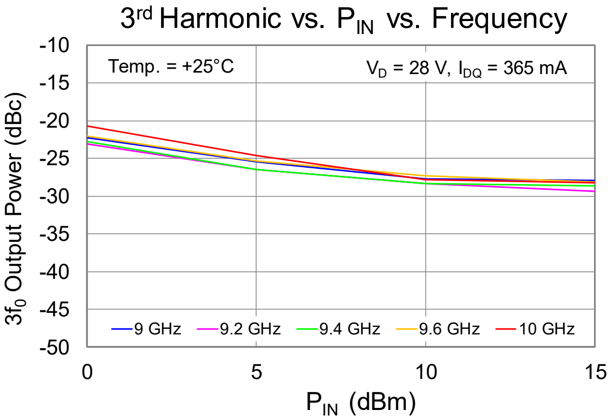




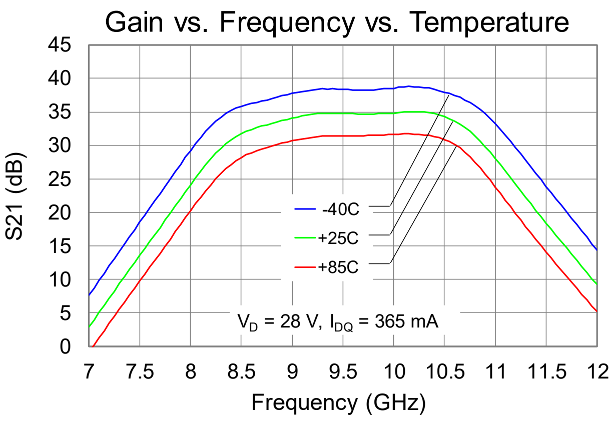


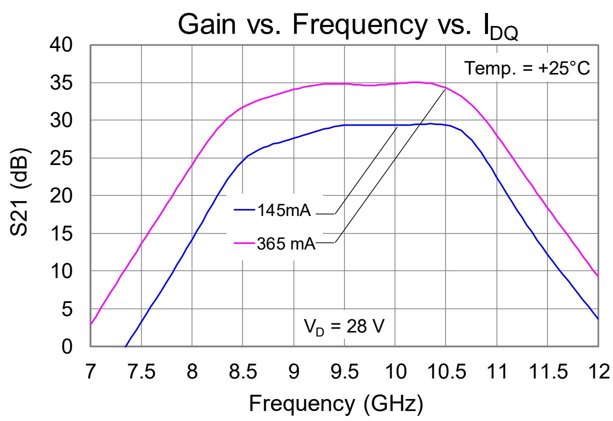


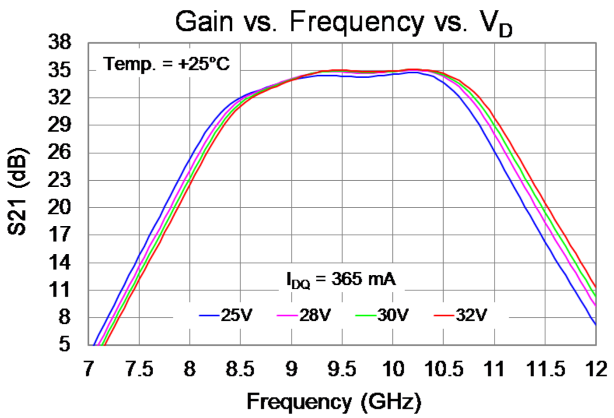


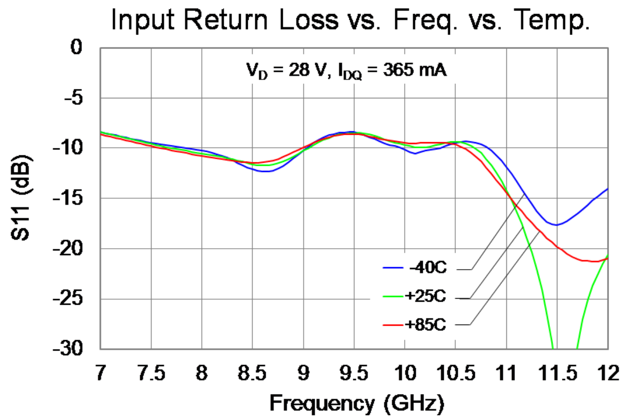


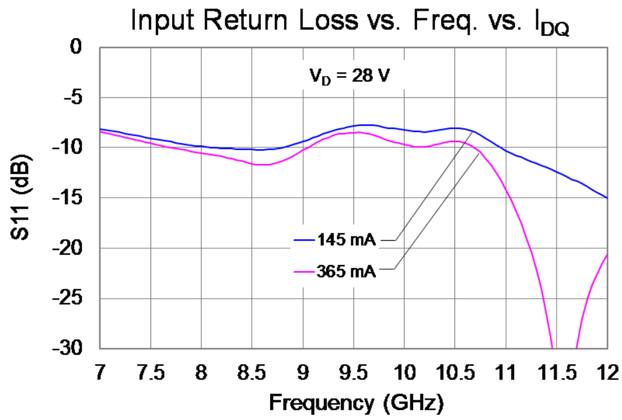
Typical Performance: Small Signal (CW Operation)


Gain vs. Frequency vs. Temperature


Gain vs. Frequency vs. I_{DQ}


Gain vs. Frequency vs. V_D


Input Return Loss vs. Freq. vs. Temp.


Input Return Loss vs. Freq. vs. I_{DQ}

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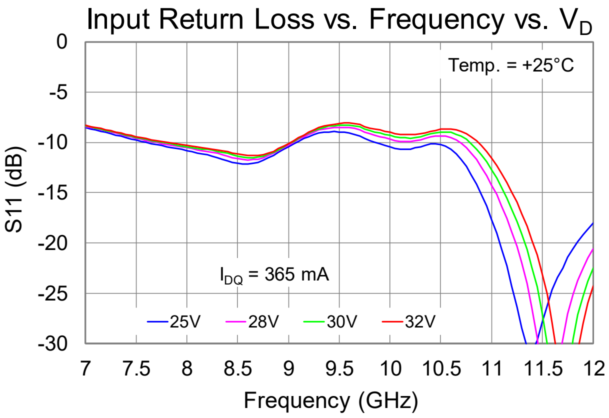
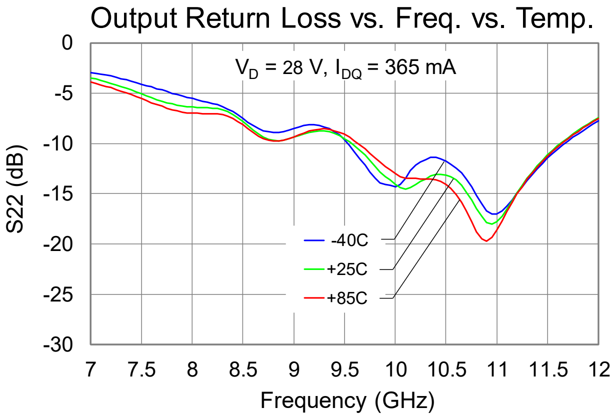
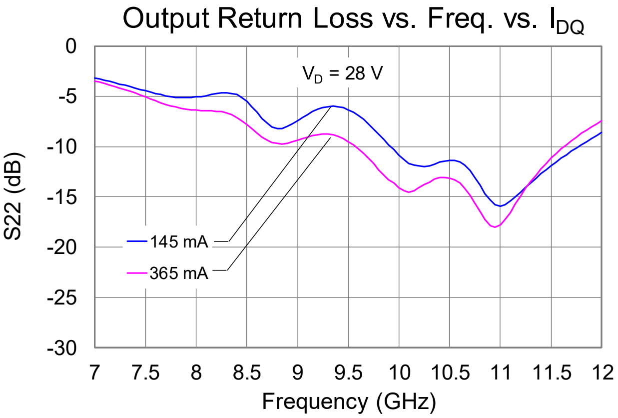
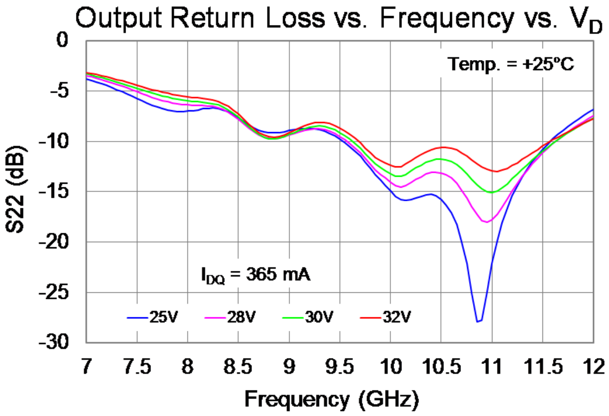








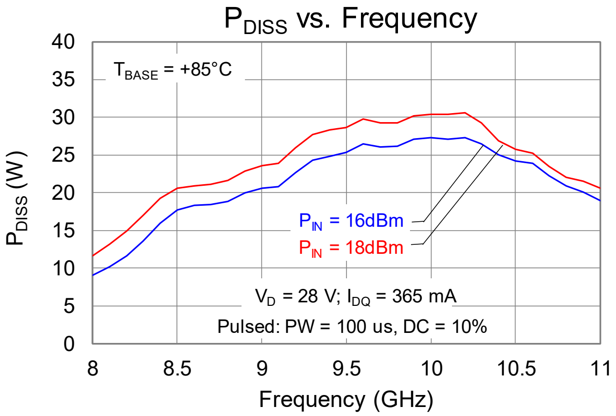
Thermal and Reliability Information

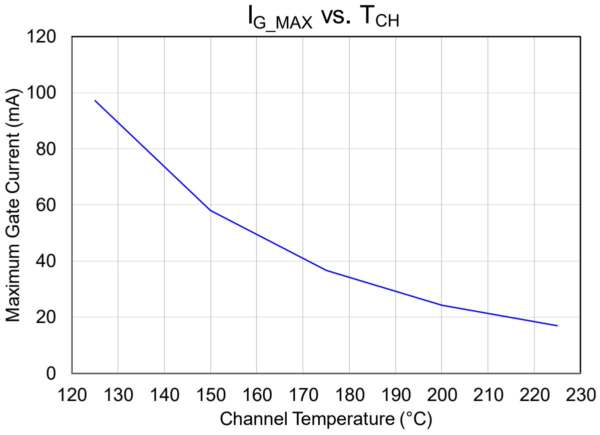
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) [1]	T_{BASE} = 85 °C; V_D = 28 V, I_{DQ} = 365 mA, (Quiescnent or small signal applications), P_{DISS} = 10.22 W	1.31	°C/W
Channel Temperature (T_{CH}) (Small Signal) [2]		98.4	°C
Thermal Resistance (θ_{JC}) [1]	T_{BASE} = 85 °C;, V_D = 28 V, I_{DQ} = 365 mA, (Pulsed V_D : PW = 100 us, DC = 10 %), I_{D_Drive} = 1.8 A, P_{IN} = 18 dBm, P_{OUT} = 43 dBm, P_{DISS} = 30 W	1.46	°C/W
Channel Temperature (T_{CH}) (Under RF drive) [2]		128.9	°C
Thermal Resistance (θ_{JC}) [1]	T_{BASE} = 85 °C;, V_D = 28 V, I_{DQ} = 365 mA, (CW), I_{D_Drive} = 1.8 A, P_{IN} = 18 dBm, P_{OUT} = 43 dBm, P_{DISS} = 30 W	2.56	°C/W
Channel Temperature (T_{CH}) (Under RF drive) [2]		161.7	°C

Notes:

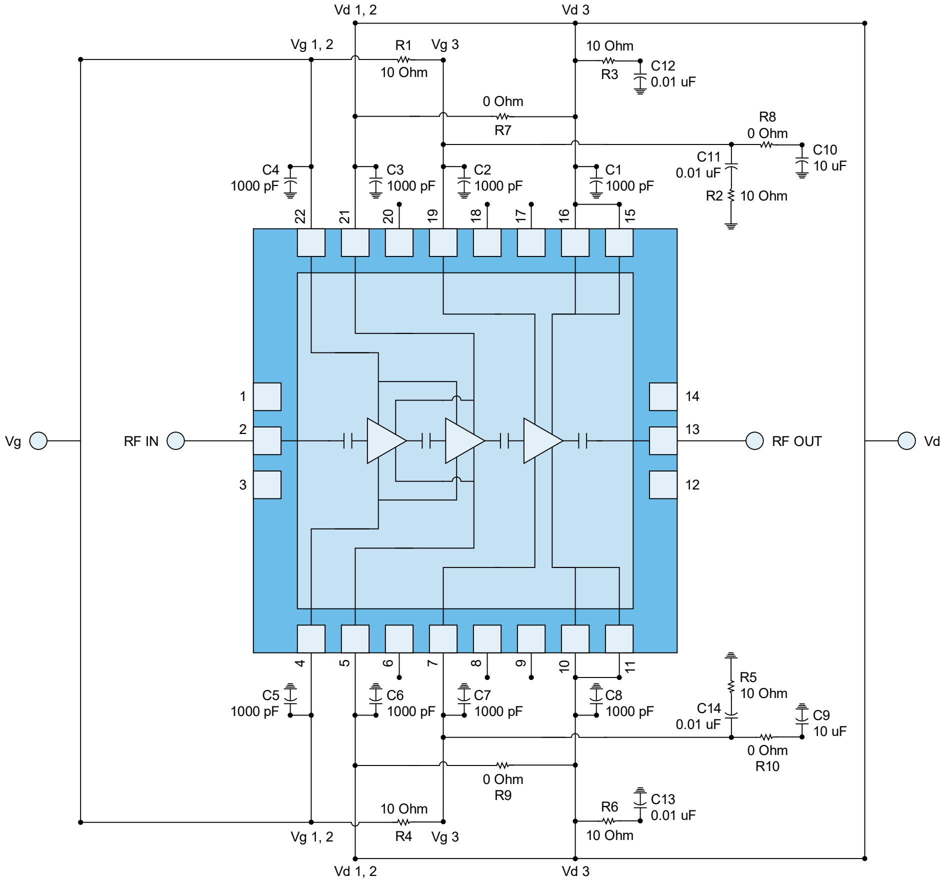
1. Thermal Resistance is referenced to the back of package.
2. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

Power Dissipation and Maximum Gate Current





Application Information



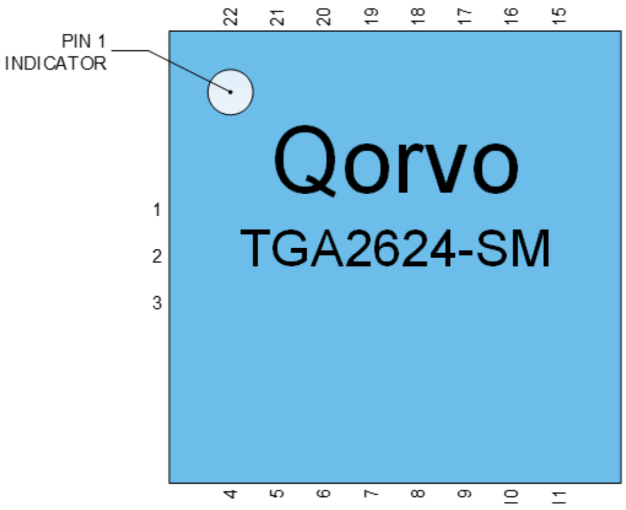
Notes:

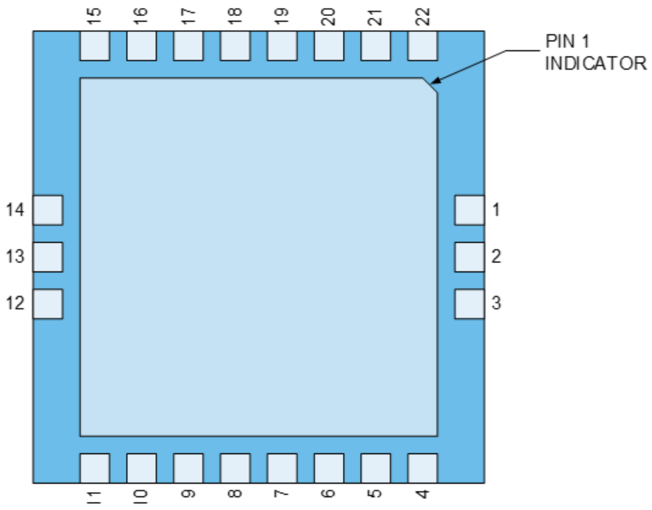
1. $V_{G:}$ must be biased from both sides - $V_{G1,2}$ & V_{G3} can be tied together.
2. V_D: must be biased from both sides - $V_{D1,2}$ & V_{D3} can be tied together.

Bias-up Procedure
Set I_D limit to 2 A, I_G limit to 25 mA
Apply -5.0 V to V_G (for pinch-off)
Increase V_D to +28 V; Ensure I_{DQ} is approx. 0 mA
Adjust V_G more positive until I_{DQ} = 365 mA V_G ~ -2.5 V typ
Apply RF signal

Bias-down Procedure
Turn off RF signal
Reduce V_G to −5 V; ensure I_{DQ} is approx. 0 mA
Set V_D to 0 V
Turn off V_D supply
Turn off V_G supply

Pin Layout

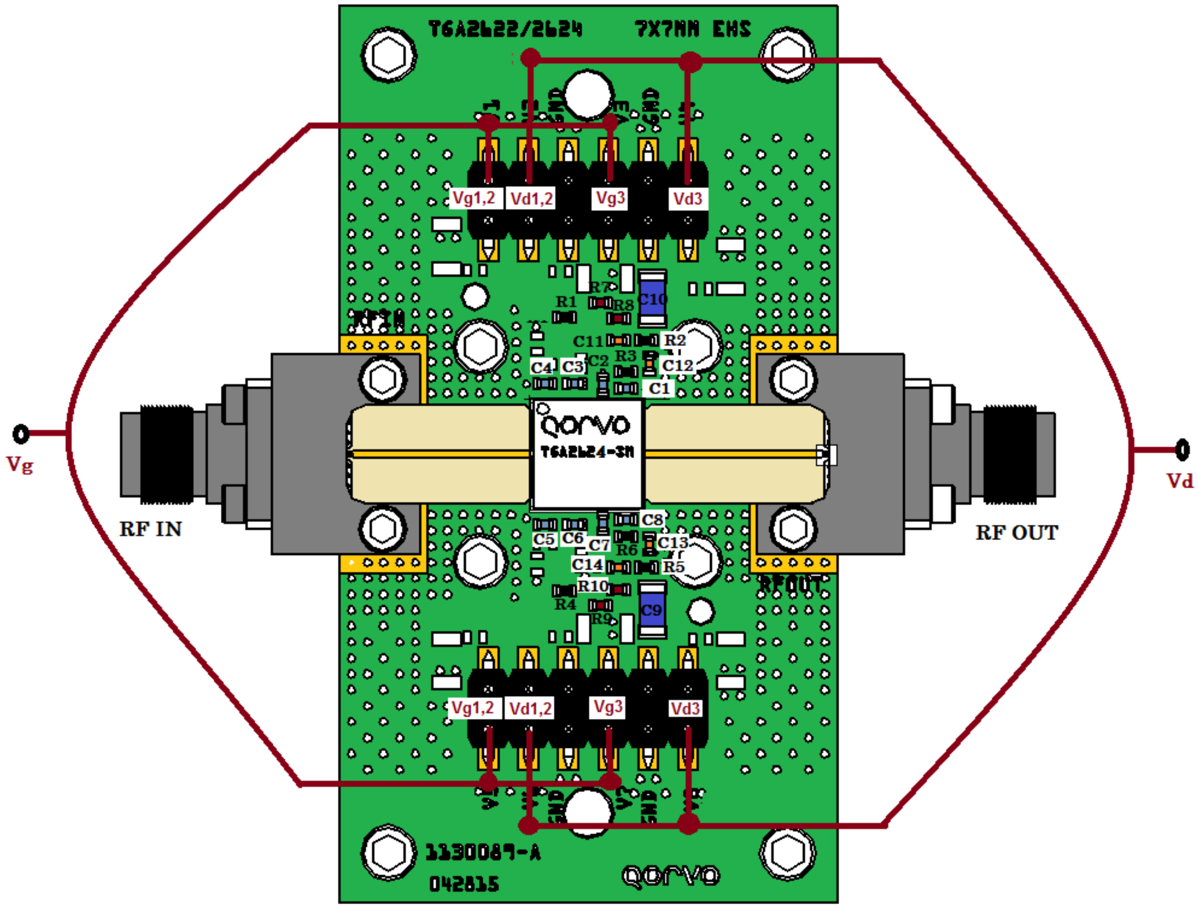




Pin Description

Pin No.	Symbol	Description
1, 3, 12, 14	GND	Must be grounded on the PCB
2	RF_{IN}	Input; matched to 50 Ω; DC blocked
4, 22	$V_{G1,2}$	Gate Voltages 1,2; Bias network is required; must be biased from both sides; see recommended Application Information on page 13.
5, 21	$V_{D1,2}$	Drain voltages 1,2; Bias network is required; must be biased from both sides; see recommended Application Information on page 13.
6, 8, 9, 17, 18, 20	N/C	No internal connection
7, 19	V_{G3}	Gate Voltage 3; Bias network is required; must be biased from both sides; see recommended Application Information on page 13.
10, 11, 15, 16	V_{D3}	Drain voltage 3; Bias network is required; must be biased from both sides; see recommended Application Information on page 13.
13	RF_{OUT}	Output; matched to 50 Ω; DC blocked

Evaluation Board Layout



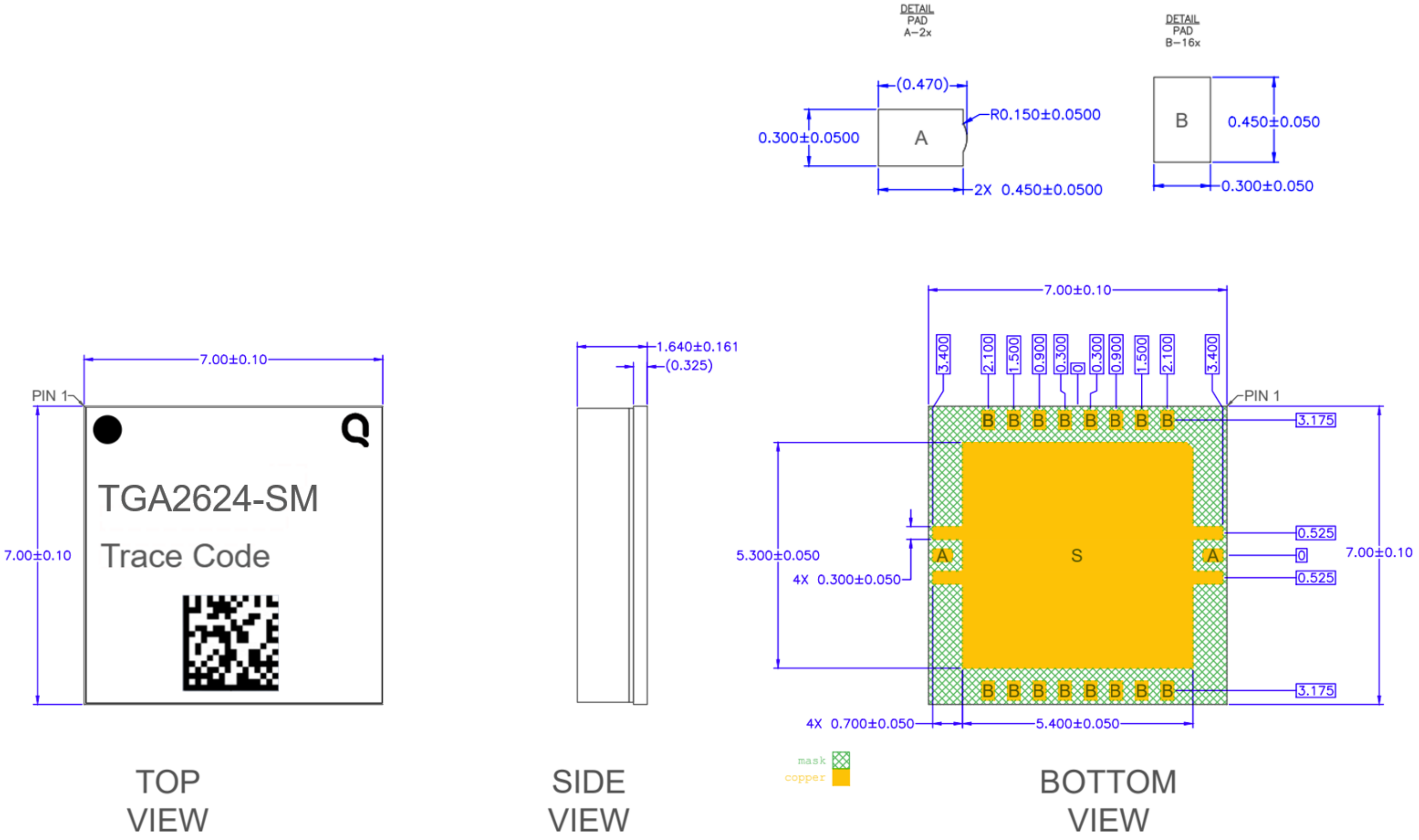
Notes:

1. Both Top and Bottom V_D and V_G must be biased

Bill of Material

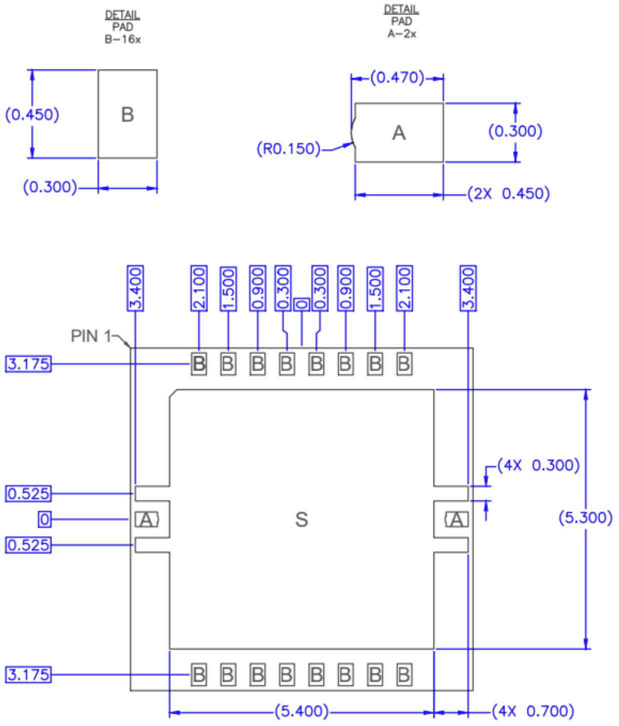
Reference Design	Value	Description	Manufacture	Part-Number
C1–C8	1000 pF	Cap, 0402, 100 V, 10%, X7R	Various	
C9–C10	10 µF	Cap, 1206, 50 V, 20%, X5R	Various	
C11–C14	0.01 µF	Cap, 0402, 50 V, 10%, X7R	Various	
R1–R6	10 ohms	Res, 0402, 50 V, 5%, SMD	Various	
R7–R10	0 ohms	Res, 0402, jumpers required for the above EVB	Various	

Mechanical Information

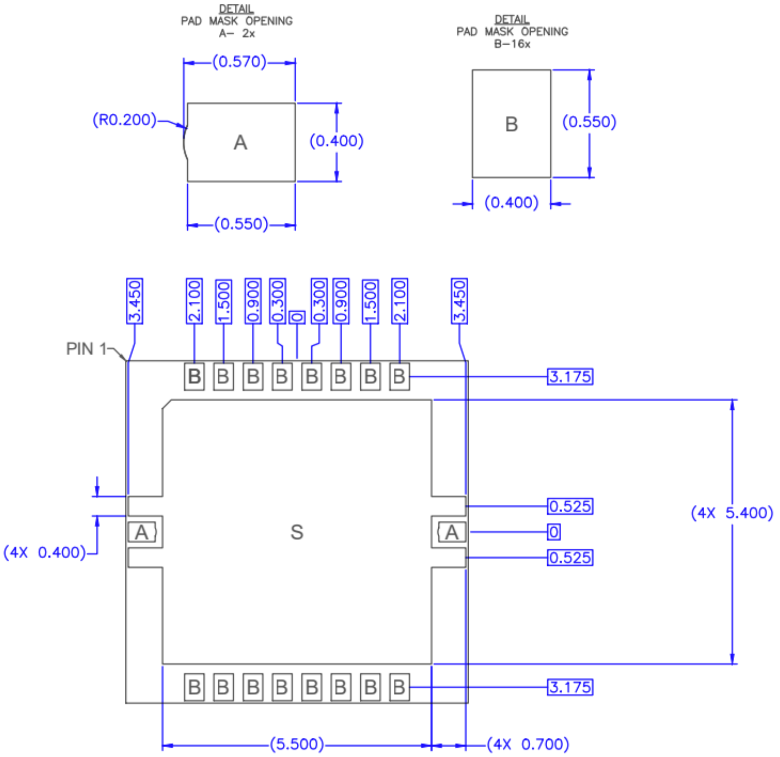


Units: Millimeters (mm)
Tolerances: unless specified: x.xx = ± 0.25; x.xxx = ± 0.100
Materials: Base: Laminate Substrate
Lid: Laminate
All metalized features are gold plated
Part is epoxy sealed
2DID Marking can be used to trace part manufacturing information

Application PCB Land Pattern and Masks



Recommended Land Pattern



Recommended Land Pattern Mask

Units: Millimeters (mm)
Tolerances: unless specified: x.xx = ± 0.25; x.xxx = ± 0.100

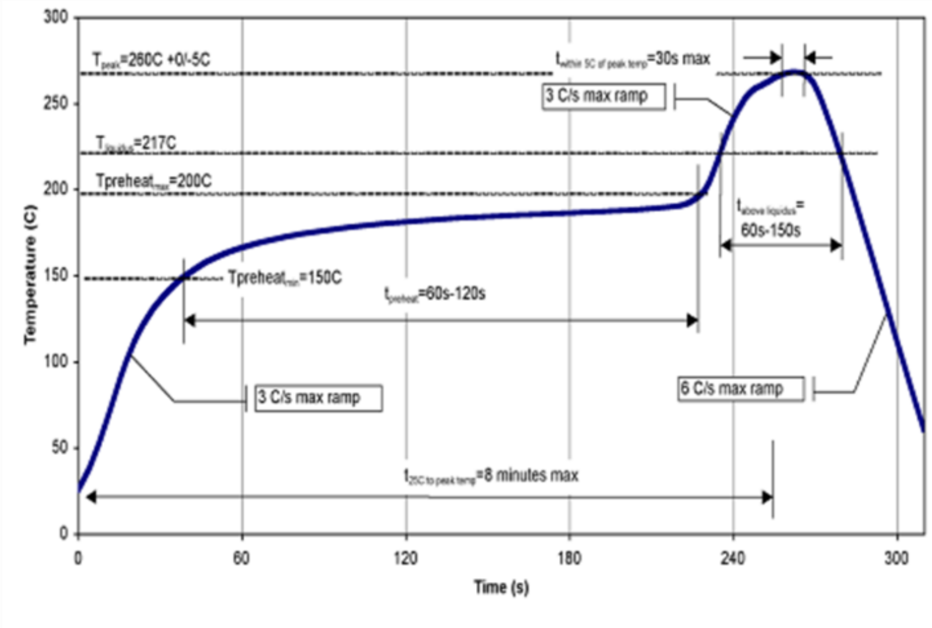
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au.

Solder rework not recommended.



Recommended Soldering Temperature Profile

Handling Precautions

Parameter	Rating	Standard
ESD-Human Body Model (HBM)	1A	JEDEC/JESD22-A114
MSL-Moisture Sensitivity Level	MSL3	JEDEC/IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations.

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notices

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