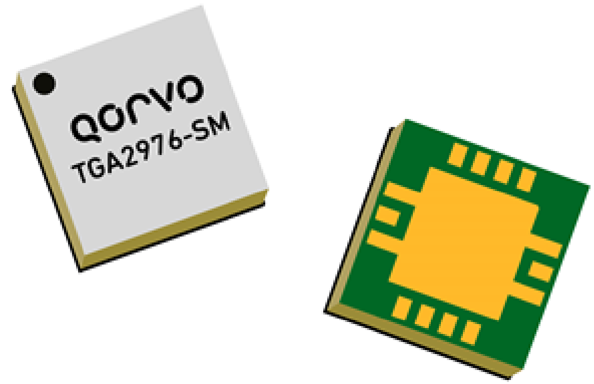
TGA2976-SM

0.1 – 3.0 GHz 10W GaN Power Amplifier

Product Overview

Qorvo's TGA2976-SM is a wideband cascode amplifier fabricated on Qorvo's production 0.25um GaN on SiC process. The cascode configuration offers exceptional wideband performance as well as supporting 40 V operation. The TGA2976-SM operates from 0.1 - 3.0 GHz and provides greater than 10 W of saturated output power with greater than 13 dB of large signal gain and greater than 38% power-added efficiency.

The TGA2976-SM is available in a low-cost, surface mount 14 lead 4x4 Air Cavity laminate package. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2976-SM is fully matched to 50 Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

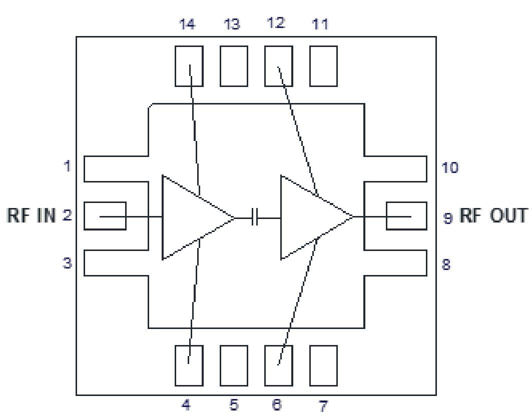


AC-QFN 4x4 mm 14L

Key Features

- Frequency Range: 0.1 – 3.0 GHz
- PSAT: >40 dBm at P_{IN} = 27 dBm
- PAE: 48% @ mid-band
- Large Signal Gain: >13 dB
- Small Signal Gain: >20 dB
- Bias: V_D = 40 V, I_{DQ} = 360 mA
- Wideband Flat Gain and Power
- Package Dimensions: 4.0 x 4.0 x 1.80 mm

Functional Block Diagram



Top View

Applications

- Commercial and military radar
- Communications
- Electronic Warfare

Ordering Information

Part No.	Description
TGA2976-SM	0.1-3.0 GHz 10 W GaN Power Amplifier
TGA2976-SM EVB	TGA2976-SM Evaluation Board

Absolute Maximum Ratings

Parameter	Min	Max	Units
Drain Voltage (V_D)	-	80	V
Gate Voltage Range (V_{G1})	-8	0	V
Gate Voltage Range (V_{G2}, values should be V_D / 2 + V_{G1})	0	40	V
Drain Current (I_D)	-	760	mA
Gate Current (I_{G1}, I_{G2})	See plots in page 3		
Power Dissipation (P_{DISS}), 85°C	-	28	W
Input Power (P_{IN}), CW, 50 Ω, 85°C,	-	33	dBm
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 40V, 85°C	-	33	dBm
Mounting Temperature	-	260	°C
Storage Temperature	-55	150	°C

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Drain Voltage (V_D)		40		V
Drain Current (I_{DQ})		360		mA
Gate Voltage Range (V_{G1})	-2.8	−2.5	-2.0	V
Gate Voltage (V_{G2})		17.7		V

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		0.1		3.0	GHz
Small Signal Gain			> 20		dB
Input Return Loss			> 5		dB
Output Return Loss			> 9		dB
Output Power	P_{IN} = 27 dBm		> 40		dBm
Power Added Efficiency	P_{IN} = 27 dBm, mid-band		48		%
3rd Order Intermodulation	120 mA, P_{OUT}/tone = 28 dBm		-30		dBc
5th Order Intermodulation	120 mA, P_{OUT}/tone = 28 dBm		-38		dBc
Small Signal Gain Temperature Coefficient			-0.03		dB/°C
Output Power Temperature Coefficient			-0.009		dBm/°C
Recommended Operating Voltage			40	50	V

Notes:

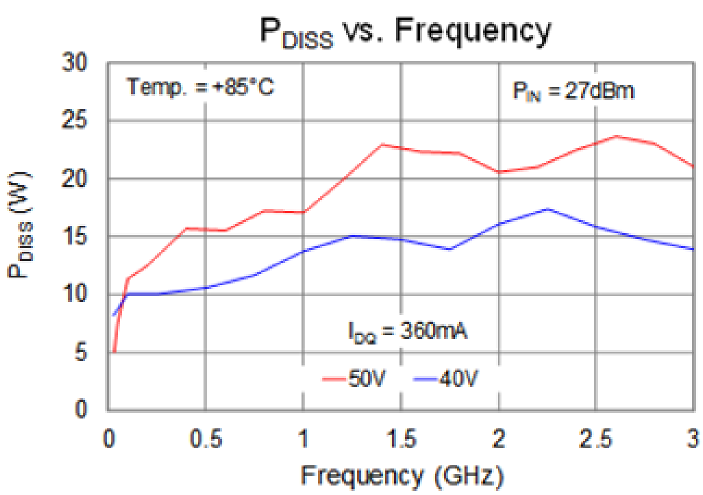
1. Test conditions unless otherwise noted: 25°C , V_D = 40 V, I_{DQ} = 360 mA, V_{G1} varies, V_{G2} = +17.7 V
2. Test data used EVB with external bias tee (not onboard surface mount components, refer to page 11 for difference.

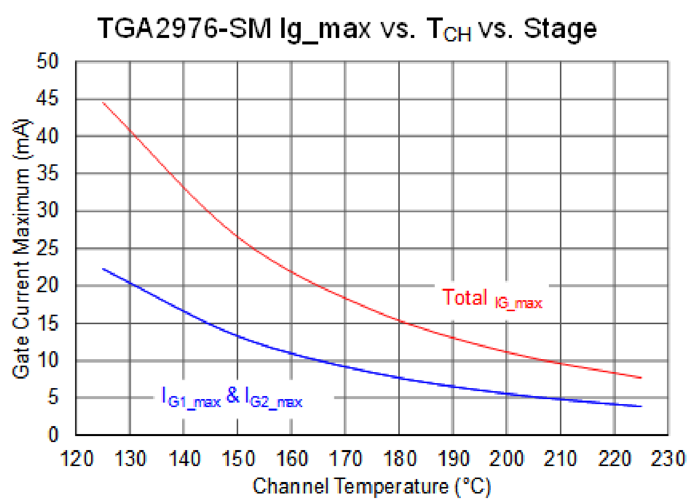
Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D(2) = 40 V (CW), I_{DQ} = 360 mA, Freq = 2.25 GHz, I_{D_Drive} = 655 mA, P_{IN} = 27 dBm, P_{OUT} = 39.7 dBm, P_{DISS} = 17.4 W	3.4	ºC/W
Channel Temperature, T_{CH} (Under RF) 3		144.0	°C
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85 °C, V_D(2) = 50 V (CW), I_{DQ} = 360 mA, Freq = 2.6 GHz, I_{D_Drive} = 665 mA, P_{IN} = 27 dBm, P_{OUT} = 40.1 dBm, P_{DISS} = 23.6 W	3.5	ºC/W
Channel Temperature, T_{CH} (Under RF) 3		167.0	°C

Notes:
1. Thermal resistance measured at back of package.
2. The drain voltage for Cascode amplifier transistor is ½ of V_D
3. IR scan equivalent. Refer to the following document: GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

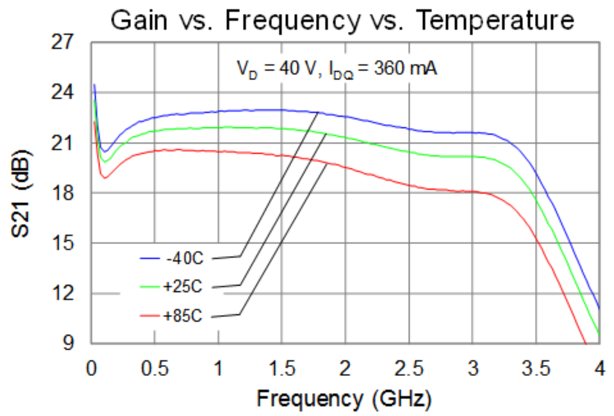
Power Dissipation and Maximum Gate Current

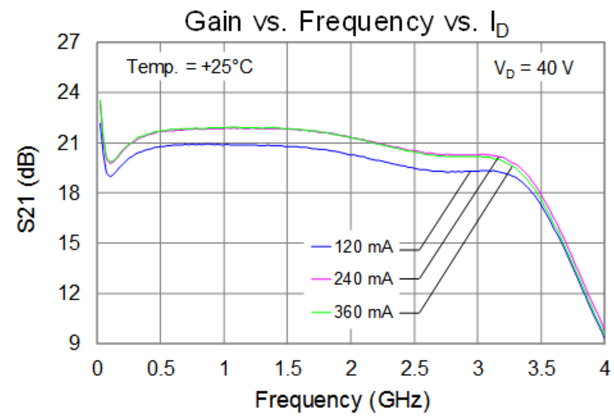


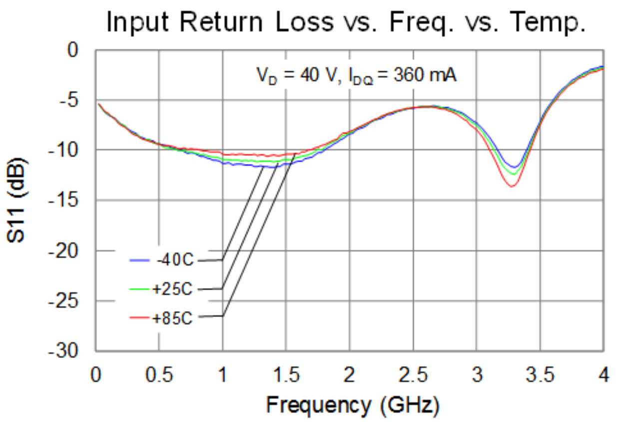


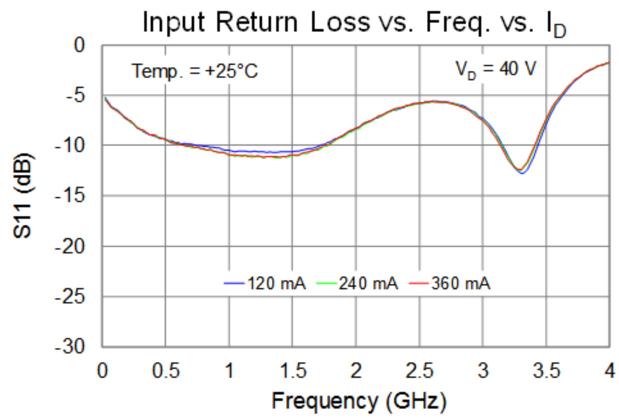
Performance Plots – Small Signal

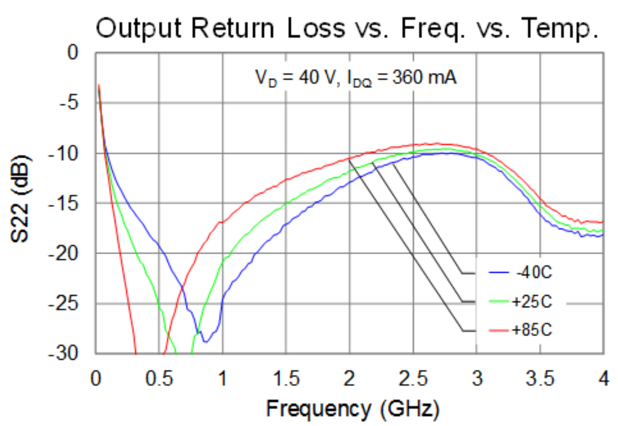
The plots reflect performance measured with an external coaxial bias tee and DC blocks

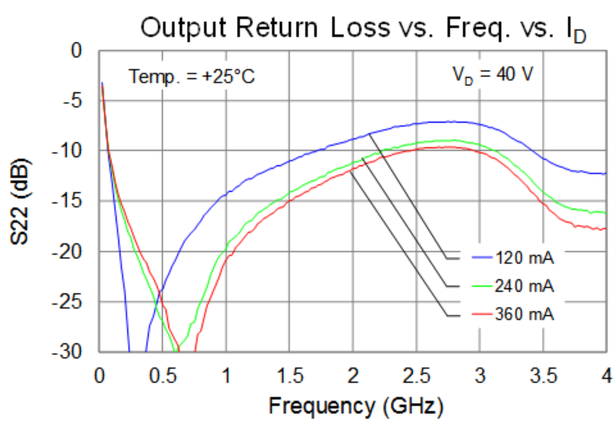












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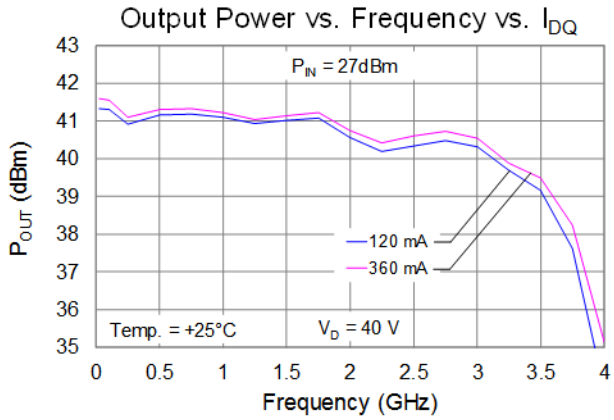
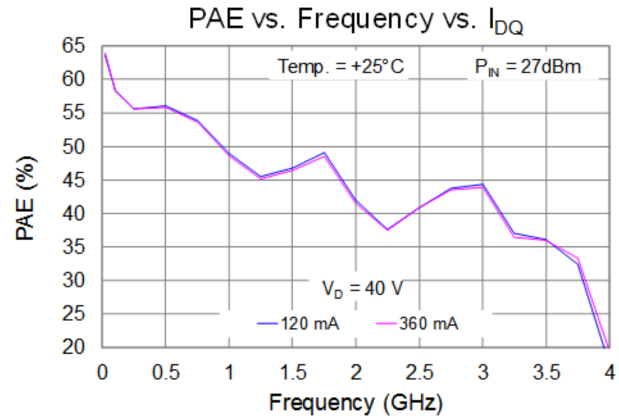
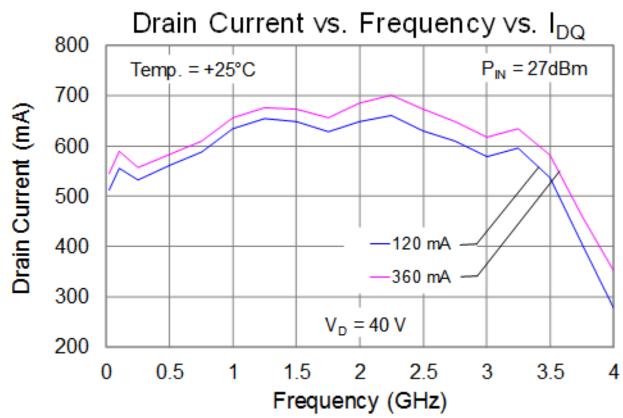
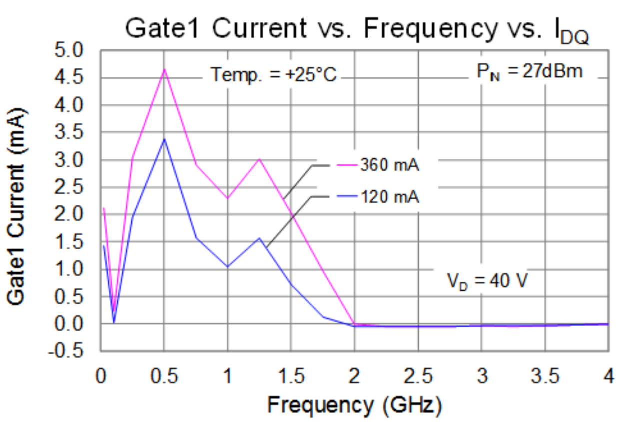
Performance Plots – Small Signal

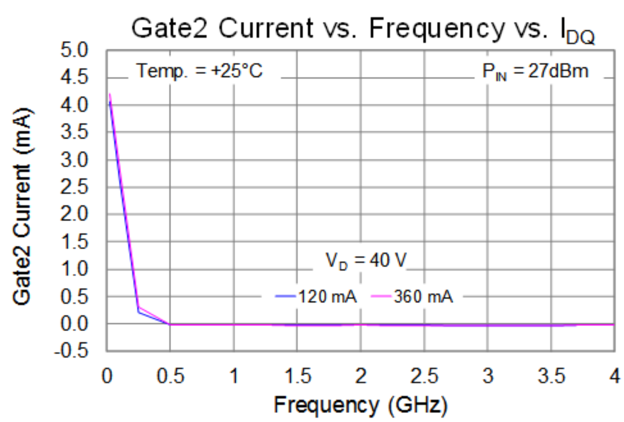
The plots reflect performance measured with an external coaxial bias tee and DC blocks





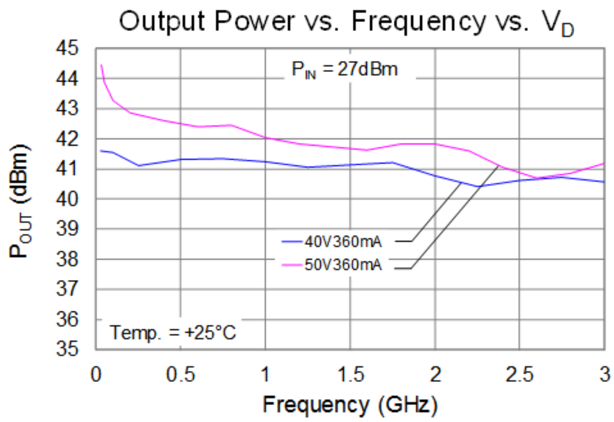


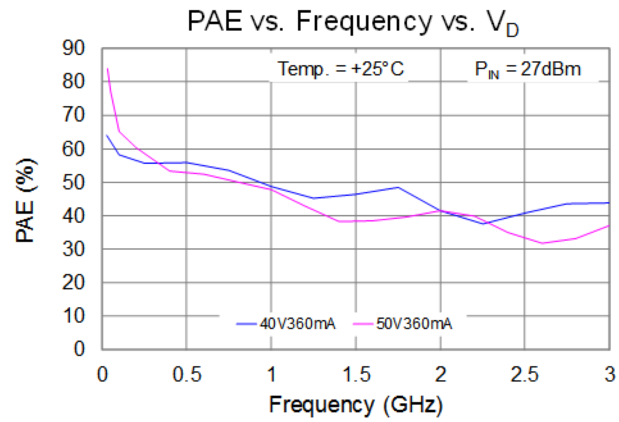


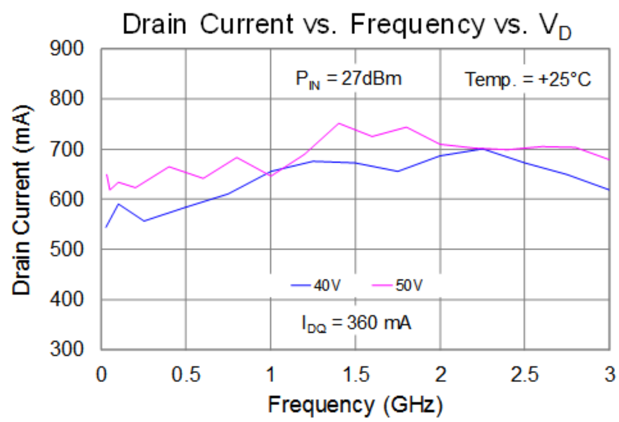


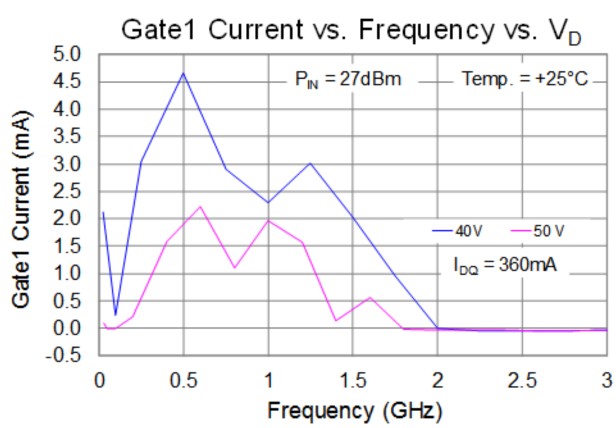
Performance Plots – Large Signal (CW)

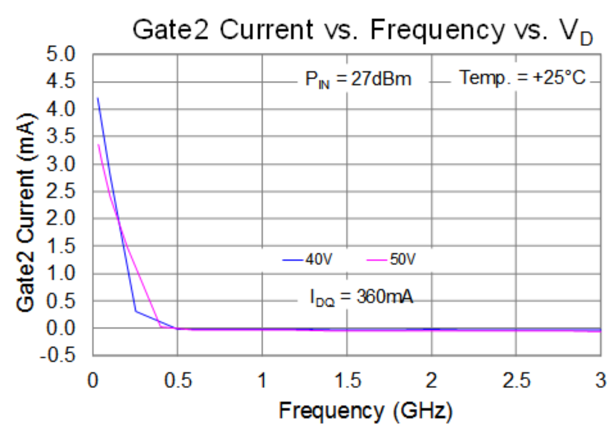
The plots reflect performance measured with an external coaxial bias tee and DC blocks











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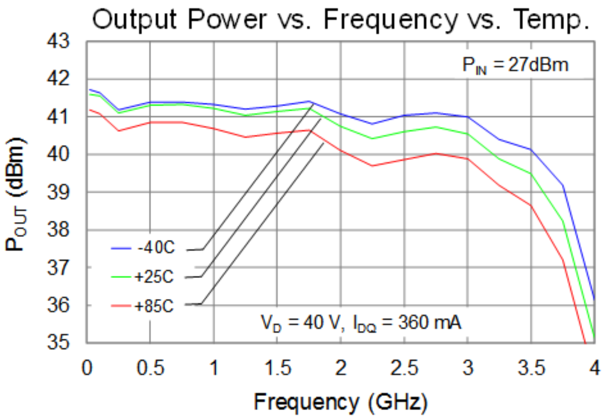

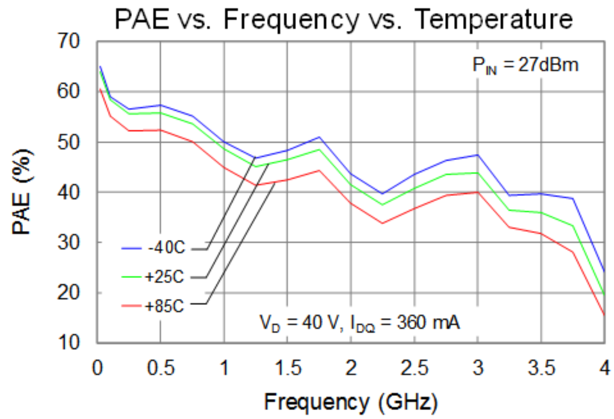

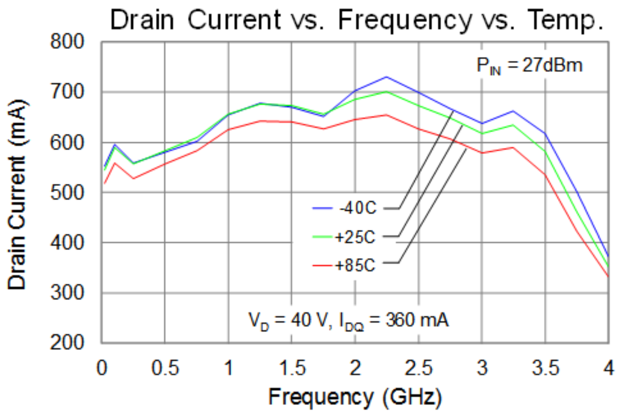

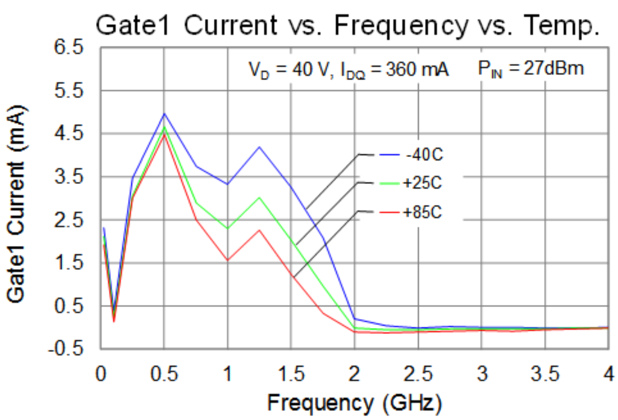

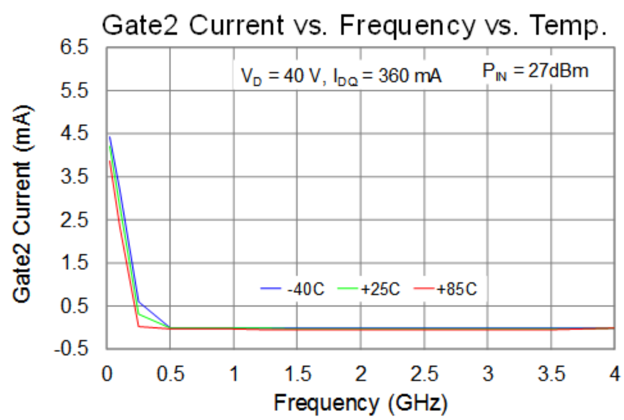

Performance Plots – Large Signal (CW)

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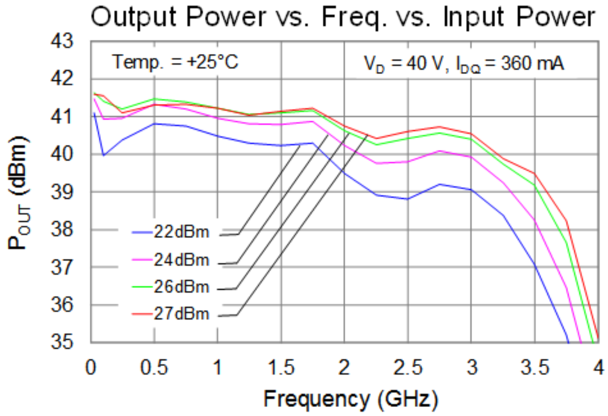
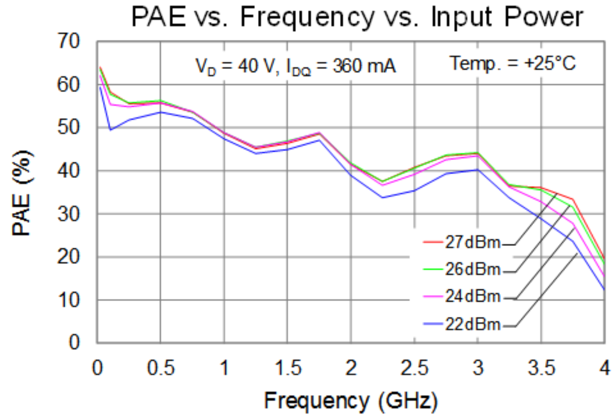
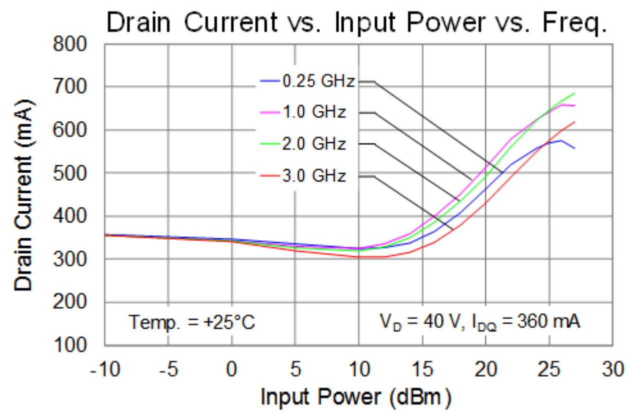
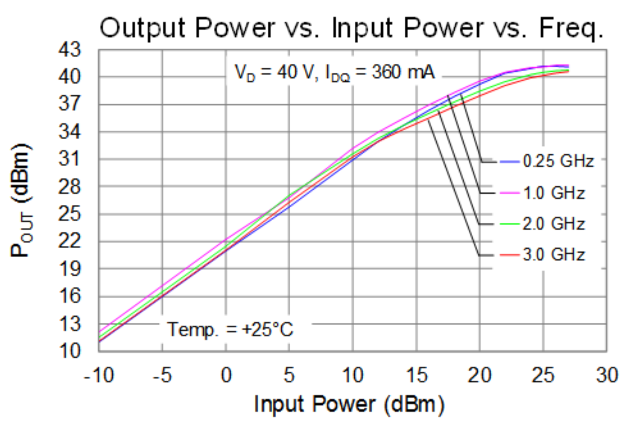
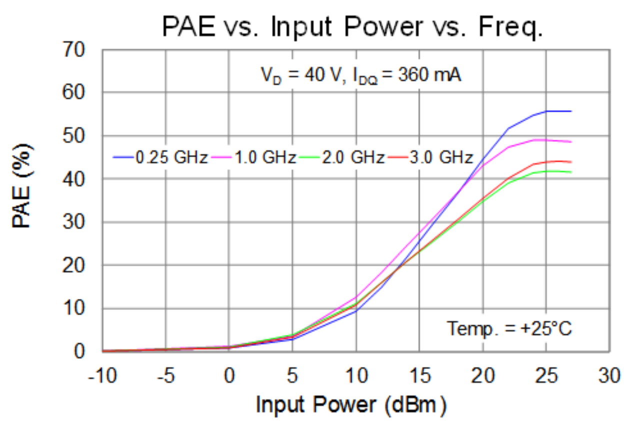




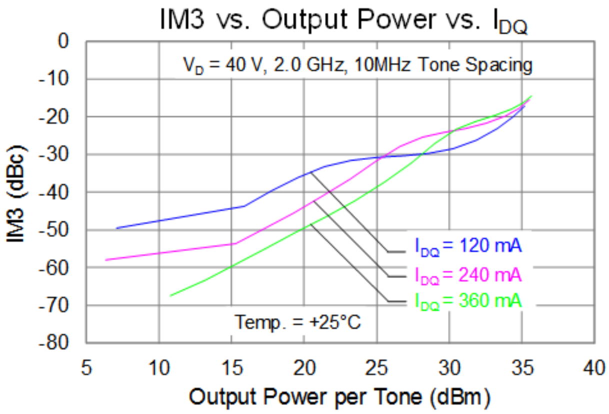


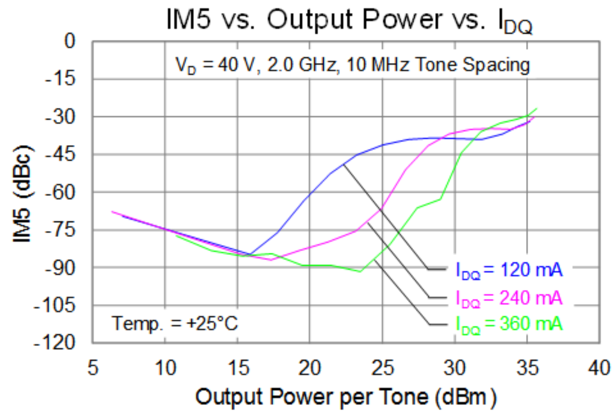


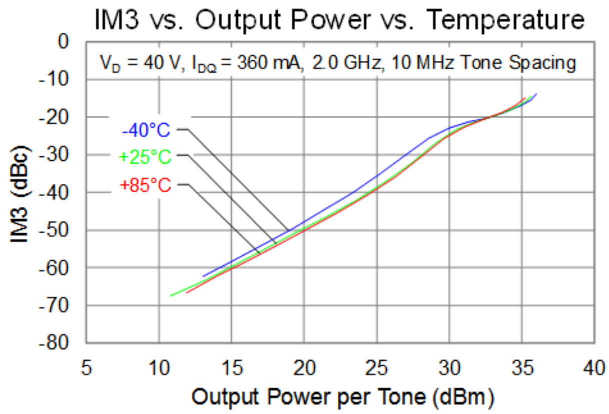


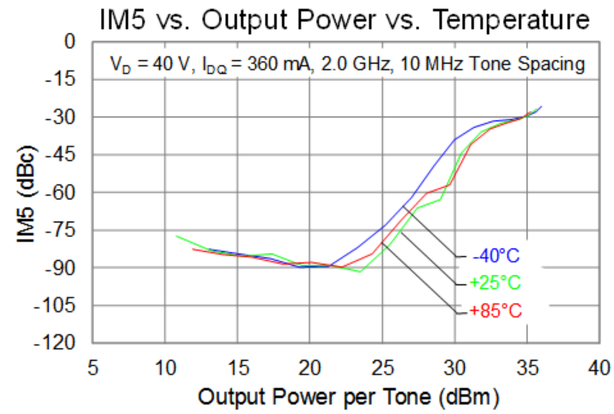
Performance Plots – Linearity

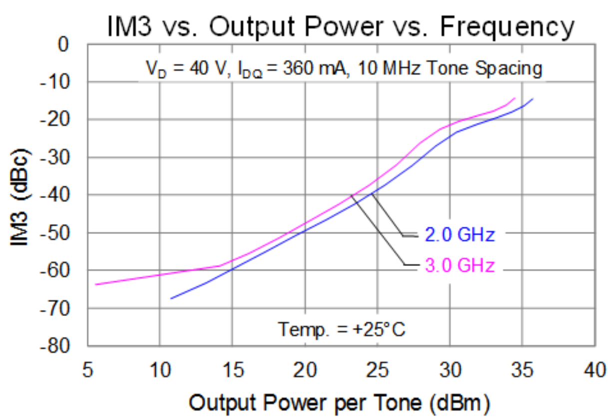
The plots reflect performance measured with an external coaxial bias tee and DC blocks

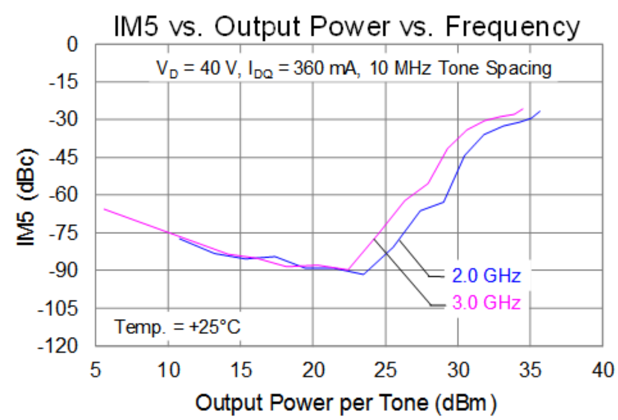












Performance Plots – Linearity

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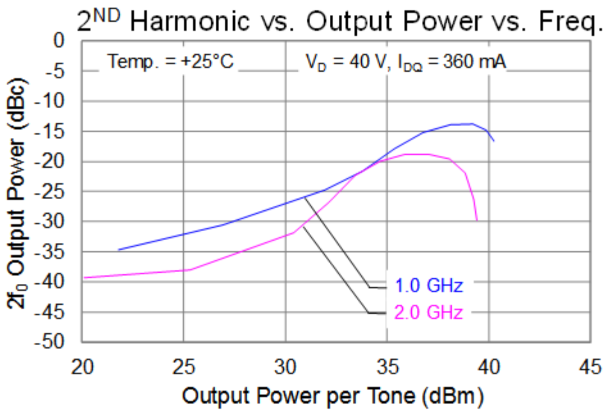
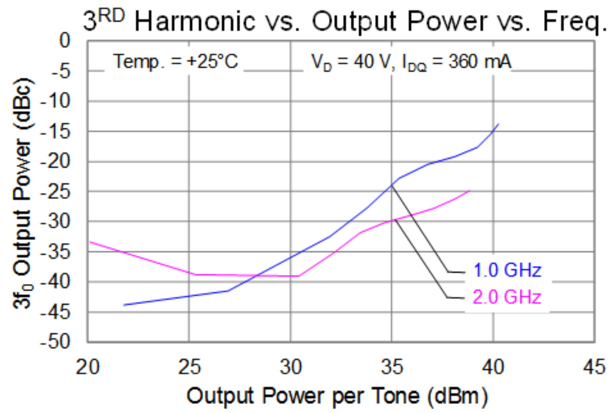
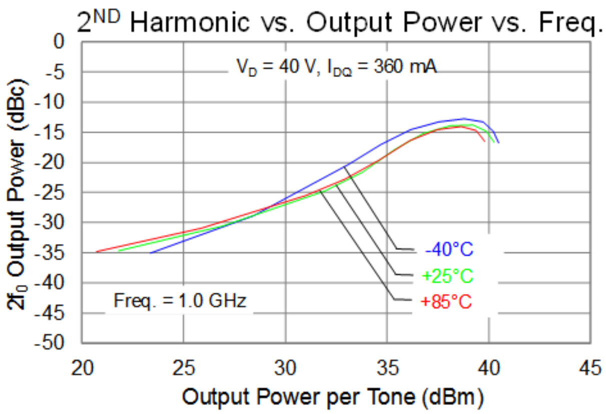
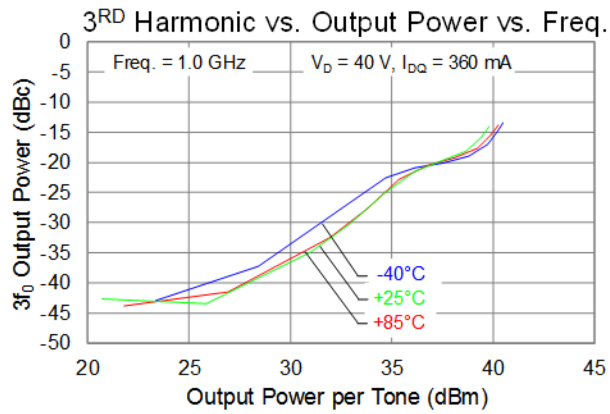
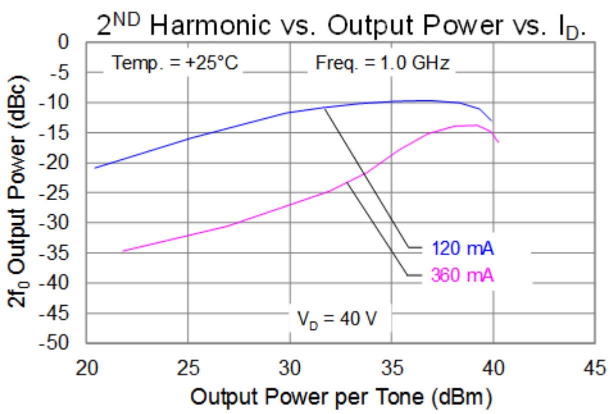
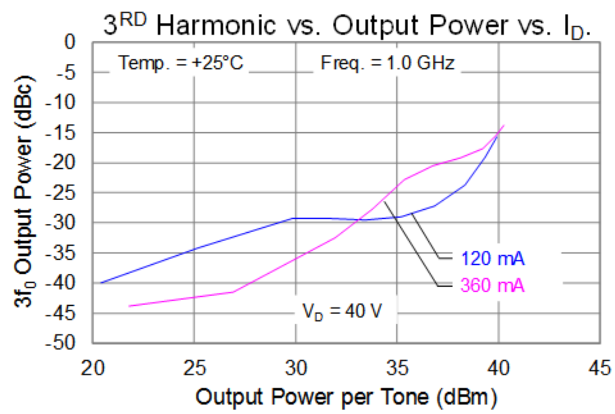






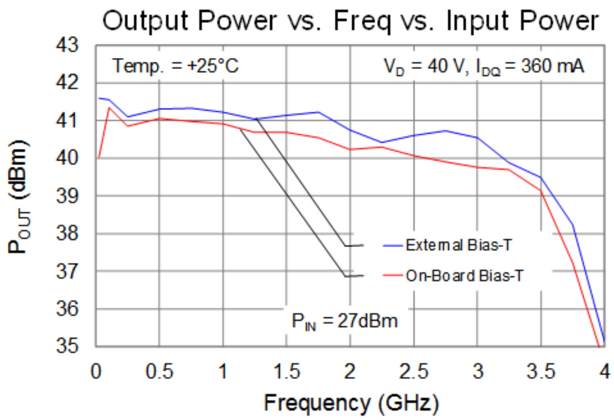


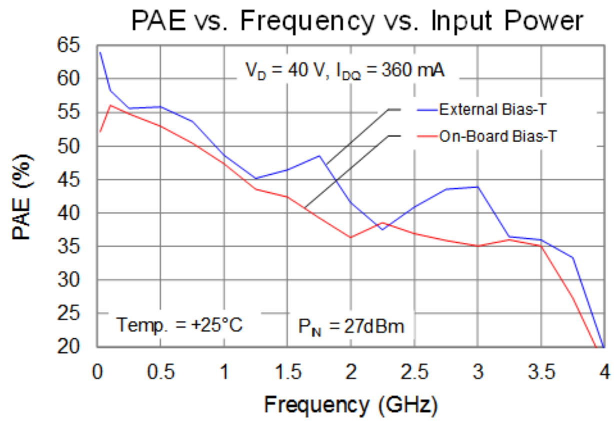




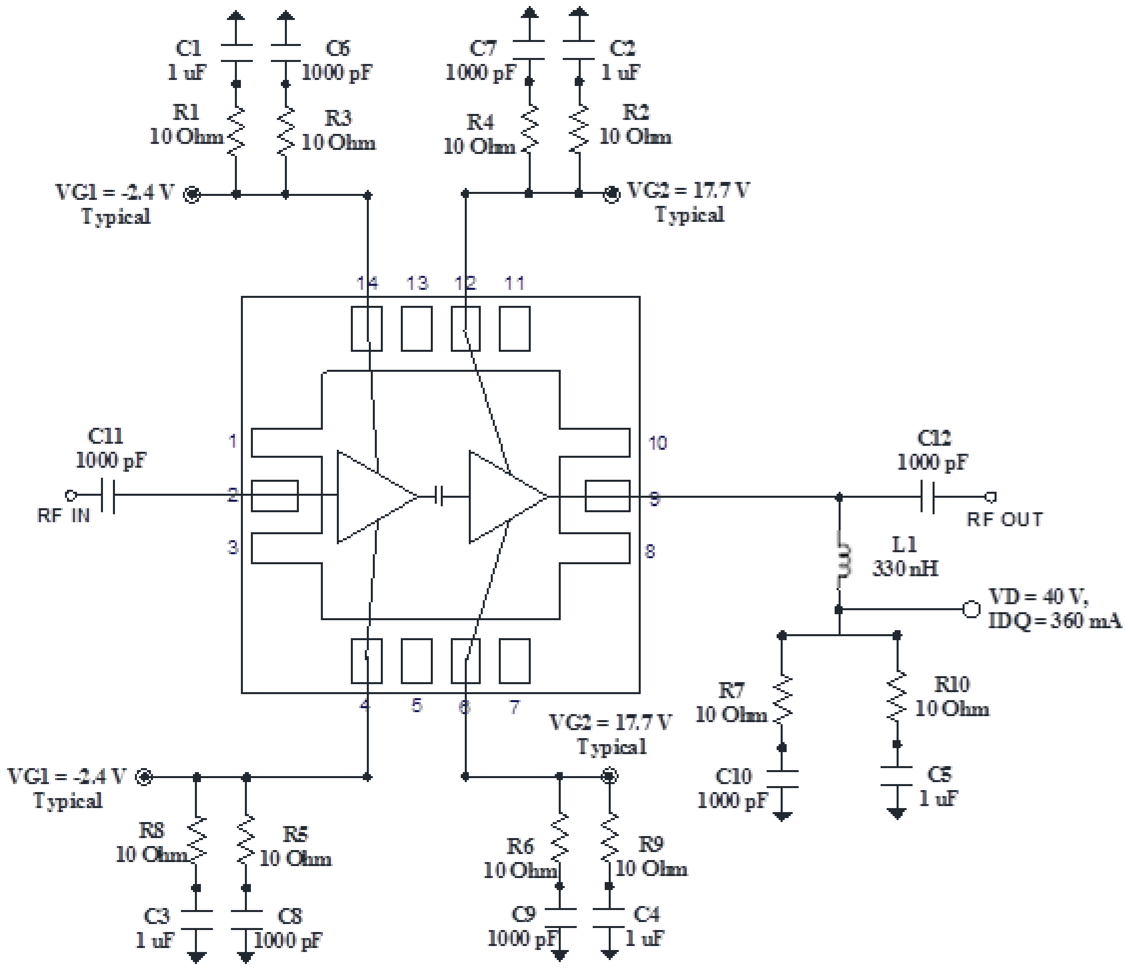
Performance Plots – Large Signal (CW), On–board vs. External Bias–T

The plots below reflect performance measured between external bias tee and on-board bias tee





Application Circuit



Notes:
1. V_{G1} & V_{G2} can be biased from either side (Top or Bottom.)
2. Plot data (DVT) shown are captured with EVBs using external bias tee (not on EVB board), performance of the DUT with on board surface mount DC blocks and bias tee components may be degraded relative to the DVT data option (Ref page 11). These components should be optimized for the desired operational bandwidth.

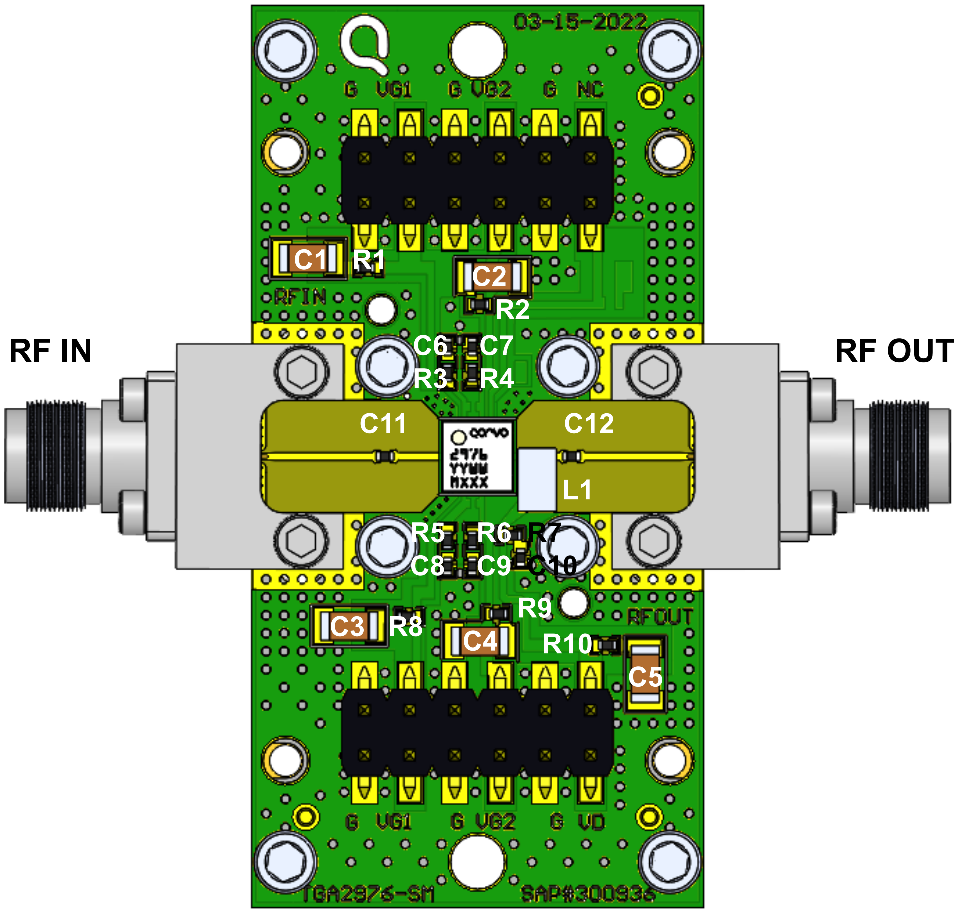
Bias-Up Procedure

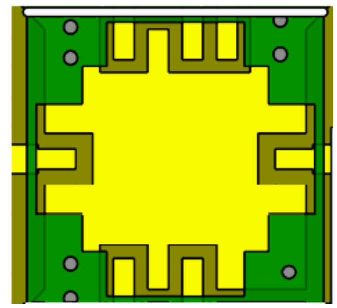
1. Set I_D limit to 755 mA, I_{G1} & I_{G2} limit to 5 mA
2. Set V_{G1} to -5.0 V
3. Set VD +40 V
4. Set V_{G2} to (V_D/2) - 2.7 V or (40 V/2) - 2.7 V = 17.3 V
5. Adjust V_{G1} more positive until I_{DQ} = 360 mA
6. Adjust V_{G2} to (V_D/2) + V_{G1}; (V_{G2} ~ +17.7 V Typical)
7. Apply RF signal

Bias-Up Procedure

1. Turn off RF signal
2. Reduce V_{G1} to -5.0 V. Ensure I_{DQ} ~ 0mA
3. Reduce V_{G2} to 0 V.
4. Set V_D to 0 V
5. Turn off V_D supply
6. Turn off V_{G2} supply
7. Turn off V_{G1} supply

EVB Assembly Drawing





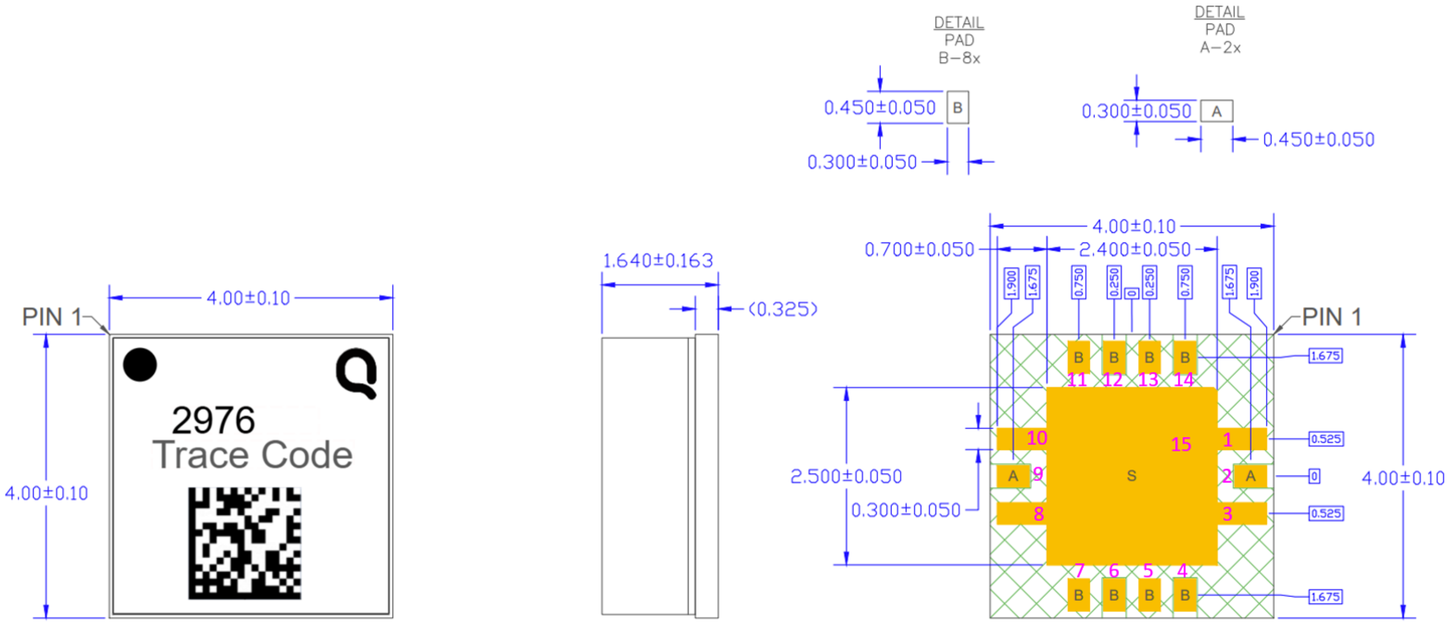
Package Mounting Area

Note: RF Layer is 8 mil thick Rogers Corp. RO4003C, ε_r = 3.38. Both metal layers are 0.5 oz. copper.
The EVB has on board bias Tee. Performance using onboard bias-tee may have degraded performance compared with external bias tee. See page 11 for the performance difference.

Bill of Materials for On–Board Bias–T

Reference Des.	Value	Description	Manuf.	Part Number
C1 – C5	1uF	Cap, 1206, 50V, 15%, X7R	Various	
C6 – C12	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
L1	330nH	Inductor, 1206, 850 mA	Various	
R1 – R10	10Ω	Res, 0402, 5%	Various	

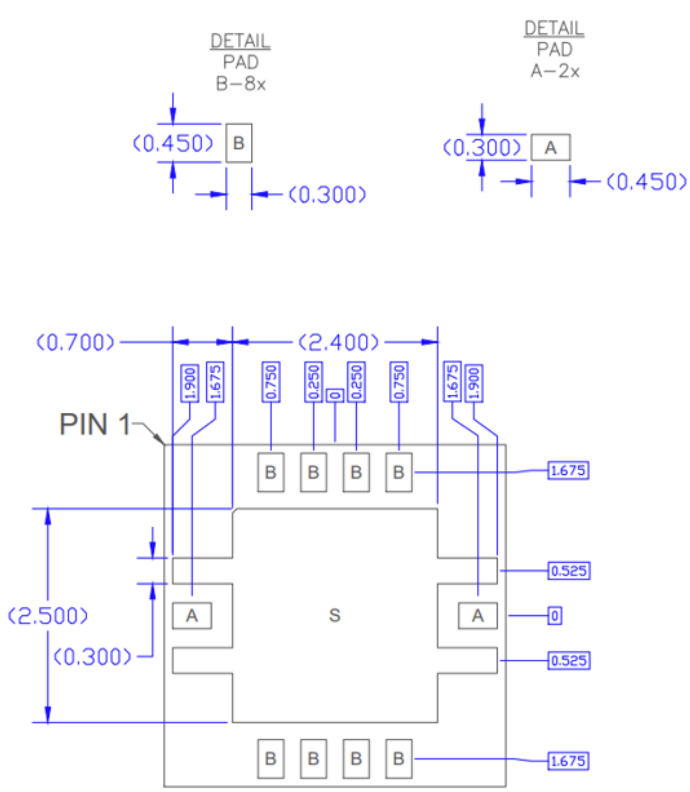
Mechanical Drawing and Pad Description



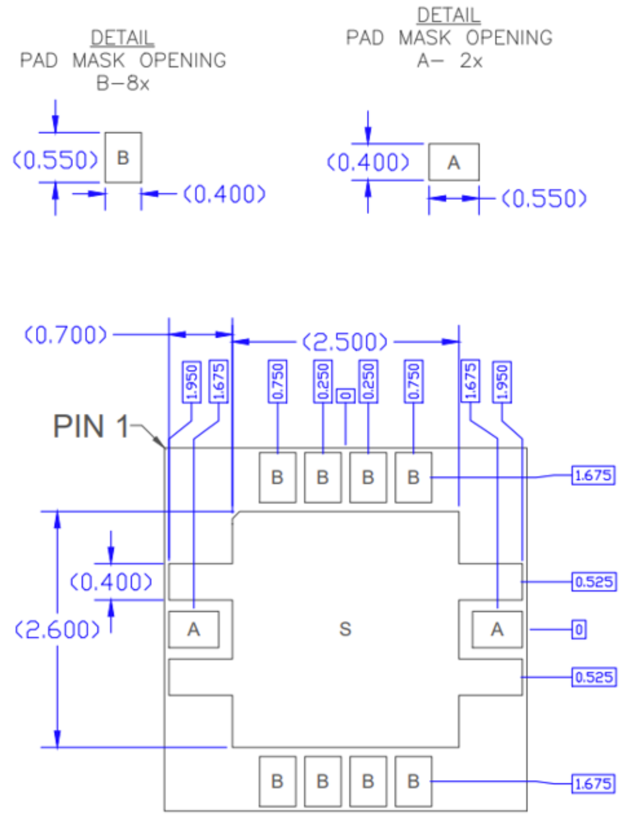
Units: Millimeters (mm)
Tolerances: unless specified: x.xx = ± 0.25; x.xxx = ± 0.100
Materials: Base: Laminate Substrate
Lid: Laminate
All metalized features are gold plated
Part is epoxy sealed
2DID Marking can be used to trace part manufacturing information

Pad No.	Symbol	Description
1, 3, 8, 10	GND	Connected to ground paddle (pin 15); must be grounded on PCB.
2	RF IN	RF Input, matched to 50 Ω, DC coupled.
4, 14	GATE1	Gate voltage 1; bias network is required; see recommended Application Information on page 14.
5, 7, 11, 13	N/C	No internal connection; should be connected to PCB ground.
6, 12	GATE2	Gate voltage 2; bias network is required; see recommended Application Information on page 14.
9	RF OUT/ DRAIN	RF Output, matched to 50 Ω, DC coupled.
15	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

Application PCB Land Patterns and Masks



Recommended Land Pattern



Recommended Land Pattern Mask

Units: Millimeters (mm)
Tolerances: unless specified: x.xx = ± 0.25; x.xxx = ± 0.100

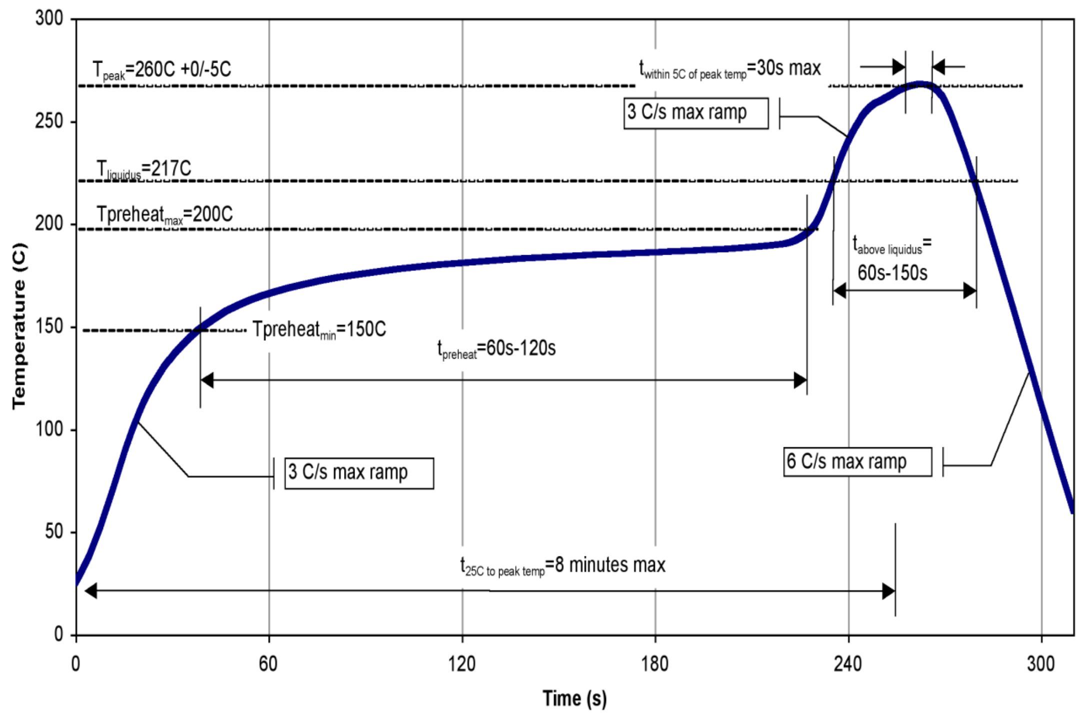
Assembly Notes

Compatible with lead-free soldering processes with 260°C peak reflow temperature.

This package is air-cavity and non-hermetic, and therefore cannot be subjected to aqueous washing. The use of no-clean solder to avoid washing after soldering is highly recommended.

Contact plating: Ni-Au.

Solder rework not recommended.



Recommended Soldering Temperature Profile

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:
- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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