TGF2965-SM

5 W, 32 V, 0.03–3.0 GHz, GaN RF Input-Matched Transistor

General Description

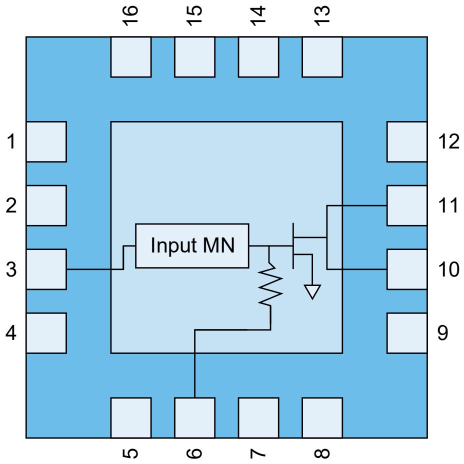
The Qorvo TGF2965-SM is a 5 W (P_{3dB}), 50 Ω-input matched discrete GaN on SiC HEMT which operates from 0.03 to 3.0 GHz. The integrated input matching network enables wideband gain and power performance, while the output can be matched on board to optimize power and efficiency for any region within the band.

The device is housed in an industry-standard 3 x 3 mm surface mount QFN package.

Lead-free and ROHS compliant

Evaluation boards are available upon request.

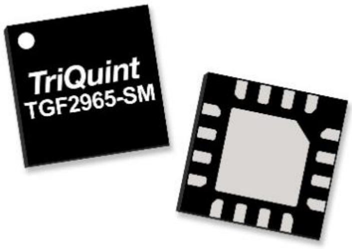
Functional Block Diagram



TGF2965-SM EVB Performance

Freq.(GHz)	P_{3dB}(W)	G_{3dB}(dB)	PAE_{3dB}(%)
0.03	4.4	13.5	45.5
0.05	4.6	13.9	48.5
0.1	4.7	13.9	48.7
0.5	4.0	12.6	42.2
1.0	5.0	13.8	52.9
1.5	4.7	13.5	43.6
2.0	5.2	14.2	46.8
2.5	5.0	14.1	50.6
3.0	4.4	12.3	47.3

CW Signal, V_D = 32 V, I_{DQ} = 30 mA, 25°C Base Temperature



Product Features

- Frequency: 0.03 to 3.0 GHz
- Output Power (P_{3dB})[1]: 6.0 W
- Linear Gain[1]: 18 dB
- Typical $DEFF_{3dB}$[1]: 65%
- Operating Voltage: 32 V
- Low thermal resistance package
- CW and Pulse capable
- 3 x 3 mm package

[1] At 2 GHz

Applications

- Military Radar
- Civilian Radar
- Land Mobile and Military Radio Communications
- Test Instrumentation
- Wideband and Narrowband Amplifiers
- Jammers

Ordering Information

Part	Description
1123170	TGF2965-SM 100 pc MOQ
1123185	TGF2965-SM 30-3000 MHz EVB

Absolute Maximum Ratings

Parameter	Value/Range
Breakdown Voltage (BV_{DG})	100 V min.
Gate Voltage Range (V_G)	-7 to +2 V
Drain Current (I_D)	0.6 A
Gate Current (I_G)	See page 4.
Power Dissipation (P_D)	7.5 W
RF Input Power, CW, T = 25 °C (P_{IN})	30 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter[1]	Value/Range
Drain Voltage (V_D)	32 V (Typ.)
Drain Quiescent Current (I_{DQ})	25 mA (Typ.)
Peak Drain Current (I_D)	326 mA (Typ.)
Gate Voltage (V_G)	-2.7 V (Typ.)
Power Dissipation, CW (P_D)	7.05 W (Max)
Power Dissipation, Pulse (P_D)[2]	9.1 W (Max)

[1] Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

[2] 100uS Pulse Width, 20% Duty Cycle

RF Characterization–Load Pull Performance

Test conditions unless noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 30 mA, Pulse: 100 uS Pulse Width, 20% Duty Cycle

Symbol	Parameter	Typical					Units
F	Frequency	1	1.5	2	2.5	3	GHz
G_{LIN}	Linear Gain, Power Tuned	17.3	17.4	18.2	17.8	16.9	dB
P_{3dB}	Output Power at 3 dB Gain Compression, Power Tuned	37.8	37.7	37.8	38.1	38.3	dBm
$DEFF_{3dB}$	Drain Efficiency at 3 dB Gain Compression, Efficiency Tuned	76.0	62.7	65.2	65.4	71.9	%
G_{3dB}	Gain at 3 dB Compression, Power Tuned	14.3	14.4	15.2	14.8	13.9	dB

RF Characterization–0.03–3.0 GHz EVB Performance at 2.5 GHz–Pulsed

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 32 V, I_{DQ} = 30 mA, Pulse: 100 uS Pulse Width, 20% Duty Cycle

Symbol	Parameter	Min	Typical	Max	Units
G_{LIN}	Linear Gain		17.1		dB
P_{3dB}	Output Power at 3 dB Gain Compression		5.0		W
DE_{3dB}	Drain Efficiency at 3 dB Gain Compression		50.6		%
G_{3dB}	Gain at 3 dB Compression		14.1		dB

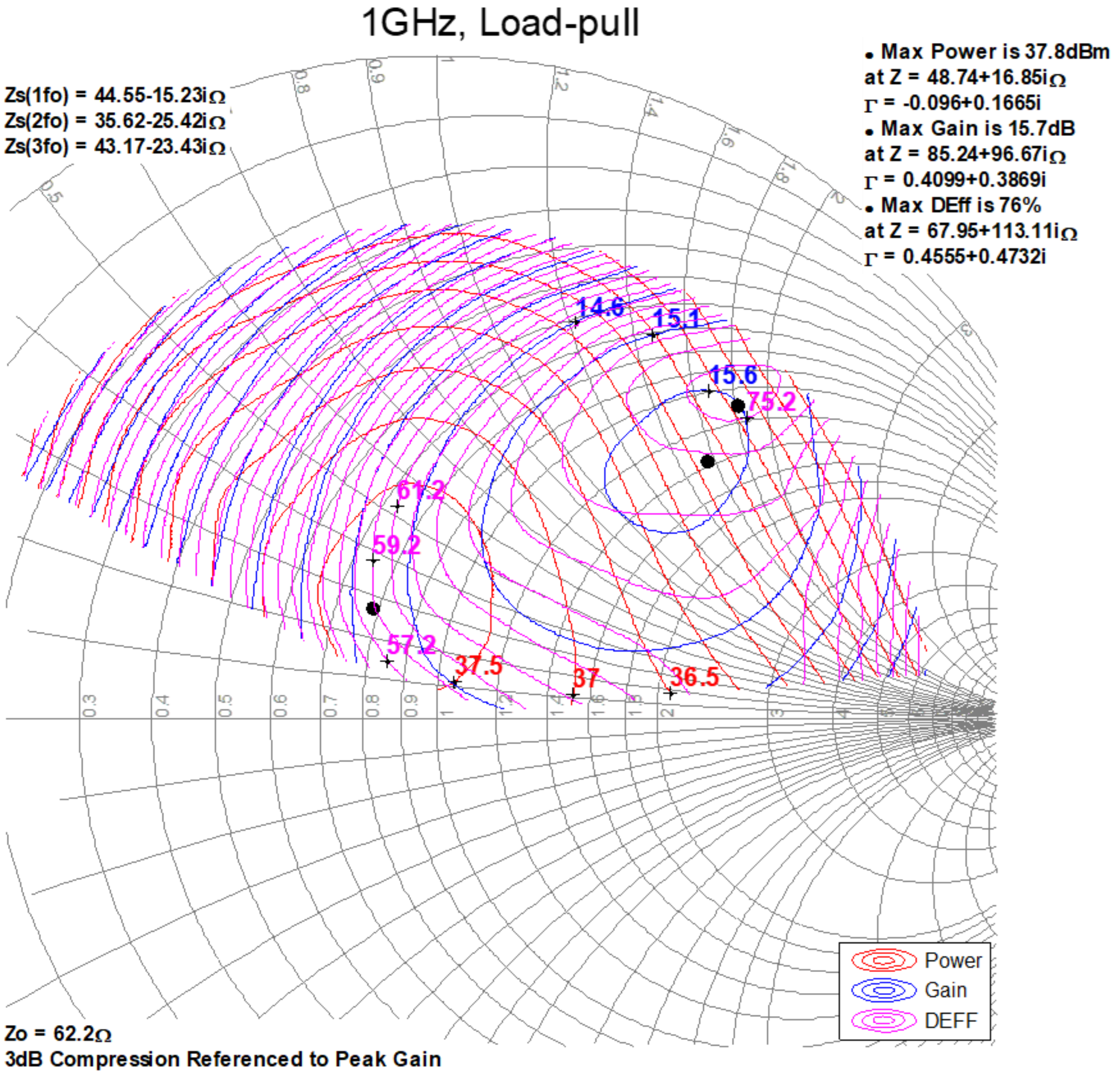
RF Characterization–Mismatch Ruggedness at 1, 2 and 3 GHz

Test conditions unless otherwise noted: T_A = 25 °C, V_D = 28 V, I_{DQ} = 30 mA, Pulse: 100 uS Pulse Width, 20% Duty Cycle
Driving input power is determined at pulsed compression under matched condition at EVB output connector.

Symbol	Parameter	dB Compression	Typical
VSWR	Impedance Mismatch Ruggedness	3	10:1
VSWR	Impedance Mismatch Ruggedness	8	2:1

Load Pull Smith Charts [1, 2]

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

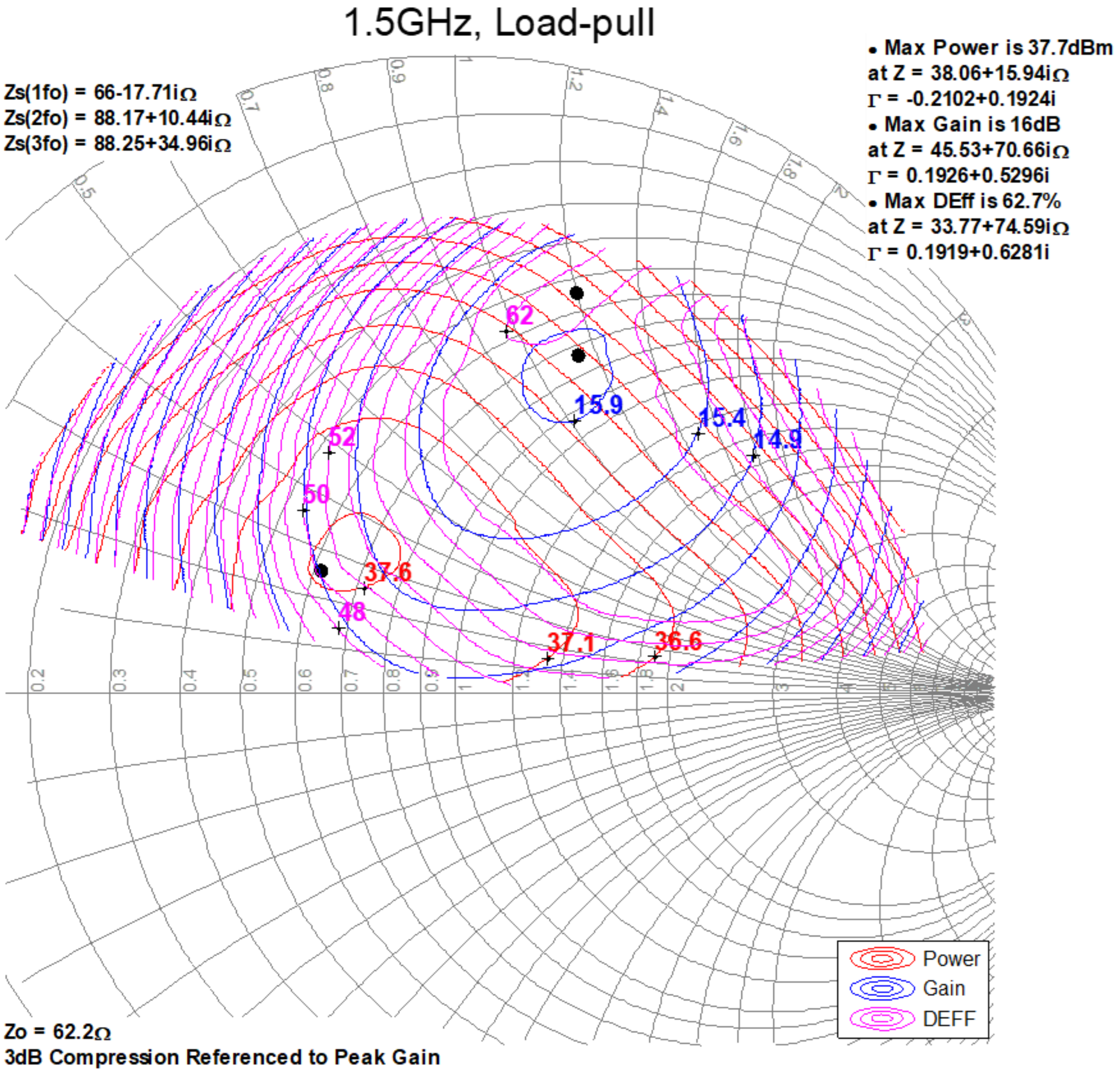


Notes:

1. 32 V, 30 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 18 for load pull and source pull reference planes.

Load Pull Smith Charts [1, 2]

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

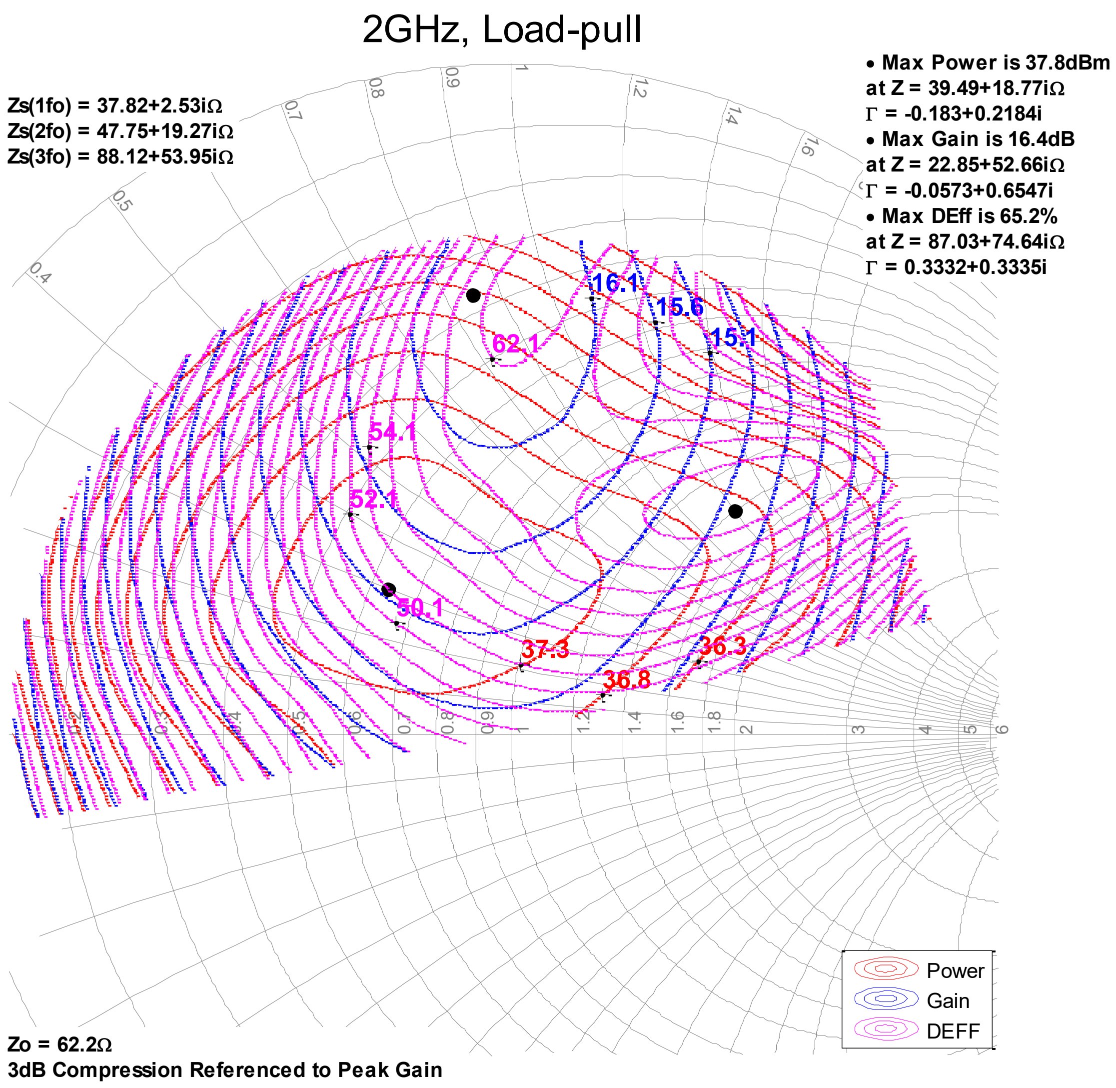


Notes:

1. 32 V, 30 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 18 for load pull and source pull reference planes.

Load Pull Smith Charts [1, 2]

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.


2GHz, Load-pull

Zs(1fo) = 37.82+2.53iΩ
Zs(2fo) = 47.75+19.27iΩ
Zs(3fo) = 88.12+53.95iΩ

- **Max Power is 37.8dBm**
at Z = 39.49+18.77iΩ
Γ = -0.183+0.2184i
- **Max Gain is 16.4dB**
at Z = 22.85+52.66iΩ
Γ = -0.0573+0.6547i
- **Max DEff is 65.2%**
at Z = 87.03+74.64iΩ
Γ = 0.3332+0.3335i

Zo = 62.2Ω
3dB Compression Referenced to Peak Gain

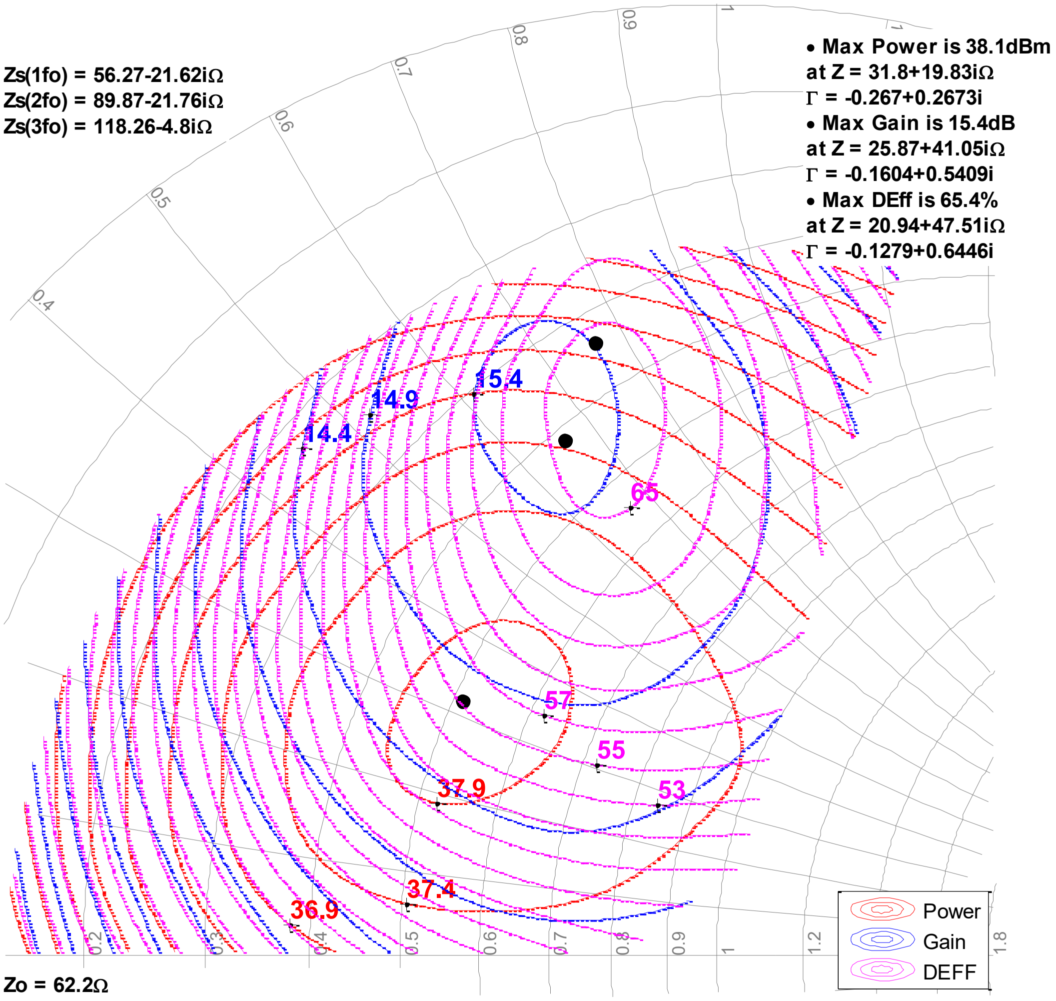
Notes:

1. 32 V, 30 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 18 for load pull and source pull reference planes.

Load Pull Smith Charts [1, 2]

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.

2.5GHz, Load-pull



Zs(1fo) = 56.27-21.62iΩ
Zs(2fo) = 89.87-21.76iΩ
Zs(3fo) = 118.26-4.8iΩ

- **Max Power is 38.1dBm**
at Z = 31.8+19.83iΩ
Γ = -0.267+0.2673i
- **Max Gain is 15.4dB**
at Z = 25.87+41.05iΩ
Γ = -0.1604+0.5409i
- **Max DEff is 65.4%**
at Z = 20.94+47.51iΩ
Γ = -0.1279+0.6446i

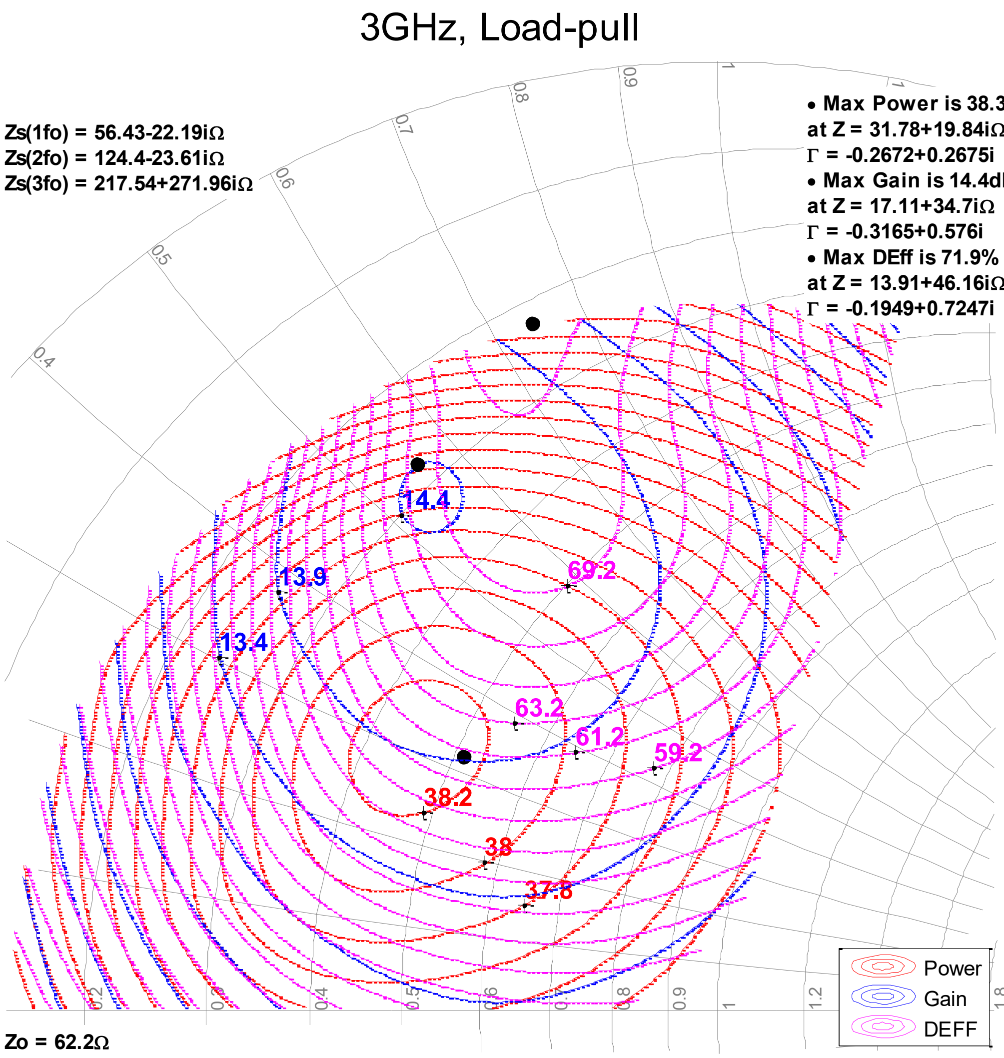
Zo = 62.2Ω
3dB Compression Referenced to Peak Gain

Notes:

1. 32 V, 30 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 18 for load pull and source pull reference planes.

Load Pull Smith Charts [1, 2]

RF performance that the device typically exhibits when placed in the specified impedance environment. The impedances are not the impedances of the device, they are the impedances presented to the device via an RF circuit or load-pull system. The impedances listed follow an optimized trajectory to maintain high power and high efficiency.



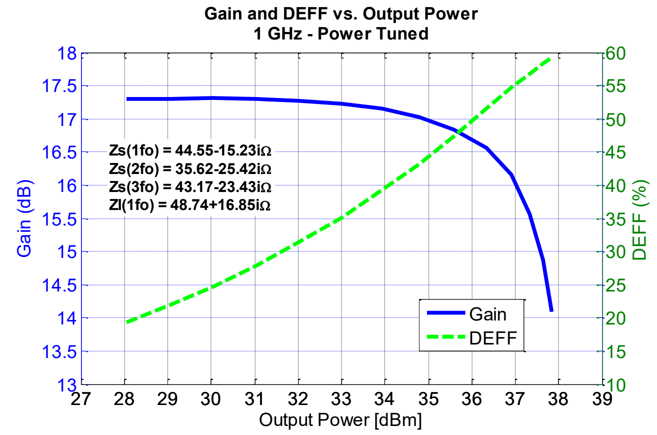
Zs(1fo) = 56.43-22.19iΩ
Zs(2fo) = 124.4-23.61iΩ
Zs(3fo) = 217.54+271.96iΩ

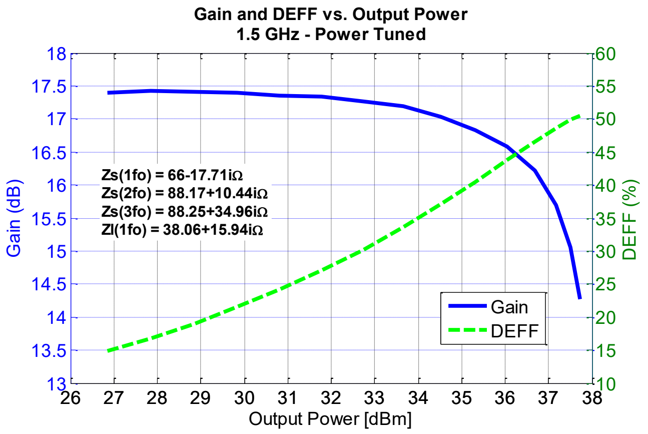
- **Max Power is 38.3dBm**
at Z = 31.78+19.84iΩ
Γ = -0.2672+0.2675i
- **Max Gain is 14.4dB**
at Z = 17.11+34.7iΩ
Γ = -0.3165+0.576i
- **Max DEff is 71.9%**
at Z = 13.91+46.16iΩ
Γ = -0.1949+0.7247i

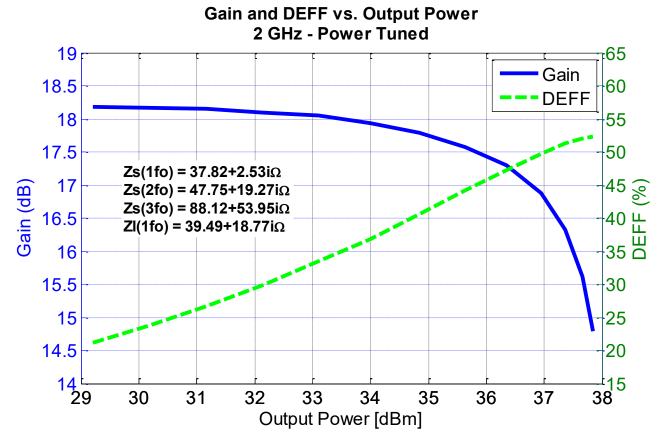
Zo = 62.2Ω
3dB Compression Referenced to Peak Gain

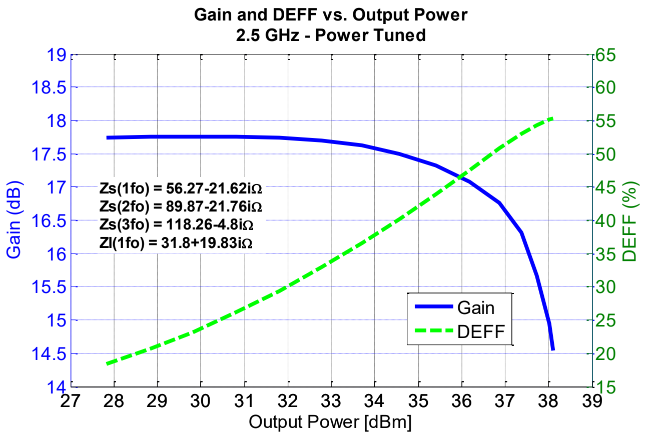
Notes:
1. 32 V, 30 mA, Pulsed signal with 100 uS pulse width and 20% duty cycle. 3 dB compression referenced to peak gain.
2. See page 18 for load pull and source pull reference planes.

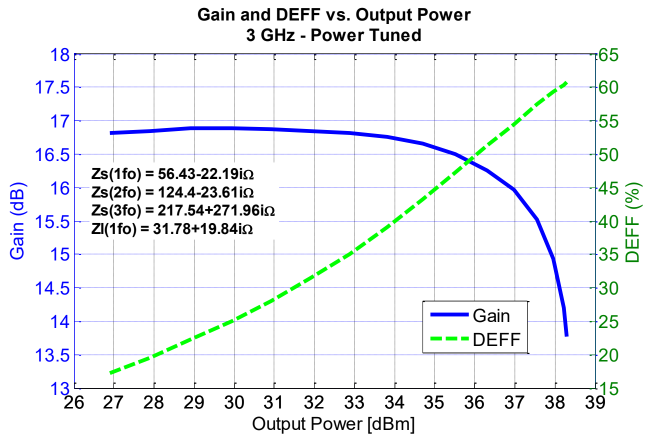
Load Pull Performance–Power Tuned [1,2]







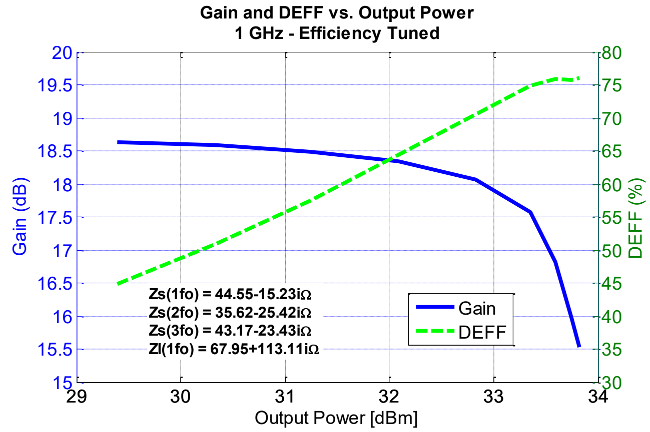


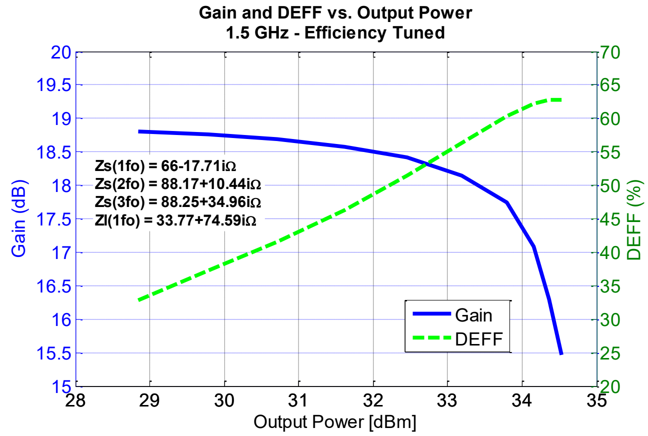


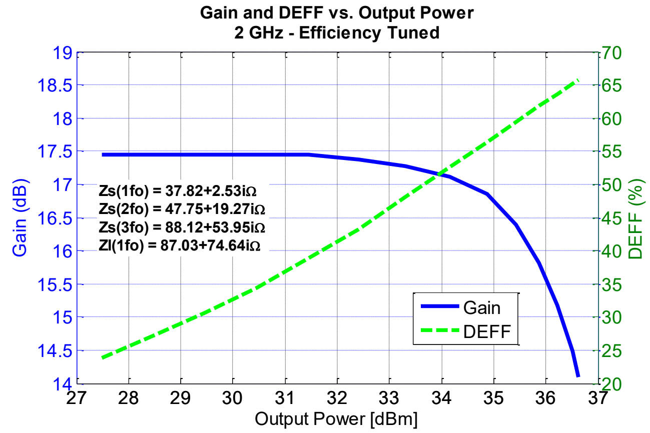
Notes:

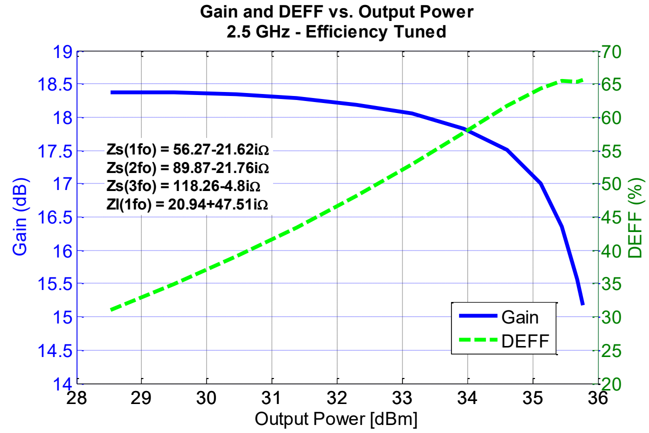
1. Pulsed signal with 100uS pulse width and 20% duty cycle
2. See page 18 for load pull and source pull reference planes where the performance was measured.

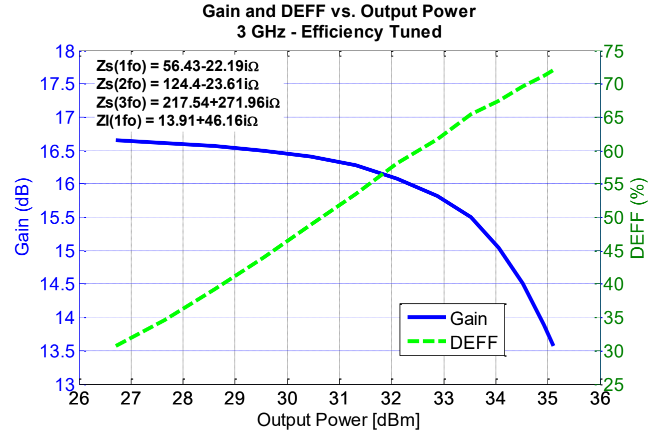
Load Pull Performance–Efficiency Tuned [1,2]


Gain and DEFF vs. Output Power
1 GHz - Efficiency Tuned


Gain and DEFF vs. Output Power
1.5 GHz - Efficiency Tuned


Gain and DEFF vs. Output Power
2 GHz - Efficiency Tuned


Gain and DEFF vs. Output Power
2.5 GHz - Efficiency Tuned

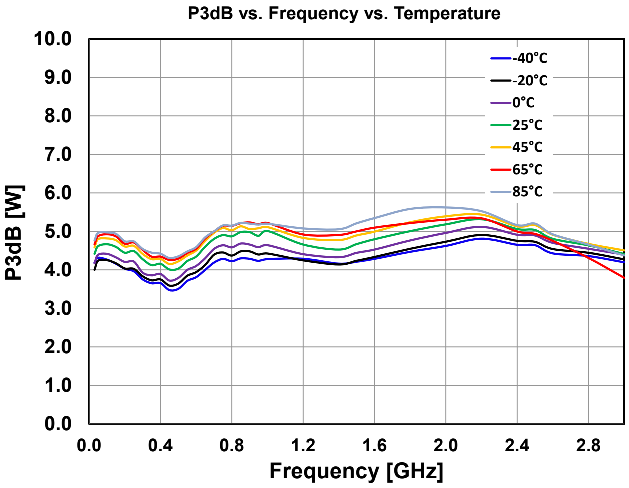

Gain and DEFF vs. Output Power
3 GHz - Efficiency Tuned

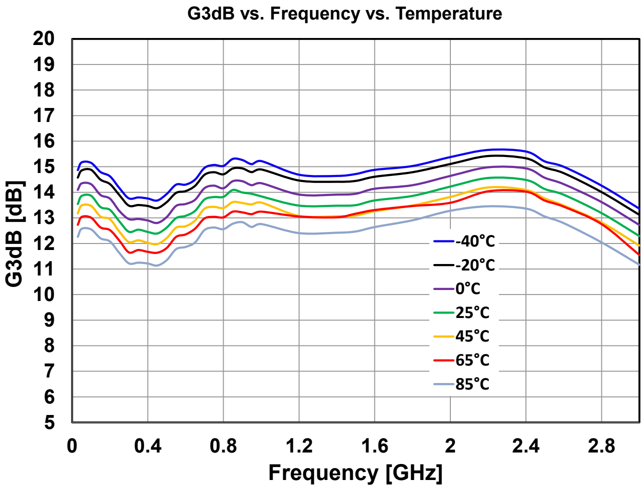
Notes:

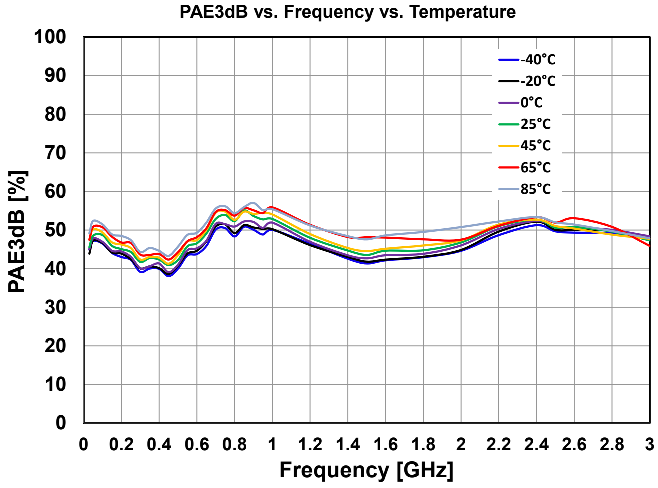
1. Pulsed signal with 100uS pulse width and 20% duty cycle
2. See page 18 for load pull and source pull reference planes where the performance was measured.

0.03–3.0 GHz Evaluation Board Performance Over Temperature[1, 2]

Performance measured on Qorvo's 0.03 GHz to 3 GHz Evaluation Board.





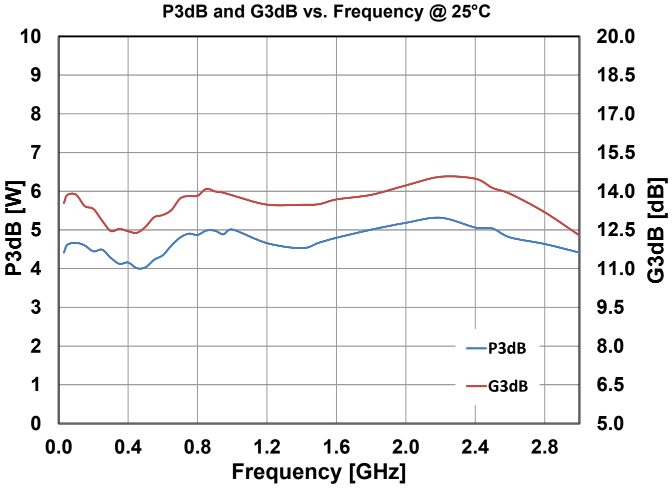


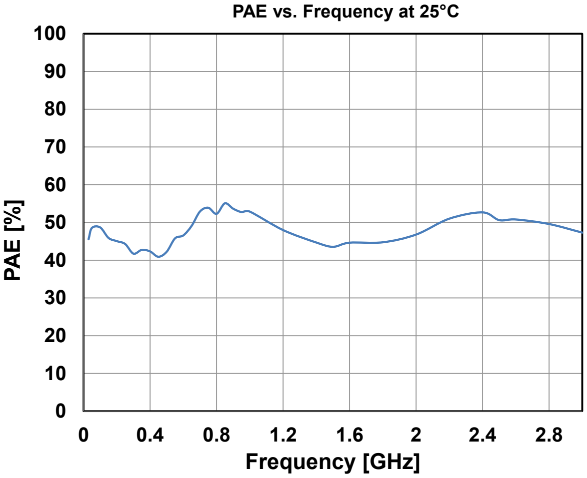
Notes:

1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 30 mA
2. Test Signal: Pulse Width = 100 µs, Duty Cycle = 20%

0.03–3.0 GHz Evaluation Board Performance At 25 °C[1, 2] – Pulsed

Performance measured on Qorvo's 0.03 GHz to 3 GHz Evaluation Board.



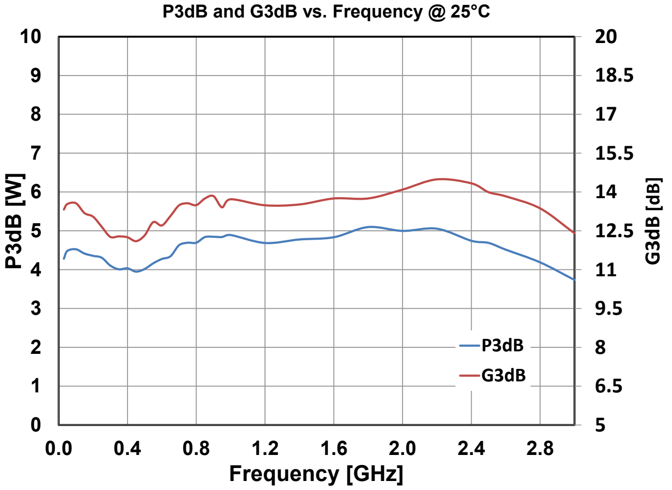


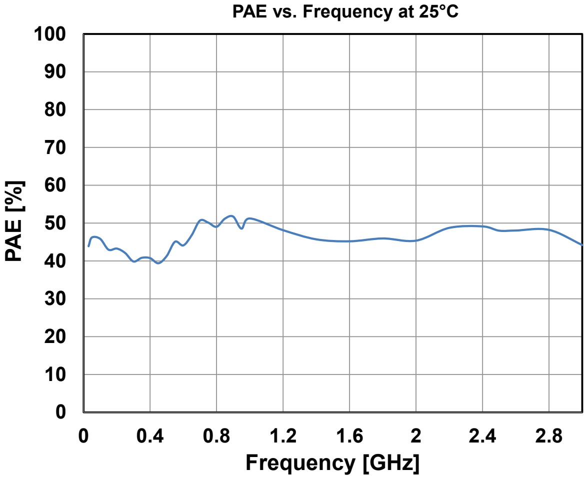
Notes:

1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 30 mA, 25 °C
2. Test Signal: Pulse Width = 100 µs, Duty Cycle = 20%

0.03–3.0 GHz Evaluation Board Performance At 25 °C[1] – CW

Performance measured on Qorvo's 0.03 GHz to 3 GHz Evaluation Board.

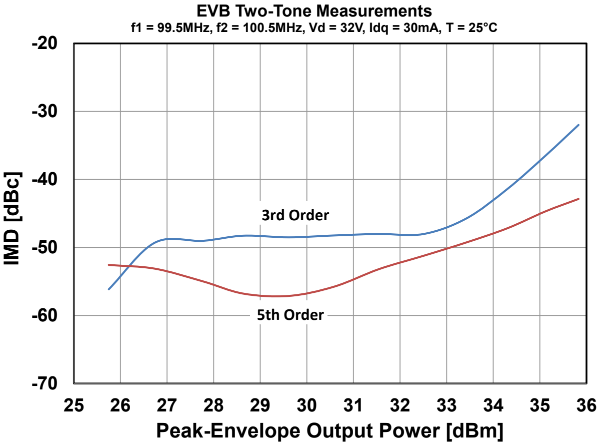


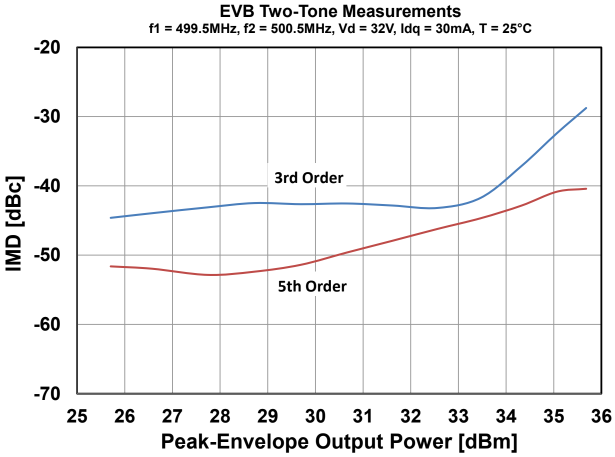


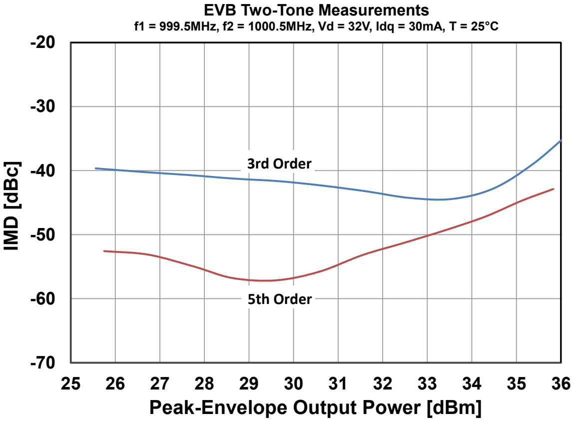
Notes:

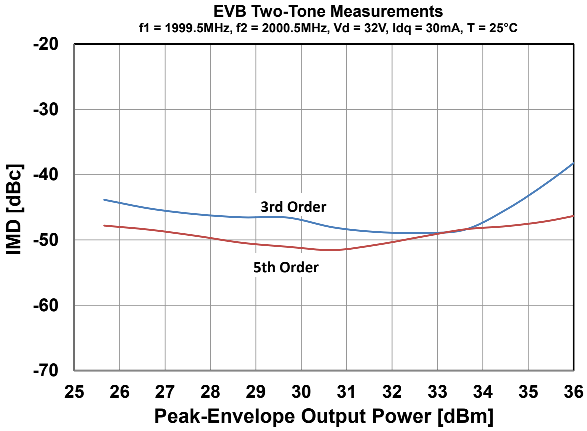
1. Test Conditions: V_{DS} = 32 V, I_{DQ} = 30 mA, 25 °C

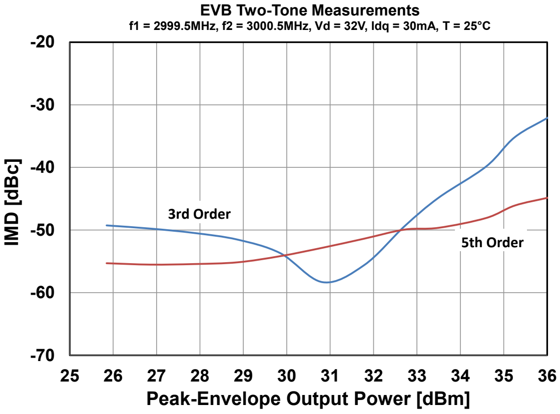
0.03 – 3.0 GHz Evaluation Board Performance–Two-Tone Measurements [1]







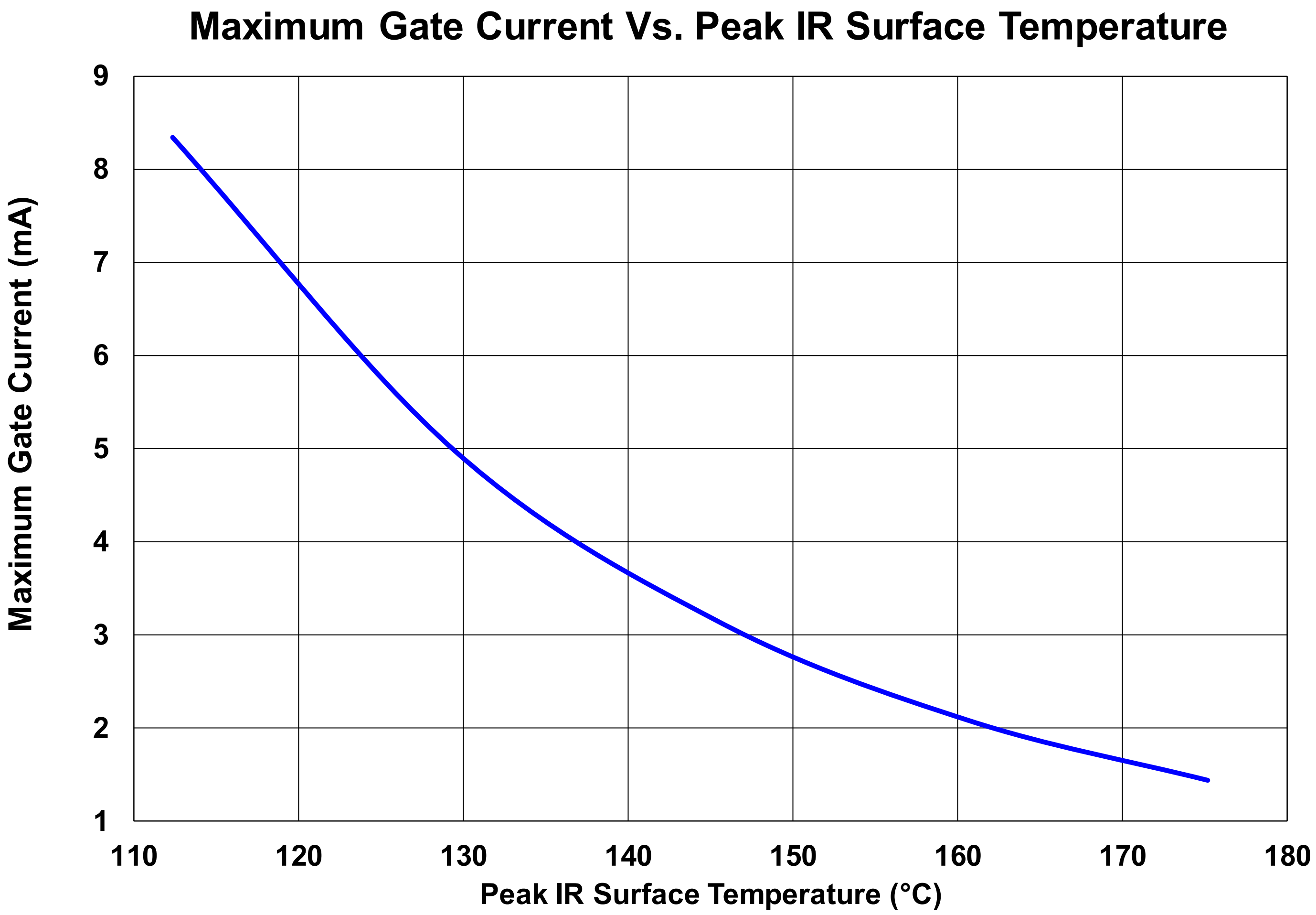




Notes:

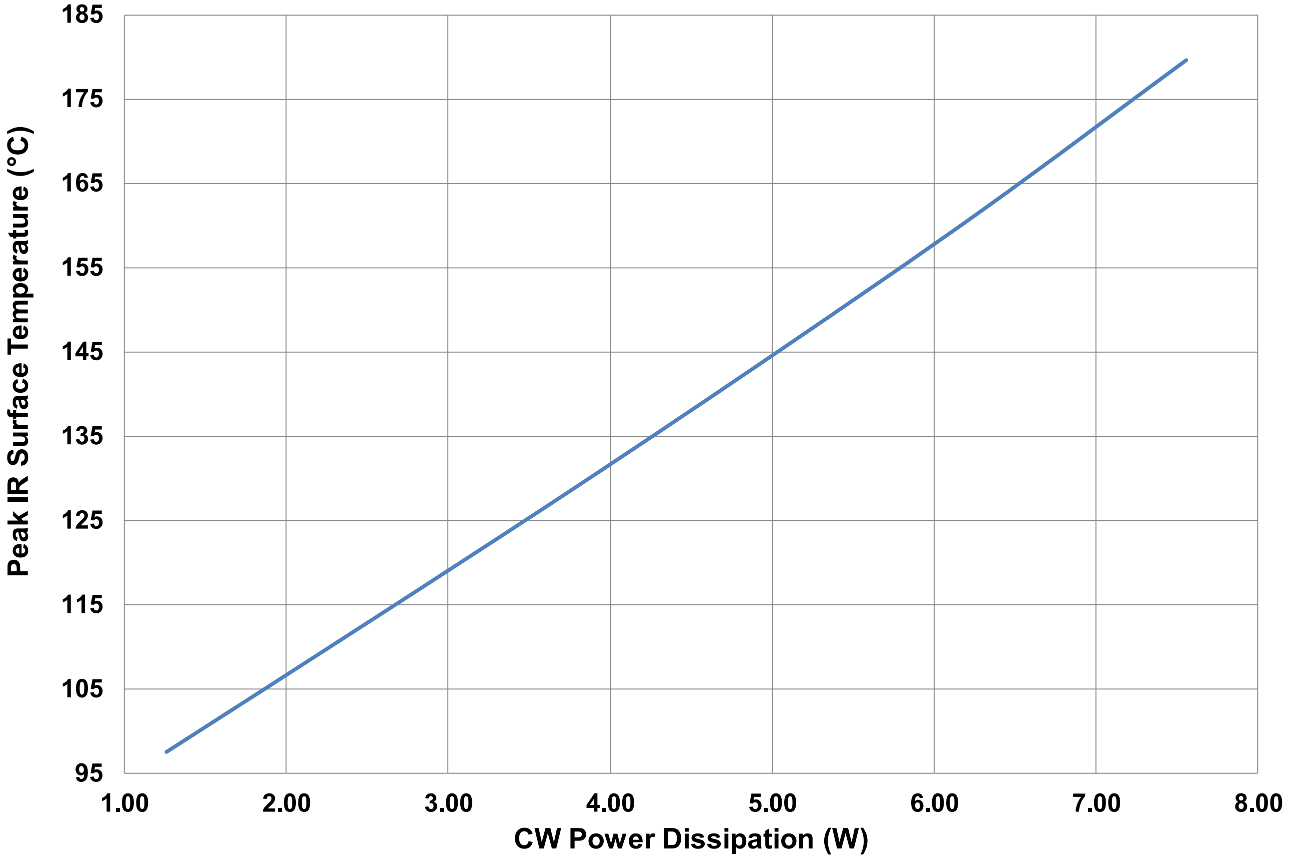
1. The Intermodulation Distortion products (IMD) are referenced to peak-envelope output power, which is 6 dB above single-tone output power

Maximum Gate Current



Thermal and Reliability Information - CW

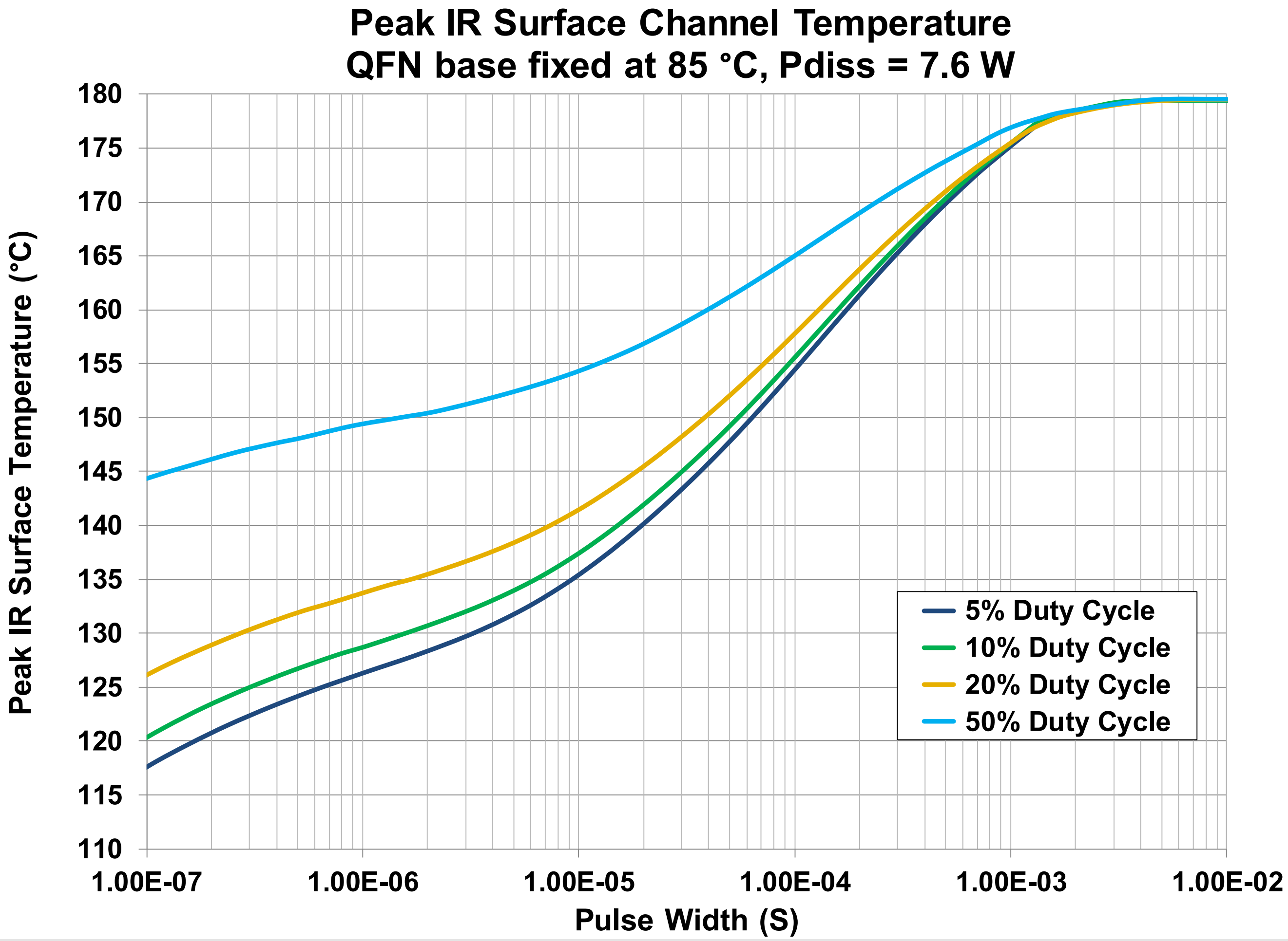
Peak IR Surface Temperature vs. CW Power Dissipation
Backside of QFN base fixed at 85 °C



Parameter	Conditions	Values	Units
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 1.26 W Pdiss, CW	9.9	°C/W
Peak IR Surface Temperature[1] (T_{CH})		97.4	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 2.52 W Pdiss, CW	11.1	°C/W
Peak IR Surface Temperature[1] (T_{CH})		113	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 3.78 W Pdiss, CW	11.6	°C/W
Peak IR Surface Temperature[1] (T_{CH})		129	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 5.04 W Pdiss, CW	11.9	°C/W
Peak IR Surface Temperature[1] (T_{CH})		145	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 6.30 W Pdiss, CW	12.2	°C/W
Peak IR Surface Temperature[1] (T_{CH})		162	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.56 W Pdiss, CW	12.5	°C/W
Peak IR Surface Temperature[1] (T_{CH})		180	°C

[1] Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

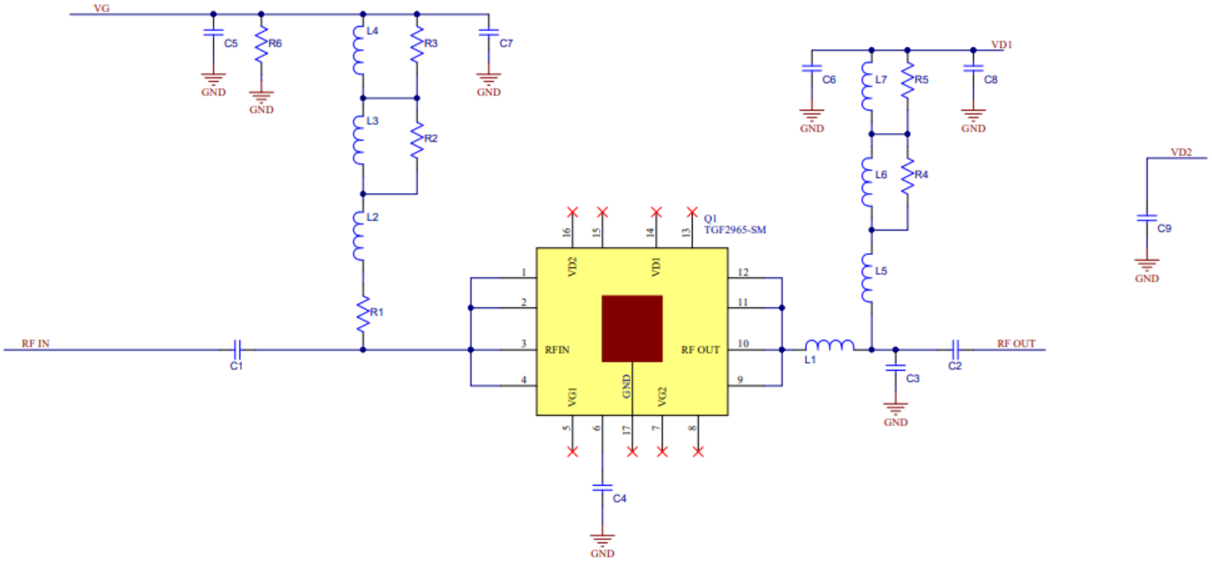
Thermal and Reliability Information - Pulsed



Parameter	Conditions	Values	Units
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 5% DC	9.1	°C/W
Peak IR Surface Temperature[1] (T_{CH})		154	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 10% DC	9.3	°C/W
Peak IR Surface Temperature[1] (T_{CH})		156	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 20% DC	9.6	°C/W
Peak IR Surface Temperature[1] (T_{CH})		158	°C
Thermal Resistance, IR[1] (θ_{JC})	85 °C Case 7.6 W Pdiss, 100 uS Pulse Width, 50% DC	10.5	°C/W
Peak IR Surface Temperature[1] (T_{CH})		165	°C

[1] Refer to the following document GaN Device Channel Temperature, Thermal Resistance, and Reliability Estimates

0.03–3.0 GHz Evaluation Board Schematic

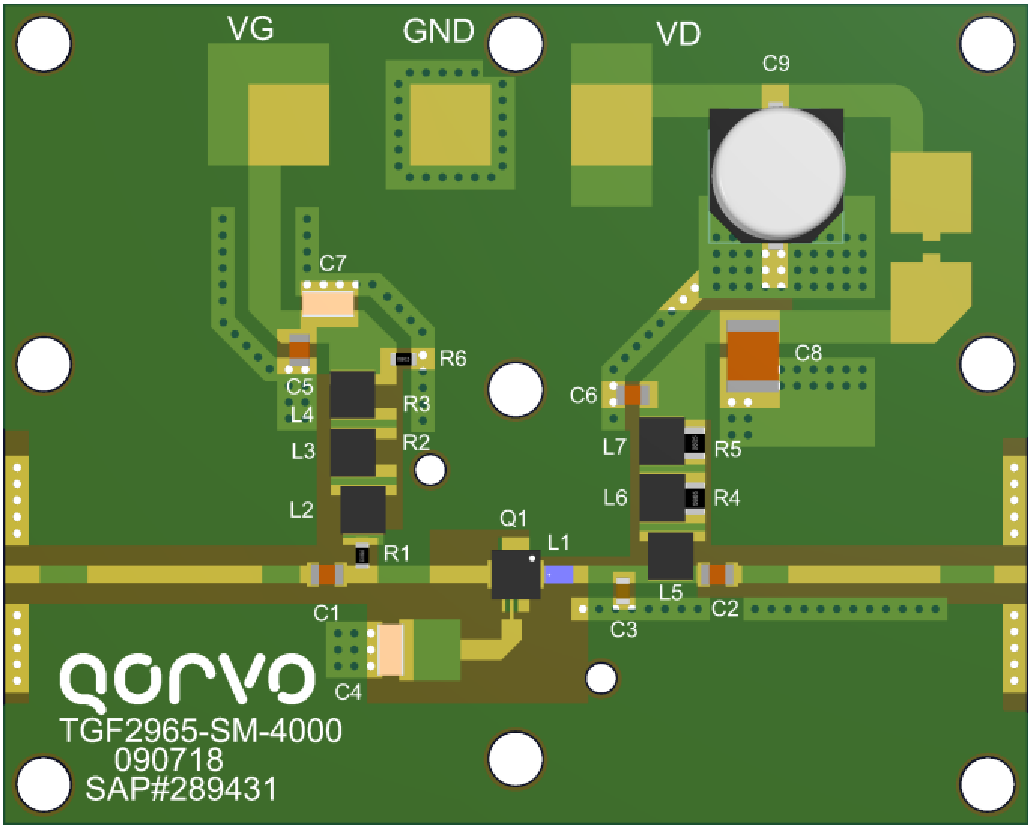


Bias-up Procedure
V_G set to -5 V.
V_D set to 32 V.
Adjust V_G more positive until quiescent I_D is 30 mA.
Apply RF signal.

Bias-down Procedure
Turn off RF signal
Turn off V_D and wait 1 second to allow drain capacitor dissipation
Turn off V_G

0.03–3.0 GHz Evaluation Board Layout

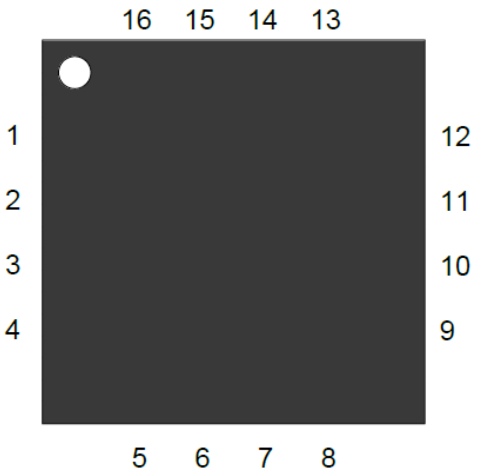
Top RF layer is 0.020” thick Rogers RO4350B, ε_r = 3.48. The pad pattern shown has been developed and tested for optimized assembly at Qorvo Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances.

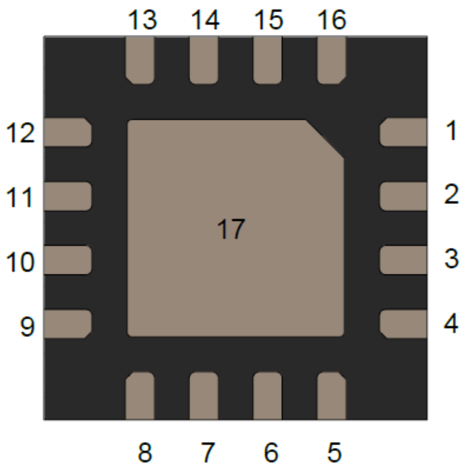


0.03–3.0 GHz EVB Bill of Materials

Reference Des.	Value	Qty	Manuf.	Part Number
C1, C2, C5, C6	2400 pF	4	Knowles Novacap	C08BL242X-5UN-X0T
C3	0.2 pF	1	AVX	600S0R2AT250XT
C4, C7	10 uF	2	Murata	LLL31MR60J106ME01L
C8	1 uF	1	AVX	18121C105KAT2A
C9	220 uF	1	United Chemi-con	EMVY500ADA221MJA0G
L1	2 nH	1	CoilCraft	0603CT-2N0XJRW
L2, L5	82 nH	2	CoilCraft	1008CS-820XGLB
L3, L6	100 nH	2	CoilCraft	1008CS-101XGLB
L4, L7	900 nH	2	CoilCraft	1008AF-901XJLB
R1	499 Ω	1	VISHAY	CRCW0603499RFKEA
R2, R3, R4, R5	402 Ω	4	VISHAY	CRCW0805402RFKEA
R6	1 kΩ	1	VISHAY	CRCW06031K00FKEA

Pin Layout



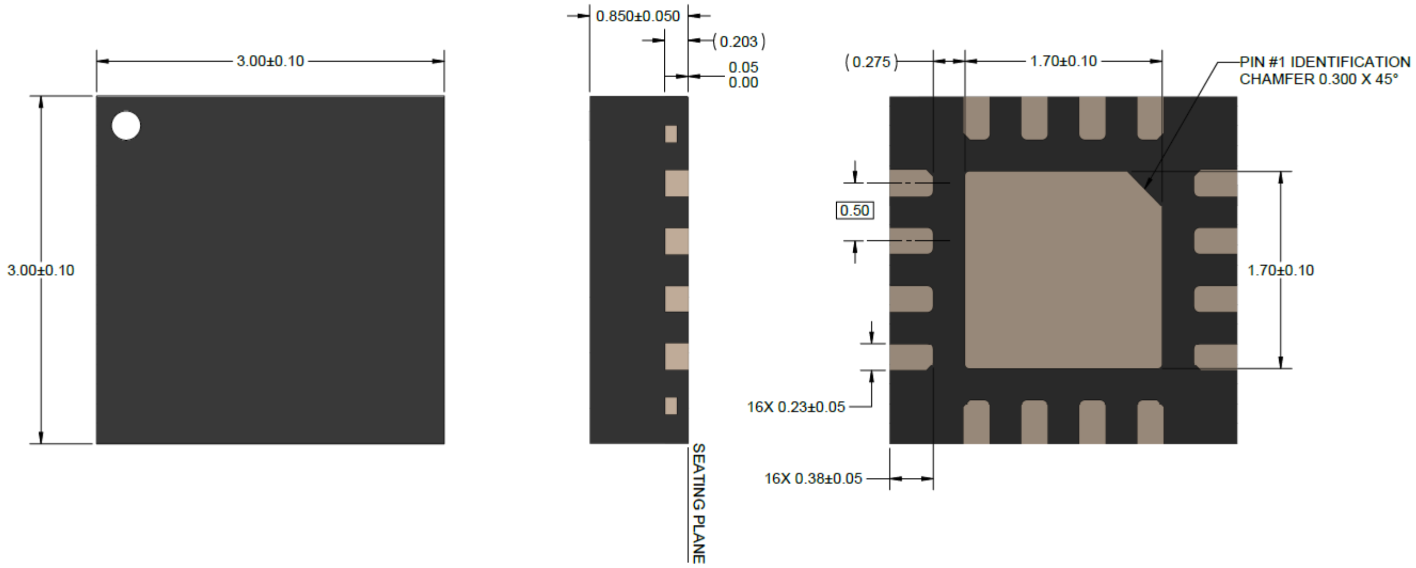


Pin Description

Pin Number	Symbol	Description
3	V_G/RF IN	Gate voltage / RF Input to be matched to 50 ohms
10, 11	V_D/RF OUT	Drain voltage / RF Output to be matched to 50 ohms
1, 2, 4-9, 12-16	GND	Ground
6	BYP	Off-chip capacitor to extend low-frequency gain
17	GND	Source connected to ground

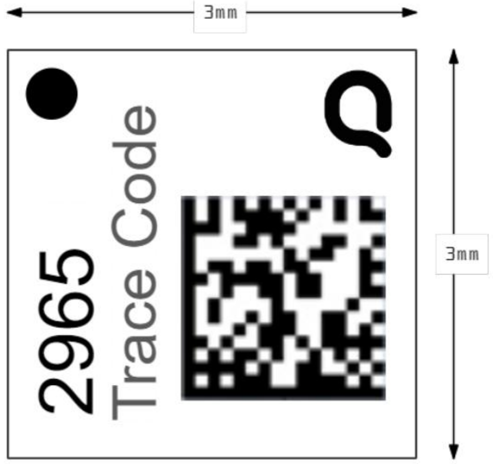
Mechanical Dimensions and Marking Diagram

All dimensions are in millimeters.



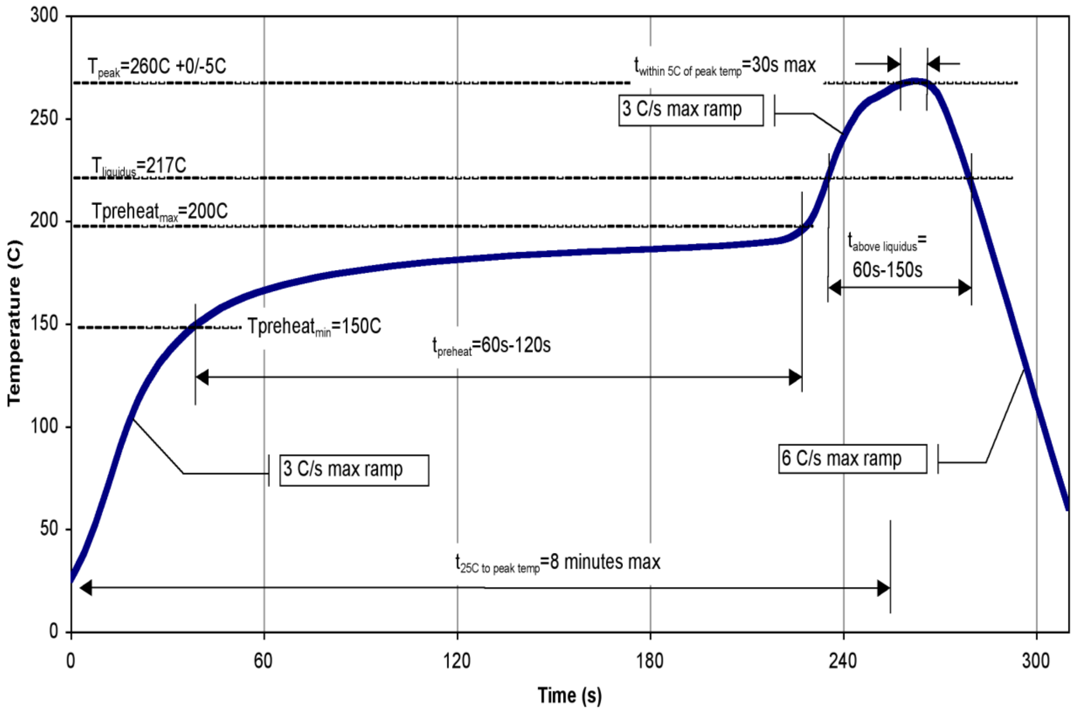
Notes:

1. Unless otherwise noted, all dimension tolerances are +/- 0.100 mm.
2. Package leads are gold plated.
3. Part is mold encapsulated.



● Pin 1 Indicator
Qorvo Logo - Use Q5D
Trace Code to be assigned by SubCon

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B 500V	ANSI/ESDA/JEDEC JS-001
ESD – Charge Device Model (CDM)	Class C3 1000V	ANSI/ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL3	IPC/JEDEC/J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260 °C max. reflow temp.) and tin/lead (245 °C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu Au thickness is 0.00254 µm min.

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Qorvo:

Web: www.qorvo.com **Tel: 1-844-890-8163** **Email:** customer.support@qorvo.com

For technical questions and application information:

Email: info-products@qorvo.com

Important Notice

The information contained herein is believed to be reliable; however, Qorvo makes no warranties regarding the information contained herein and assumes no responsibility or liability whatsoever for the use of the information contained herein. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for Qorvo products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information. **THIS INFORMATION DOES NOT CONSTITUTE A WARRANTY WITH RESPECT TO THE PRODUCTS DESCRIBED HEREIN, AND QORVO HEREBY DISCLAIMS ANY AND ALL WARRANTIES WITH RESPECT TO SUCH PRODUCTS WHETHER EXPRESS OR IMPLIED BY LAW, COURSE OF DEALING, COURSE OF PERFORMANCE, USAGE OF TRADE OR OTHERWISE, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE**.

Without limiting the generality of the foregoing, Qorvo products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.