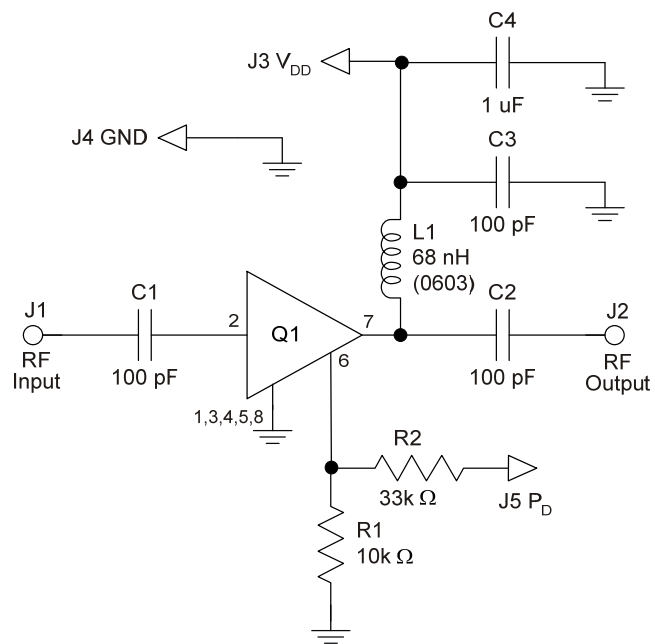
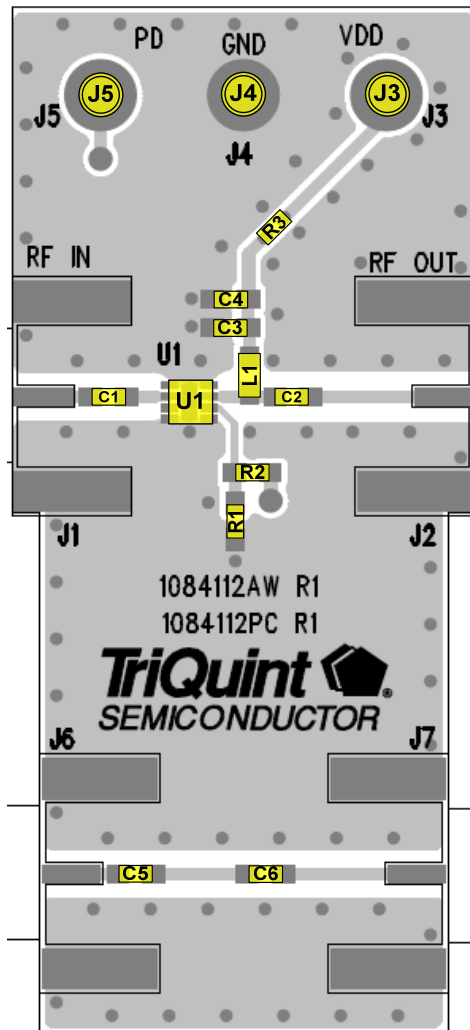


TQP3M9036

Ultra Low Noise, High Linearity LNA



Application Circuit Configuration



Notes:

1. See PC Board Layout, page 5 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. R3 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. All components are of 0402 size unless stated on the schematic.
5. C1, C2, and C3 are non-critical values. The reactive impedance should be as low as possible at the frequency of operation for optimal performance.
6. The L1 value is non-critical and needs to provide high reactive impedance at the frequency of operation.
7. R1 and R2 are optional and do not need to be loaded if the shut-down functionality is not needed; i.e. FDD applications. If R1 and R2 are not loaded, the LNA will operate in its standard "ON" state.
8. A through line is included on the evaluation board to de-embed the board losses.

Bill of Material

Reference Des.	Value	Description
U1	n/a	TQP3M9037 Amplifier, 2x2 SLP Package
R1	10K Ω	Resistor, Chip, 0402, 5%, 1/16W
R2	33K Ω	Resistor, Chip, 0402, 5%, 1/16W
R3	0 Ω	Resistor, Chip, 0402, 5%, 1/16W
L1	68 nH	Inductor, 0603, 5%, Ceramic
C4	1.0 uF	Cap., Chip, 0402, 10%, 10V, X5R
C1, C2, C3, C5, C6	100 pF	Cap., Chip, 0402, 5%, 50V, NPO/COG
J3, J4, J5	n/a	Solder Turret