QM81050

Boost-Buck PMIC for Mobile Applications

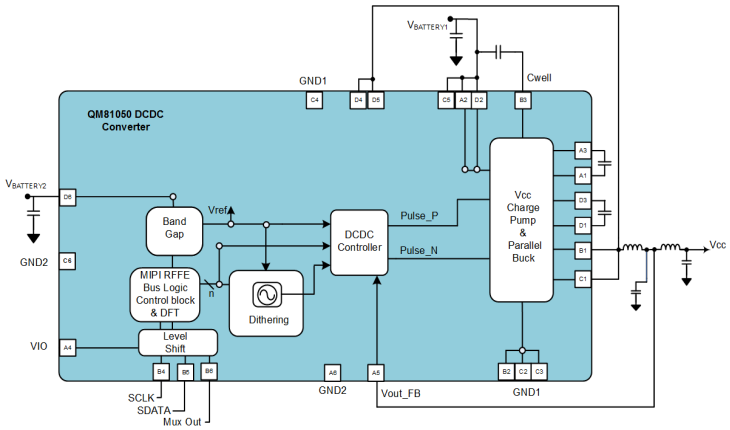
Product Overview

The QM81050 is a power management unit with a boost-buck DCDC converter designed for use in conjunction with power amplifiers in a multi-mode 3G/4G/5G handheld system. It can also support HPUE/PC2 operation.

The boost-buck mechanism of the DCDC converter allows for operation in a wide range of supply voltages, while still maintaining system performance such as linearity, output power, and high efficiency. The converter has a fast response to load and line transients. It supplies an output voltage with minimal ripple over a wide output voltage range.

Package: WLCSP, 2.48mm x 1.77mm x 0.67mm

Functional Block Diagram



Key Features

- Uses a Boost-Buck Architecture
- High Efficiency Over Various Loads
- Variable Output Voltage: 0V to 5.5V
- MIPI® RFFE Programmable Control Interface

Applications

- 3G/4G/5G Multimode, Multiband Handsets, Data Cards
- HPUE/PC2 Handsets, Data Cards

Ordering Information

Part Number	Description
QM81050SR	DCDC Converter IC Sample Reel
QM81050TR13-5K	DCDC Converter IC 5000 pcs Reel

Absolute Maximum Ratings

Parameter	Ratings	Units
VBATTERY1 Supply Voltage (1) (Standby, Idle, and Operating Modes)	-0.3 to +6.0	V
VBATTERY2 Supply Voltage (1) (Standby, Idle, and Operating Modes)	-0.3 to +6.0	V
Storage Temperature (Non-Operational)	-40 to +125	°C

Note: Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit	Conditions
Overall					
Extended Operating Temperature Range (Operational)	-30	-	85	°C	
IBATT Leakage Current	-	-	10	µA	VBATTERY1,2 = 3.6V, VIO = 0V, No load, Room Temperature
IBATT Idle Current	-	-	10	µA	VBATTERY1,2 = 3.6V, VIO = 1.8V, No Load, No MIPI RFFE R/W, Room Temperature
UVLO (Under voltage Lockout)	2.5	-	-	V	
OVP (Over voltage Protection)	-	-	6.35	V	OVP has a DAC clamp that cannot exceed what's programmed (>6.35V is default)
OCP (Over current Protection)	-	-	TBD	A	Over current protection coupled with Over temperature protection.
Maximum Output Load current – Buck Mode	1	-	-	A	Vcc < 3.4V
Maximum Output Load current – Boost Mode	1.4	-	-	A	3.4V ≥ Vcc ≤ 5.5V
Switching Frequency	0.125	-	7.875	MHz	
Boost-Buck Converter Electrical Interface					
VBATTERY1 Supply Voltage (1)	2.5	3.6	5.1	V	VCC performance will be degraded at VBATTERY1 = 2.5V - 2.9V
VBATTERY2 Supply Voltage (1)	2.5	3.6	5.1	V	VCC performance will be degraded at VBATTERY2 = 2.5V - 2.9V
VCC Output Voltage Range	0	-	5.5	V	VBATTERY1,2 ≥ 3.4V
Efficiency - Boost Mode	-	85.5	-	%	VBATTERY1,2 = 4V, VCC = Vdac = 4.2V, ILOAD = 1200mA;
	-	86.5	-	%	VBATTERY1,2 = 3.6V, VCC = Vdac = 5.5V, ILOAD = 1400mA;
	-	85.5	-	%	VBATTERY1,2 = 3.6V, VCC = Vdac = 4.85V, ILOAD = 500mA;
	-	84.5	-	%	VBATTERY1,2 = 3.6V, VCC = Vdac = 3.9V, ILOAD = 500mA;
Efficiency - Buck Mode	-	93	-	%	VBATTERY1,2 = 4V, VCC = Vdac = 3.4V, ILOAD = 650mA;
	-	90.5	-	%	VBATTERY1,2 = 3.6V, VCC = Vdac = 2.45V, ILOAD = 200mA;

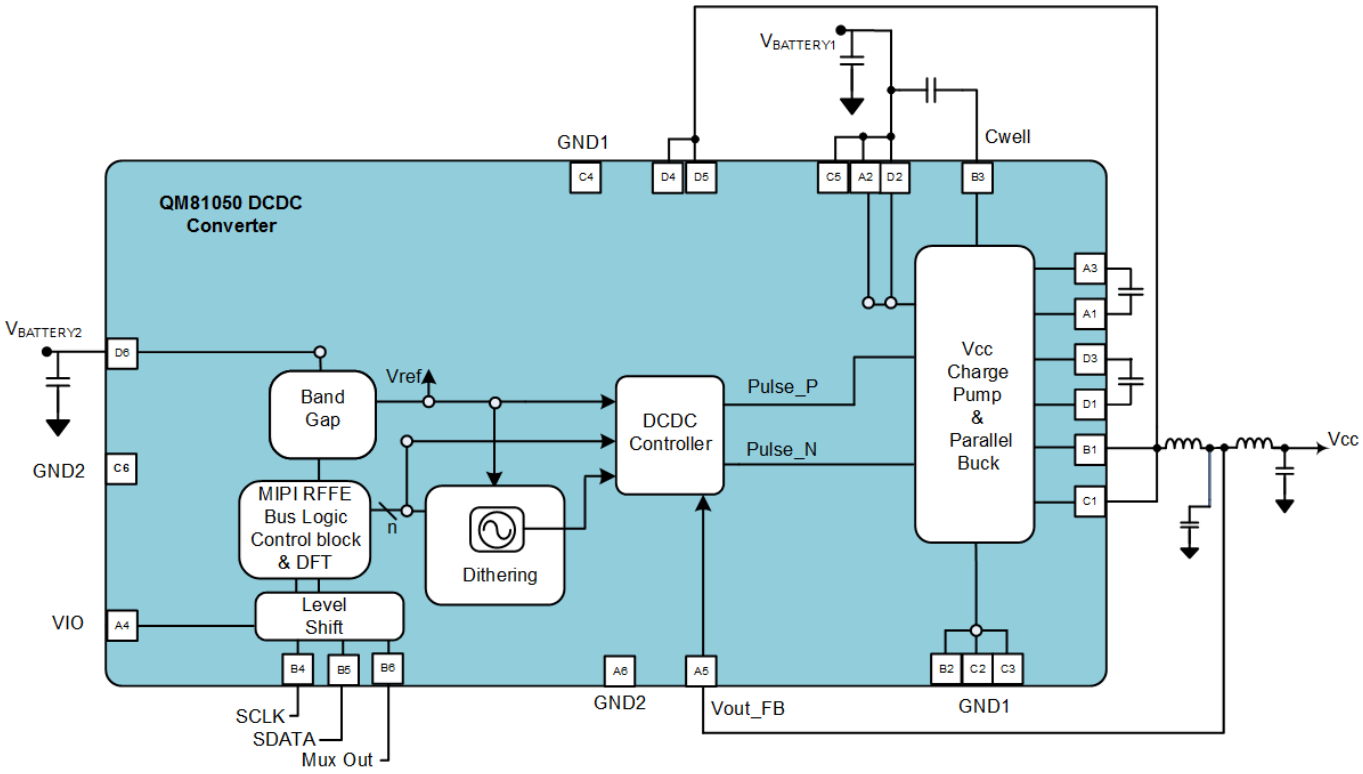
Parameter	Min.	Typ.	Max.	Unit	Conditions
Boost-Buck Converter Electrical Interface					
Initial Start Up Time	-	-	20	µs	At device power-on
Vout(VCC) Transition time – 1V to 5.5V	-	-	10	µs	10% to 90%
Vout(VCC) Transition time – 1V transitions	-	6	-	µs	10% to 90%
Transient response - Load	-	100	TBD	mV	2MHz switching frequency
Transient response - Line	-	-	100	mV	2MHz switching frequency
Accuracy - Load	-	-	5	%	
Accuracy - Line	-	-	5	%	
Output Capcitance	-	-	10	µF	For <15µs rise time, the maximum capacitance allowed on the output should be <10µF. This translates to 2.2µF + 0.68µF from converter side capacitors and 2.2uF + 4.7uF from PA side capacitors.

Note 1: VBATTERY1 and VBATTERY2 are intended to be tied to the same supply and need to be kept at the same potential, or permanent damage may occur.

Digital Interface Voltage and Timing Requirements					
VIO Supply Voltage	1.6	1.8	2	V	Externally supplied voltage that must be supplied the entire time the device is operational. Internally level shifted.
VIO Supply Current	-	-	5	mA	Master read operation.
	-	-	1.25	mA	Master write operation.
Input High Voltage	$0.7*V_{IO}$	-	V_{IO}	V	
Input Low Voltage	-0.3	-	$0.3*V_{IO}$	V	
Output High Voltage	$0.8V_{IO}$	-	V_{IO}	V	
Output Low Voltage	-0.3	-	$0.2*V_{IO}$	V	
Clock Frequency	0.1	-	55	MHz	
Clock Duty Cycle	45	50	-	%	

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Detailed Functional Block Diagram



Pin Configuration and Description

Pin Number	Label	Description
A1	cb_h	Main charge-pump phase "b" fly capacitor positive connection
B1	L	PWM output to be connected to external power inductor
C1	L	PWM output to be connected to external power inductor
D1	ca_h	Main charge-pump phase "a" fly capacitor positive connection
A2	VDD	Battery supply connection for high power charge-pump phase "b"
B2	GND	Ground return for the high power charge-pump phase "b"
C2	GND	Ground return for the high power charge-pump phase "a"
D2	VDD	Battery supply connection for high power charge-pump phase "a"
A3	cb_l	Main charge-pump phase "b" fly capacitor negative connection
B3	pbulk	Holding capacitor for CMOS substrate
C3	GND	Ground return for the high power charge-pump phase "a"
D3	ca_l	Main charge-pump phase "a" fly capacitor negative connection
A4	vio	Serial interface supply
B4	sclk	Serial interface clock input
C4	GND	Ground return for the pump
D4	Lbuck	PWM output to be connected to external power inductor
A5	Vout_fb	Voltage feedback input for the high power charge-pump
B5	sdata	Serial interface data I/O
C5	VDD	Battery supply for the pump
D5	Lbuck	PWM output to be connected to external power inductor
A6	GNDA	GND for the analog
B6	Mux_out	Mixed-signal MUX output
C6	GNDA	Ground return for quiet side of chip. Used for circuits other than the Main Charge Pump
D6	VDDA	Battery supply connection for CMOS circuitry

Register Map

Register 2, Addr: 0x02					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7	DeviceEN	Enables the support circuitry 0 = Turns OFF the bandgap, voltage references, and clock generator 1 = Turns ON the bandgap, voltage references, and clock generator	0	0 - 2	R/W
6:0	Vdac[6:0]	Vdac[6:0] defines the output voltage the part will seek to deliver. It's step resolution (the lsb of this voltage DAC output) is 50mV	000 0000	0 - 2	R/W

Register 3, Addr: 0x03					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7:6	MainCPModes[1:0]	Main Charge-Pump operating modes 00 = Ultra Low Power Mode (Buck DCM Mode) 01 = Buck Mode (Buck CCM Mode) 10 = Reserved 11 = High Power (Boost Mode)	00	0 - 2	R/W
5:0	Fminb[5:0]	Switcher Frequency Setting definition depends upon other register bit settings as defined below. This table reflects the routing of these bits throught the digital truth table. Dithering Disabled, SemiAuto=0, FullAuto_EN=0: switcher frequency (single frequency mode) Dithering Disabled, SemiAuto=1 OR FullAuto_EN=1: switcher frequency for Buck-Only CCM mode Dithering Enabled, SemiAuto=0, FullAuto_EN=0: switcher Fmin for dithering control Dithering Enabled, SemiAuto=1 OR FullAuto_EN=1: switcher Fmin for dithering control Binary weighted frequency with lsb = ~0.125 MHz. 0b000000 = 0.125 MHz	11 1110	0 - 2	R/W

Register 4, Addr: 0x04					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
5:0	Fminp[5:0]	Switcher Frequency Setting depends upon other register bit settings as defined below. This table reflects the routing of these bits throught the digital truth table. Dithering Disabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Disabled, SemiAuto=1 OR FullAuto_EN=1: switcher frequency for Pump-Buck mode Dithering Enabled, SemiAuto=0, FullAuto_EN=0: switcher Fmax for dithering control Dithering Enabled, SemiAuto=1 OR FullAuto_EN=1: switcher Fmin for dithering (Pump-Buck) Binary weighted frequency with lsb = ~0.125 MHz. 0b000000 = 0.125 MHz	11 1111	0 - 2	R/W

Register 5, Addr: 0x05					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
5:0	Fmind[5:0]	Switcher Frequency Setting depends upon other register bit settings as defined below. This table reflects the routing of these bits throught the digital truth table. Dithering Disabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Disabled, SemiAuto=1 OR FullAuto_EN=1: switcher frequency for Buck-Only DCM mode Dithering Enabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Enabled, SemiAuto=1 OR FullAuto_EN=1: switcher Fmin for dithering (Buck DCM) Binary weighted frequency with lsb = ~0.125 MHz. 0b000000 = 0.125 MHz	11 1111	0 - 2	R/W

Register 6, Addr: 0x06					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
5:0	Fmaxb[5:0]	Switcher Frequency Setting depends upon other register bit settings as defined below. This table reflects the routing of these bits throught the digital truth table. Dithering Disabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Disabled, SemiAuto=1 OR FullAuto_EN=1: Not Used Dithering Enabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Enabled, SemiAuto=1 OR FullAuto_EN=1: switcher Fmax for dithering (Buck CCM) Binary weighted frequency with lsb = ~0.125 MHz. 0b000000 = 0.125 MHz	11 1111	0 - 2	R/W

Register 7, Addr: 0x07					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
5:0	Fmaxp[5:0]	Switcher Frequency Setting depends upon other register bit settings as defined below. This table reflects the routing of these bits throught the digital truth table. Dithering Disabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Disabled, SemiAuto=1 OR FullAuto_EN=1: Not Used Dithering Enabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Enabled, SemiAuto=1 OR FullAuto_EN=1: switcher Fmax for dithering (Pump-Buck) Binary weighted frequency with lsb = ~0.125 MHz. 0b000000 = 0.125 MHz	11 1111	0 - 2	R/W

Register 8, Addr: 0x08					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7	BuckDCM1x_EN	Enables reduction to 1x Buck FETS when in DCM mode 0 = Disabled (3x Buck FETS always) 1 = Enabled (1x Buck FETS when in DCM mode)	0	0 - 2	R/W
5:0	Fmaxd[5:0]	Switcher Frequency Setting depends upon other register bit settings as defined below. This table reflects the routing of these bits throught the digital truth table. Dithering Disabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Disabled, SemiAuto=1 OR FullAuto_EN=1: Not Used Dithering Enabled, SemiAuto=0, FullAuto_EN=0: Not Used Dithering Enabled, SemiAuto=1 OR FullAuto_EN=1: switcher Fmax for dithering (Buck DCM) Binary weighted frequency with lsb = ~0.125 MHz. 0b000000 = 0.125 MHz	11 1111	0 - 2	R/W

Register 9, Addr: 0x09					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7	SemiAuto_EN	Enables SemiAuto mode. When Enabled, if the programmed Vdac[6:0] is less than or equal to the SemiAuto_Vdac_Thresh[6:0], then the part will automatically switch into Buck Only mode, regardless of the MainCPModes[1:0] selected. 0 = Disabled (OFF) 1 = Enabled (ON)	1	0 - 2	R/W
6:0	SemiAutoVth_pump[6:0]	Threshold used for SemiAuto Mode determination	100 0100	0 - 2	R/W

Register 10, Addr: 0x0A					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7	AutoBuckDCM_EN	Enables AutoBuckDCM mode. When Enabled, if the programmed Vdac[6:0] is less than or equal to the AutoBuckDCM_Vdac_Thresh[6:0], then the part will automatically switch into Buck Only DCM mode, regardless of the MainCPModes[1:0] selected. 0 = Disabled (OFF) 1 = Enabled (ON)	1	0 - 2	R/W
6:0	AutoBuckDCMVth_dcm[6:0]	Threshold used for AutoBuckDCM Mode determination	000 1010	0 - 2	R/W

Register 12, Addr: 0x0C					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7:5	DitheringCtrl[2:0]	Dither Control Selection 000 = Dithering OFF (Switching Frequency set by Fmin[5:0] 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = 3D Dithering (Slow random & Fast Linear) 110 = Reserved for future use 111 = Reserved for future use	000	0 - 2	R/W
4	ProtectionCktsEN	Enable Protection Circuits. When this bit is 1 (asserted), then protections will start reporting their status. Shutdown only occurs if specific protections are also enabled (asserted) below. 0 =Protections Circuits are off 1 = Protection Circuits are on	1	0 - 2	R/W
3	OverTempEN	Enable Over-Temperature Protections. 0 = Over-Termperature Protections (shutdown when device over temperature) are disabled, 1 = Over-Temperature Pretections are enabled/operating **Note: When DeviceEn = 0, this bit's default is 0. When DeviceEn is set high, this bit will automatically turn itself to 1.**	1	0 - 2	R/W
2	ShortCircuitEN	Enable Short-Circuit Protections. 0= Short-Circuit Protections (shutdown when device seems to be a short-circuit or is sourcing extremely excessive current) are disabled, 1 = Short-Circuit Pretections are enabled/operating **Note: When DeviceEn = 0, this bit's default is 0. When DeviceEn is set high, this bit will automatically turn itself to 1.**	1	0 - 2	R/W
1	LowVbatProtectEN	Do not change from Power-On default	0	0 - 2	R/W
0	BGVoltProtectEN	Do not change from Power-On default	0	0 - 2	R/W

Register 13, Addr: 0x0D					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
1	SoftOff_EN	Enable softoff. Lowers undershoot when device is turned off.	0	0 - 2	R/W
0	UVLo_EN	Enables UnderVoltage Protections (shutdown part when Vbat < 2.5V) 0 = Disabled 1 = Enabled	0	0 - 2	R/W

Register 15, Addr: 0x0F					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7	Vdac_Clamp_EN	Enables the Vdac Clamp 0 = Disabled 1 = Enabled	0	0 - 2	R/W
6:0	Vdac_Clamp[6:0]	Vdac Clamp setting. When enabled, prevents the Vdac from going above this setting	111 1111	0 - 2	R/W

Register 20, Addr: 0x14					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7	HotProtectionHalt (hot_fault)	Extreme Over-Temperature Shutdown Event. 0 = Over-Termperature Protections (shutdown when device over temperature) are disabled 1 = Over-Temperature Pretections are enabled/operating	0	No	R
6	HiCurProtectionHalt (hiCur_fault)	Extreme Current Shutdown Event. 0 = Over-Termperature Protections (shutdown when device over temperature) are disabled 1 = Over-Temperature Pretections are enabled/operating	0	No	R
3	UVLoHalt	Undervoltage protection circuit	0	No	R
1	DeviceHot	Over-Temperature Condition Detected. 1 = Over-Temperature Condition Detected & Device is in Shutdown Protections Mode, 0 = All seems OK. NOTE: This is a latched bit, meaning if a "1" is detected on the input at any time, then that "1" is latched into this output. This bit is reset to its default value whenever Vspi is toggled.	0	No	R
0	DeviceWarm	Short-Circuit Condition Detected. 1 = Short Circuit Condition Detected & Device is in Shutdown Protections Mode, 0 = All seems OK. NOTE: This is a latched bit, meaning if a "1" is detected on the input at any time, then that "1" is latched into this output. This bit is reset to its default value whenever Vspi is toggled.	0	No	R

Register 28, Addr: 0x1C					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7:6	PWR_MODE[1:0]	00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: LOW POWER - Retain register values, Antenna in isolation 11: Reserved Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.	10	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.	000	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.	000	No	R/W

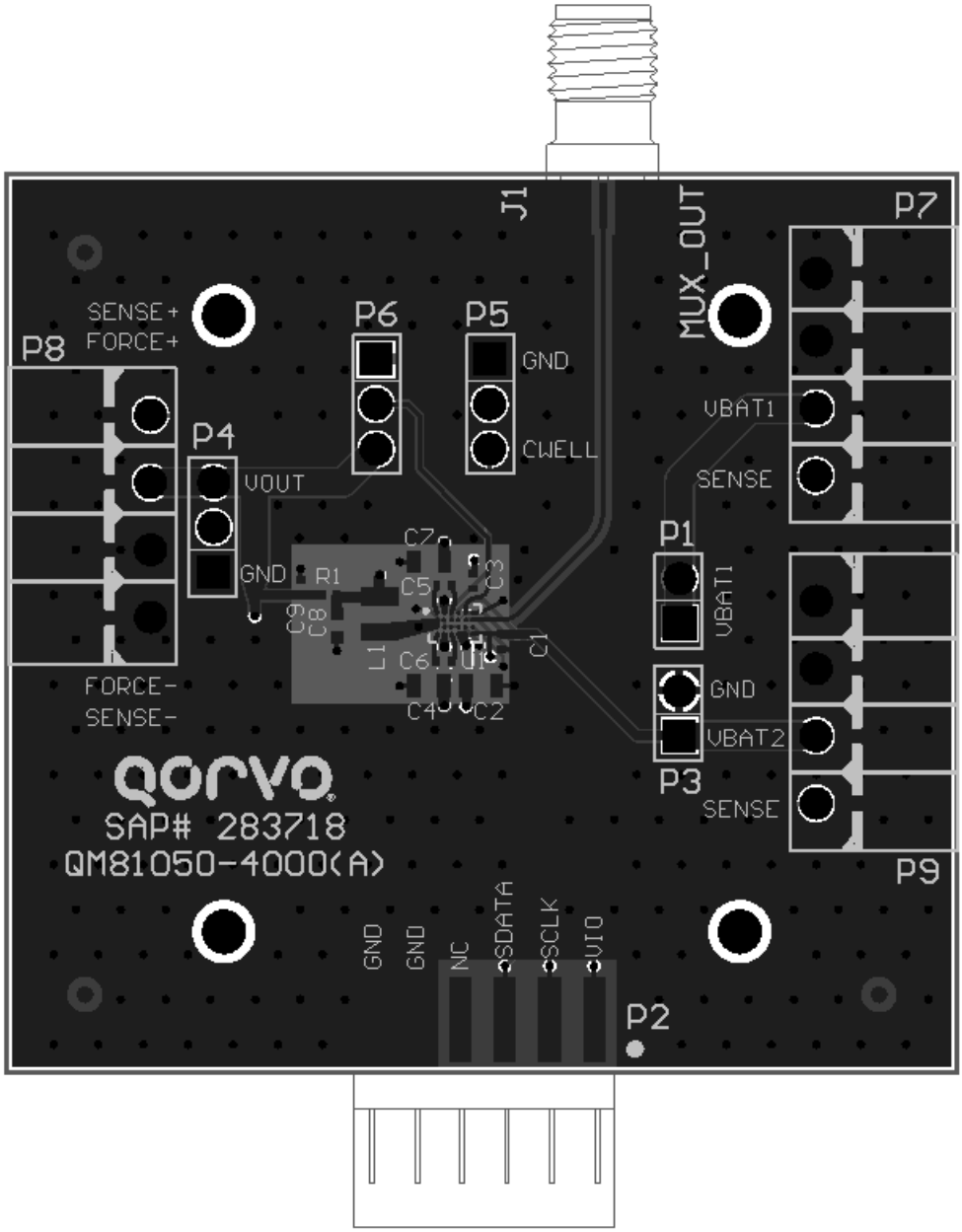
Register 29, Addr: 0x1D					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7:0	PROD_ID[7:0]	Lower eight bits of Product Number Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.8.3 for details.	0000 0001	No	R

Register 30, Addr: 0x1E					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7:0	MFG_ID_LSB[7:0]	Lower eight bits of MIPI Manufacturer ID Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.8.3 for details.	11000110	No	R

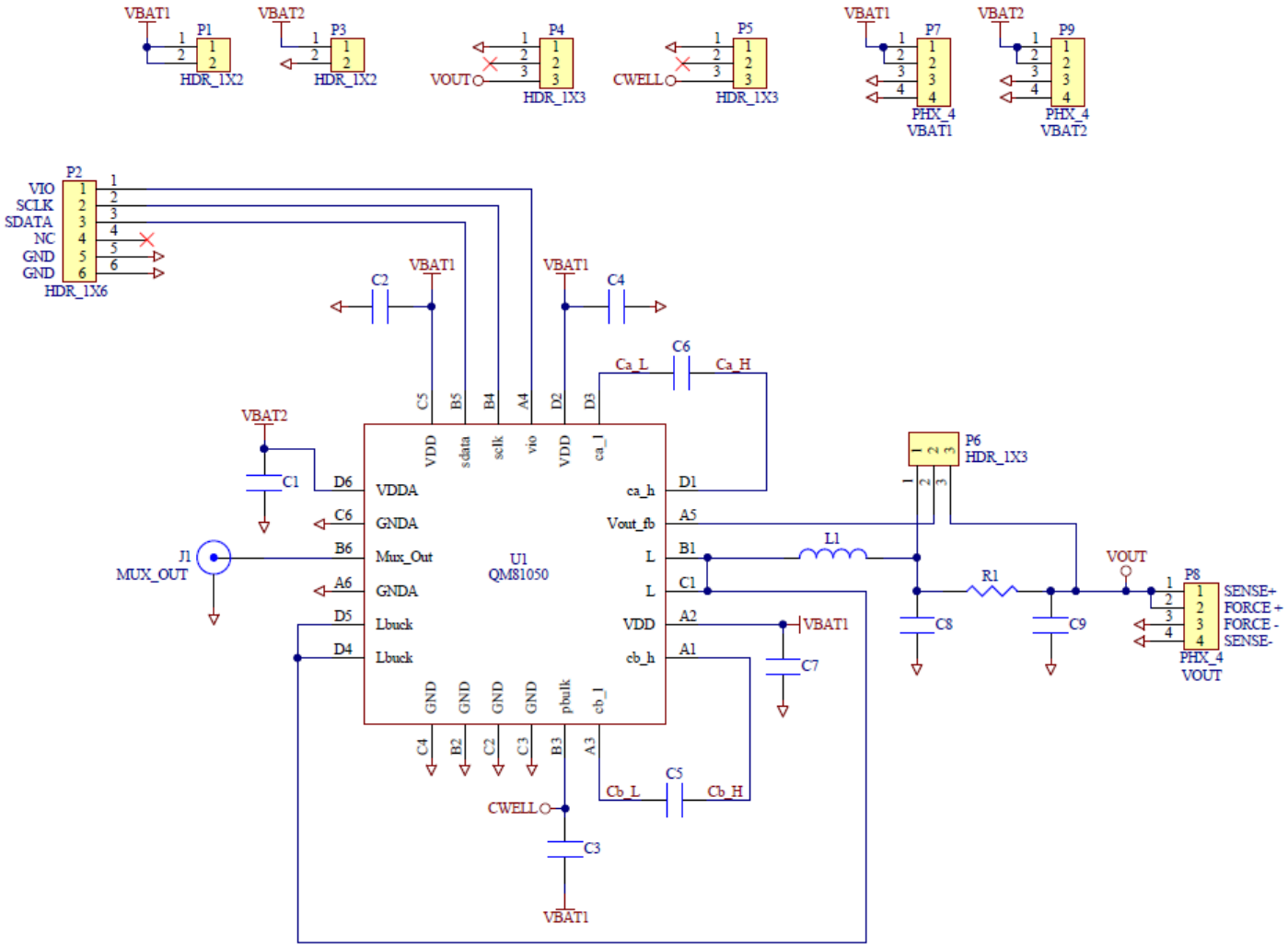
Register 31, Addr: 0x1F					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
7:6	Reserved_Reg31[7:6]	These are read-only bits that are reserved and yield a value of 00 at readback.	00	No	R
5:4	MFG_ID_MSB[9:8]	Upper two bits of MIPI Manufacturer ID Note: This is a read-only field. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this field, but does not update it. See MIPI 6.8.3 for details.	11	No	R
3:0	USID[3:0]	Programmable Unique Slave ID Note: USID is only writeable using a special programming sequence. See MIPI 6.8.3 for details.	0101	No	R/W

Register 66, Addr: 0x42					
Bit(s)	**Field Name**	**Description**	**Default**	**Trig**	**R/W**
0	FuseLatch	set high to reload the eFUSE data into the Register Map. This bit now automatically resets to 0 and kicks off the complete loading of all eFUSE assiciated bit information	0	No	R/W

Evaluation Board Layout



Evaluation Board Schematic

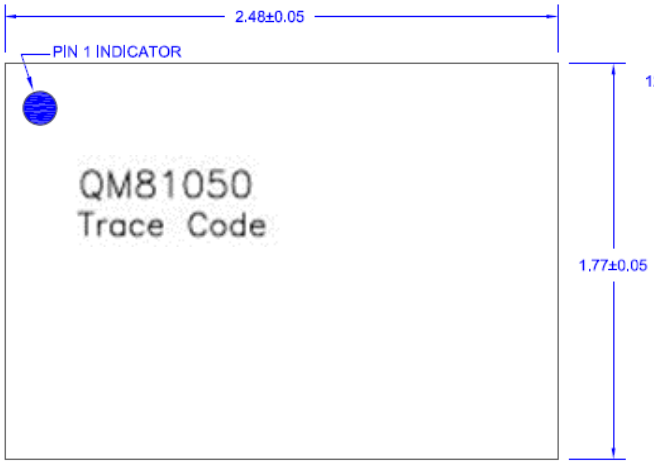


Evaluation Board Bill of Materials (BOM)

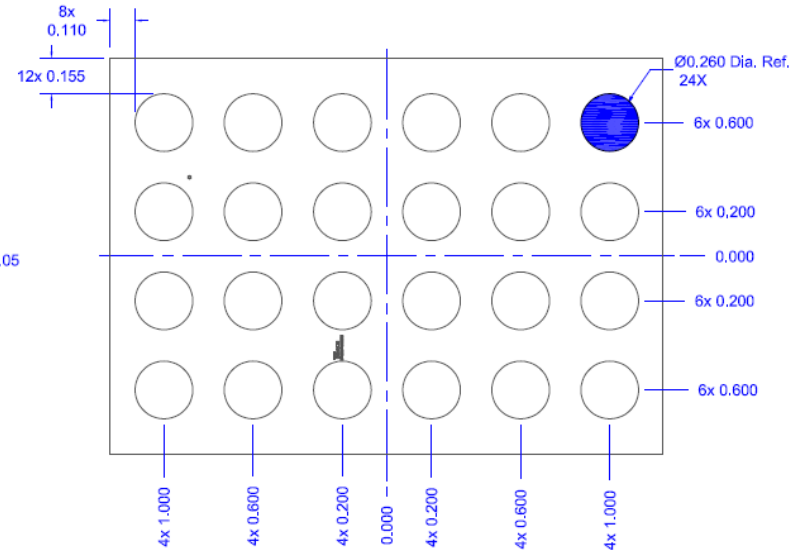
Reference Designator	Case Size	Value	Comments
C2, C4, C7	0805	10 uF	CAP, 10uF, 10%, 6.3V, X5R, 0805
C8	0603	2.2 uF	CAP, 2.2uF, 10%, 10V, X5R, 0603
C1	0402	1 uF	CAP, 1uF, 10%, 10V, X5R, 0402
C9	0402	0.68 uF	CAP, 0.68uF, 10%, 6.3V, X5R, 0402
C5, C6	0402	2.2 uF	CAP, 2.2uF, 20%, 6.3V, X5R, 0402
C3	0402	0.1 uF	CAP, 0.1uF, 10%, 50V, STD, 0402
R1	0402	0 ohm	RES, 0 OHM, 5%, 1/10W, 0402
L1	1008	1 uH	IND, PWR,1uH, 20%, 1.5A, 2x2.5x1.2mm,SMD

Package Outline and Branding Drawing

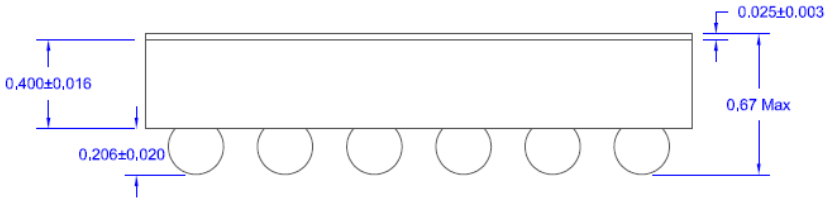
Dimension in millimeters.

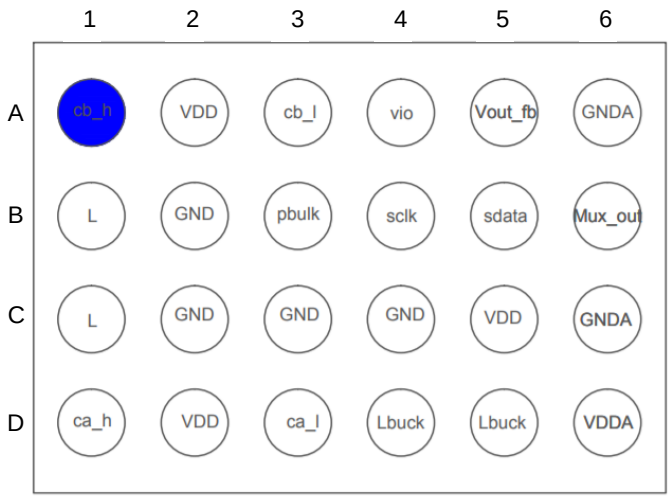


Top View Bumps Down

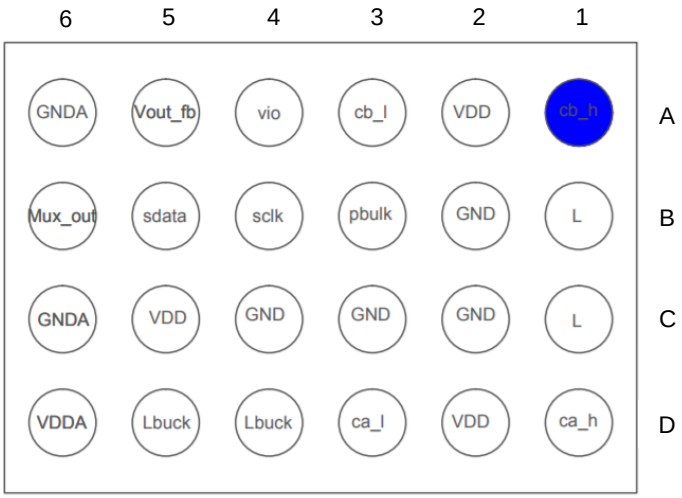


Bottom View Bumps Up





Top View Bumps Down



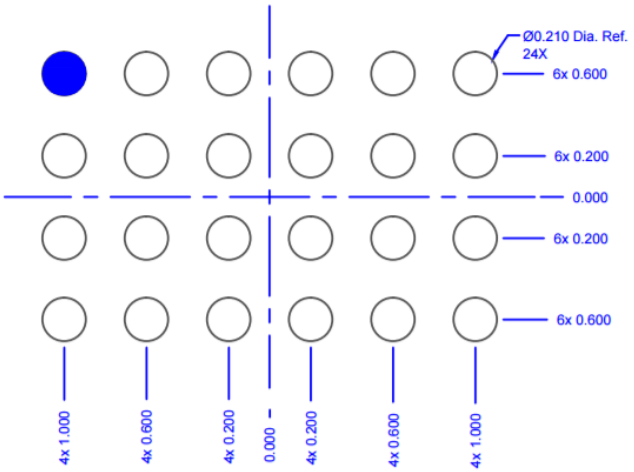
Bottom View Bumps Up

Notes:
1. Shaded area represents Pin 1 location.

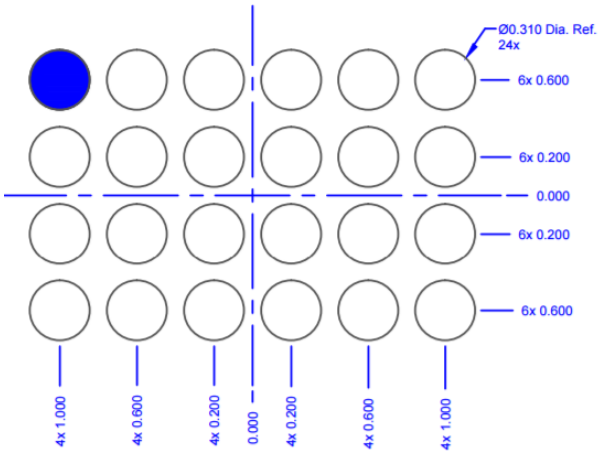
PCB Design Guidelines

PCB Metal Land and Solder Mask Pattern

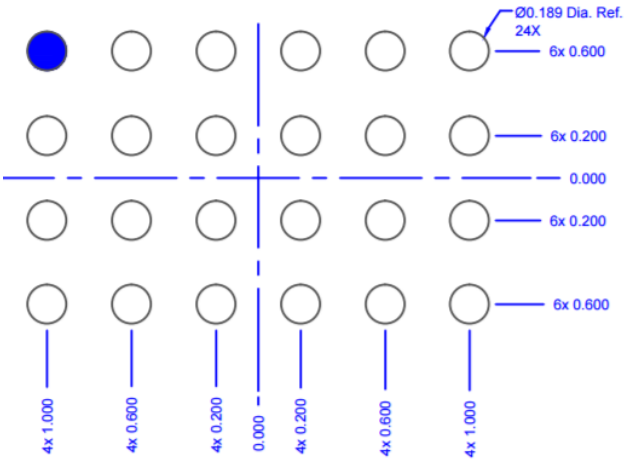
Dimension in millimeters



PCB METAL TOP VIEW



PCB SOLDERMASK TOP VIEW

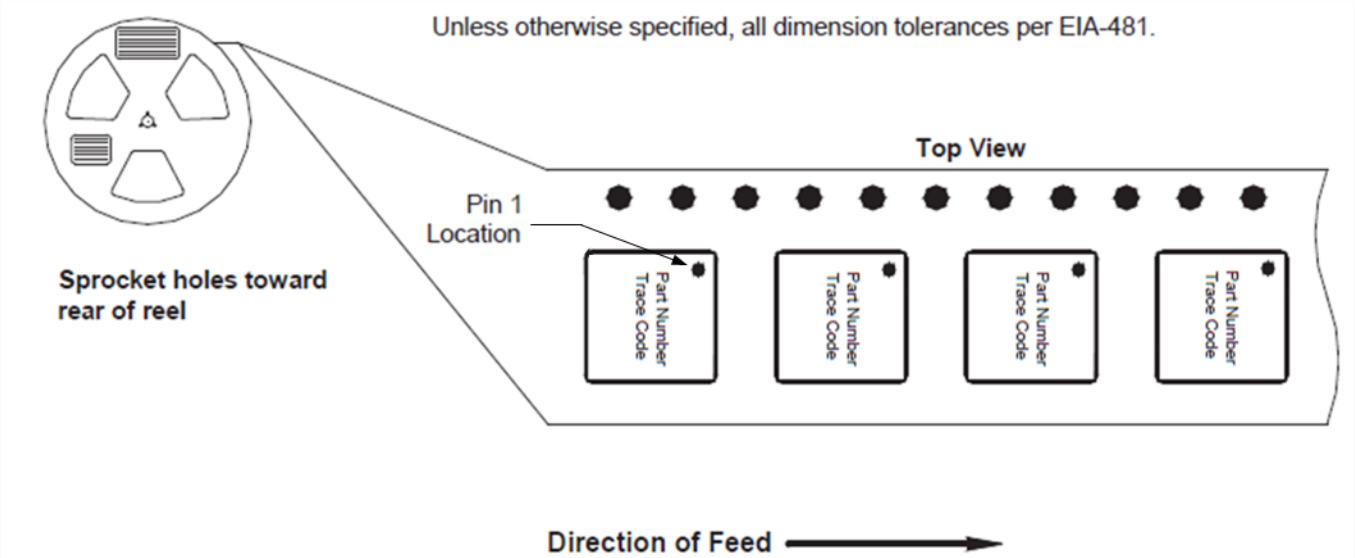


PCB STENCIL TOP VIEW

Notes:
1. Shaded area represents Pin 1 location.

Tape and Reel Information

Qorvo Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units Per Reel
QM81050TR13-5K	N/A	4 (102)	8	4	Single	5000



Tape and reel specifications for this part are also available on the Qorvo website.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESDA/JEDEC JS-001
ESD – Charge Device Model (CDM)	C3	ANSI /ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	MSL1	J-STD-020

Caution!

ESD sensitive device

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

REVISION HISTORY

REVISION	DATE	DESCRIPTION
A	2017-10-02	Initial Release
B	2017-10-18	Register map added
C	2017-11-22	Register map modified, Reg12 & Reg13
D	2018-05-25	Limits based on CM review
E	2018-08-13	Limits adjusted, updated pin mapping, updated ordering information
F	2018-10-08	Updated AMR table and Handling precautions
G	2019-03-18	Updated Pin descriptions and EVB schematic
H	2020-06-24	Updated POD and branding drawing, added CDM rating, added tape and reel info, added and modified parameters in operating conditions.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

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