Technical Brief 101

Verification of Thermal Simulations of GaAs FETs Using Liquid Crystal Measurements

Introduction

One important variable that determines the reliability of a FET device is the rise of the temperature within a transistor under bias. As shown in figure 1, as the temperature decreases, the mean time to failure of the device increases. Therefore, a device that reaches a lower temperature will have a longer lifespan. The relationship presented in Figure 1 can be determined by the Arrhenius equation [1], which is given below:

$$R = Ae^{\frac{-E_a}{kT}} \quad (1)$$

In this equation, R is the mean time to failure (usually expressed in hours), T is the operating temperature of the device in Kelvin, E_a is the activation energy in electron Volts (eV), k is Boltzmann's constant (~8.617×10^{-5} eV/K), and A is a scaling constant dependent on the specific device.

The difficulty of detecting the maximum temperature of a device causes difficulty for designers when attempting to lengthen the lifetime. There are a number of established methods for measuring device temperature such as liquid crystal and infrared testing, both of which detect heat changes within a device. Infrared testing can sense the absolute temperature over a small area, thereby allowing for a mapping of the temperature in space as demonstrated, for example, by Costrini [2]. However, infrared testing cannot easily resolve temperature difference over the sub-micron scale of typical FETs. Liquid crystal testing, on the other hand, can resolve temperature changes on a sub-micron scale and with better spatial accuracy [3]. Liquid crystal measurement utilizes a clearing point and can only determine when the temperature of the device has reached that temperature. Liquid crystal cannot provide a thermal map in the way that infrared can, but with proper laboratory preparation it can give very precise data. Close attention is paid to the area below the FET gates as discussed by Coccioli [4], as this area represents the main source of heat and therefore the location of the maximum junction temperature. As a result, liquid crystal is often the preferred method of thermal measurement.

Before a device is manufactured, it is impossible to perform the described tests. Therefore circuit designers must rely on simulation software to predict the temperature rise within FETs under bias or operation. There are a number of commercially available tools to perform these simulations. Often the most important simulation is the steady state temperature rise for a fixed background or baseplate temperature. In Figure 2, we present the output of one such steady state simulation for a Gallium Arsenide (GaAs) monolithic microwave integrated circuit (MMIC) with an area of 1 mm^2. This MMIC was biased at 5 V and 80 mA, and when the bottom of the MMIC was held at a constant 85 °C, the largest FET reached a maximum junction temperature of approximately 134 °C. We further note the temperature rise is well confined to the center gate area of this FET.

These simulation tools allow the user to enter many parameters pertaining to the FET. These include size and spacing of FET gates, the substrate properties, the epoxy used to attach the circuit to a housing or package, and the DC power dissipated by each FET device. It is imperative that these parameters are entered as accurately as possible to obtain a realistic result. The simulation tool then utilizes a mesher to discretize the calculations and produce a model.

Without proper verification of these simulations, the data cannot be fully trusted. Therefore it is important to compare measurements to simulated data. In this paper, we present a comparison of measurements to simulations of the maximum junction temperature for a number of GaAs FETs. We begin by describing the devices and presenting initial simulations which show a linear relationship between dissipated DC power and maximum temperature. We then describe the liquid crystal measurements used to determine the bias conditions necessary to achieve a specific maximum junction temperature. Next, we examine the accuracy of simulations of the FET devices under these measured bias conditions. Finally, we offer our conclusions.

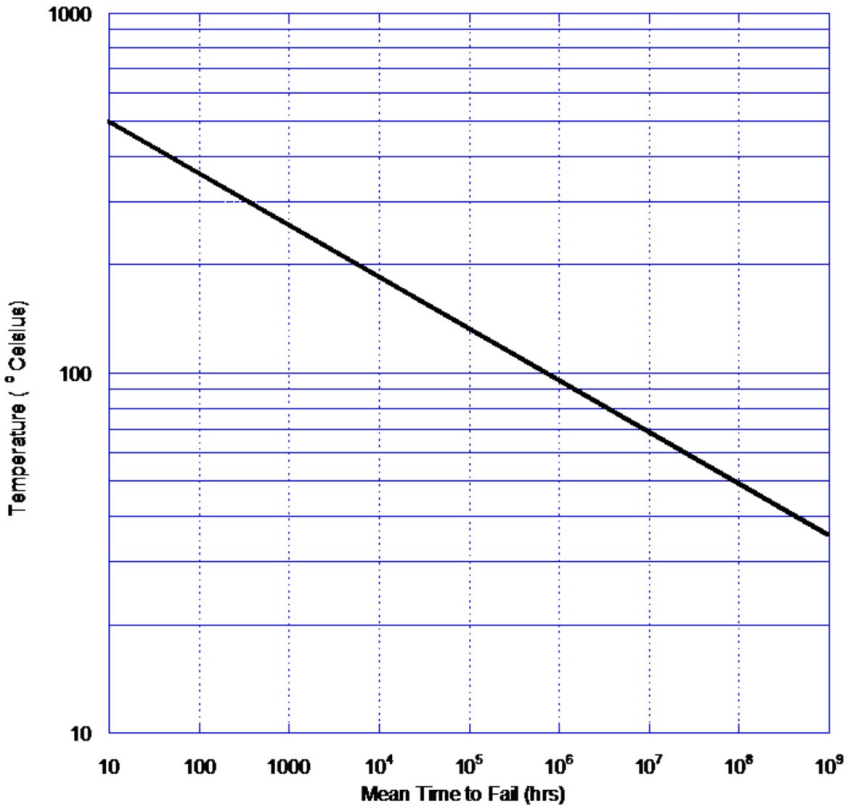

Figure 1: Arrhenius curve showing a typical relationship between maximum junction temperature of a device versus mean time to failure.

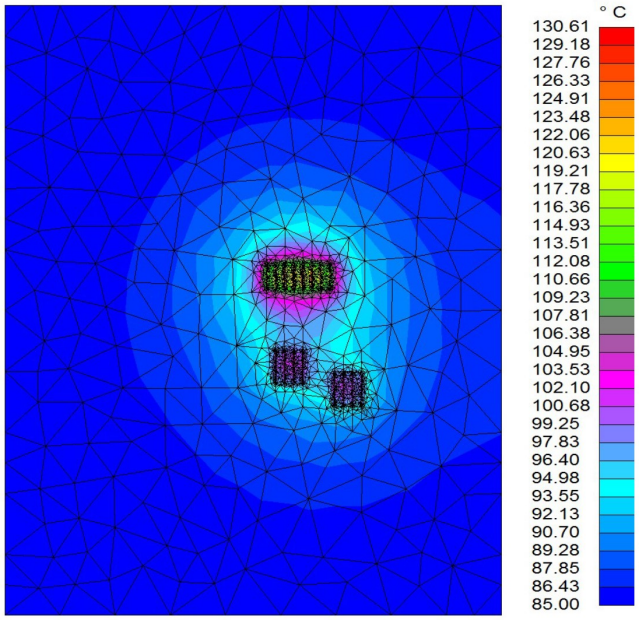

Figure 2: Output of a commercially available thermal simulation tool, with red corresponding as the hottest part of the device and blue as the coolest.

MMIC Test Devices

For this effort, we considered twelve common source FETs from two different GaAs pseudo-morphic HEMT (pHEMT) processes. The devices were fabricated on five unique MMICs and included both depletion and enhancement mode structures. A summary of these devices is presented below in Table 1. Backside vias were used to ground the sources, and each MMIC was plated with 5 um of gold on the backside.

Identifier	Process	FET type	FET size(s)	Gate Length	GaAs Thickness	Airbridges?
MMIC 1	pHEMT 1	Depletion	Q1: 8x80 um Q2: 12x100 um Q3: 6x120 um Q4: 6x170 um	0.2 um	70 um	None
MMIC 2	pHEMT 1	Depletion	Q1: 4x50 um Q2: 4x100 um	0.15 um	70 um	None
MMIC 3	pHEMT 1	Depletion	Q1: 8x50 um Q2: 8x50 um Q3: 8x50 um	0.15 um	70 um	Devices Q1 and Q3
MMIC 4	pHEMT 1	Depletion	Q1: 6x75 um Q2: 6x75 um	0.15 um	70 um	None
MMIC 5	pHEMT 2	Enhancement	Q1: 8x80 um	0.25 um	100 um	Device Q1

Table 1: List of GaAs MMIC devices used in this study.

Photographs of each MMIC are presented below in Figures 3 through 7. For size, we note the ground bond pads are approximately 100 um x 100 um in size.

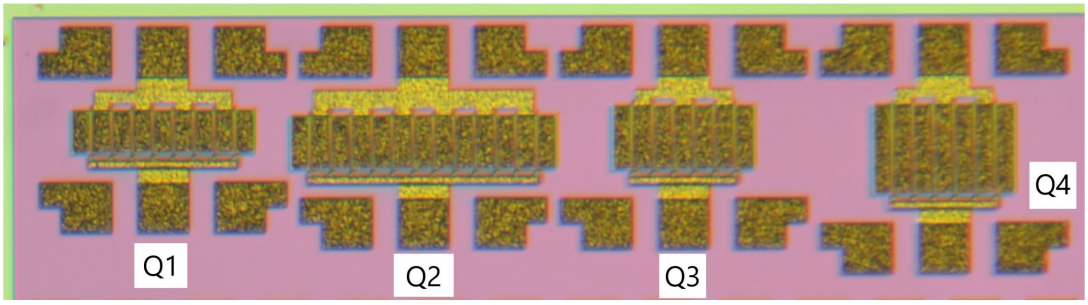

Figure 3: Die photograph of MMIC 1 with four devices, Q1-Q4.

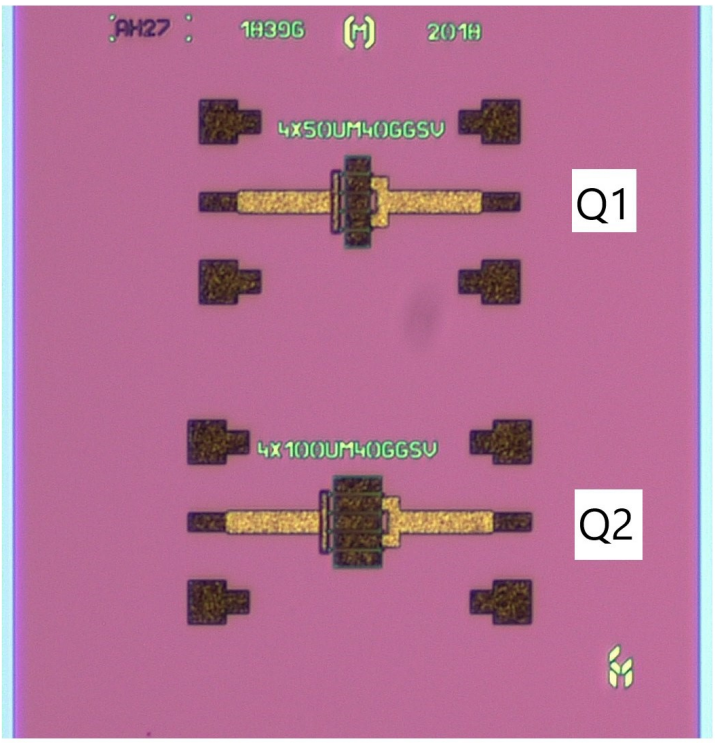

Figure 4: Die photograph of MMIC 2 with two devices, Q1 and Q2.

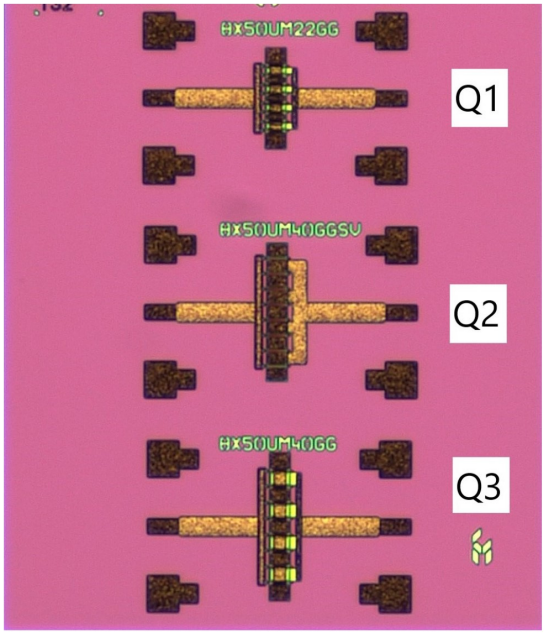

Figure 5: Die photograph of MMIC 3 with three devices, Q1-Q3. Devices Q1 and Q3 contain airbridges, which are present in the photo.

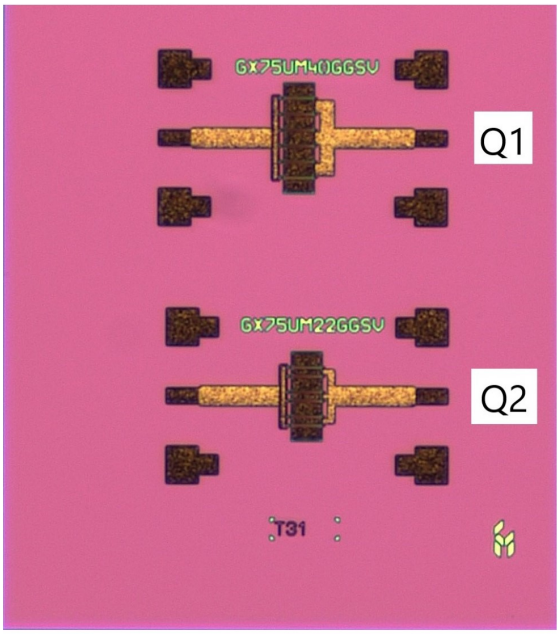

Figure 6: Die photograph of MMIC 4 with two devices, Q1 and Q2.

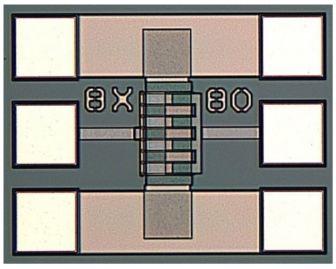

Figure 7: Die photograph of MMIC 5 with one device, Q1, which contains airbridges over the drain and source.

Prior to liquid crystal measurements, we first simulated each device with a commercially available tool to determine the relationship between DC power dissipation and maximum junction temperature. We examined the temperature rise at five different levels of drain current with a fixed drain voltage of 5 V, both with and without the presence of backside ground vias. A previous study by Wright [5] intimated that backside vias could lower the junction temperature if they were close enough to the FET gates. In Figures 8 and 9, we present the simulations of the maximum junction temperature as a function of drain current for two FETs, MMIC5/Q1 and MMIC1/Q1, respectively. Here, we have also generated a linear regression to fit each data set, which allows us to estimate the current necessary to reach any desired junction temperature.

In Figure 8, we further note the presence of backside vias did not have a significant impact on the junction temperature, whereas in Figure 9 the impact is clear. This result is easily explained by the location of these vias. In MMIC 5 (Figure 8), the two backside vias are each 68 um from the nearest FET gate, and their presence actually increased the junction temperature by 1.6% at a current of 150 mA. In MMIC 1 (Figure 9), the backside vias are 6.25 um from the gate, and their presence lowered the junction temperature by 4.1%. Although not shown, simulations of the other MMICs showed identical results in that vias spaced 6.25 um from the gates led to a decrease in temperature, whereas vias spaced 68 um away did not. This result confirms the hypothesis in [5].

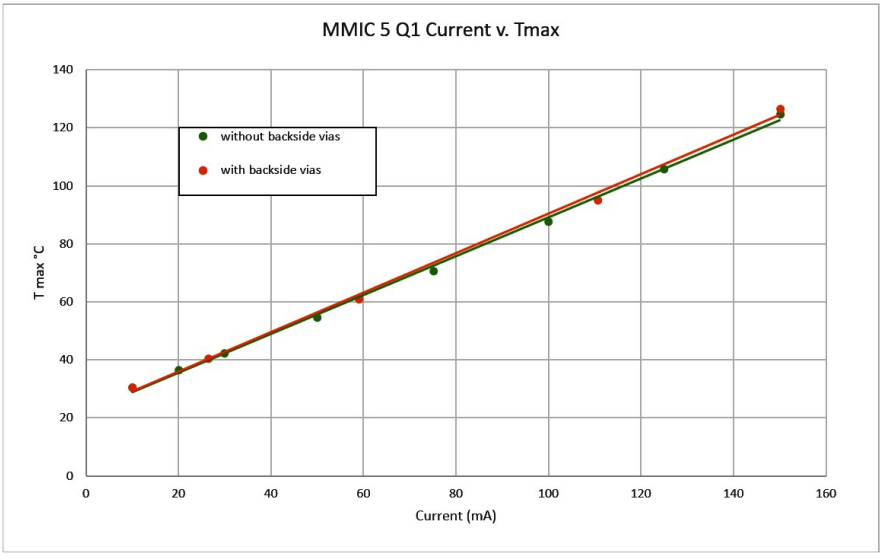

Figure 8: MMIC 5 Q1 plot of current versus maximum temperature. The backside vias are 68 um from the gates.

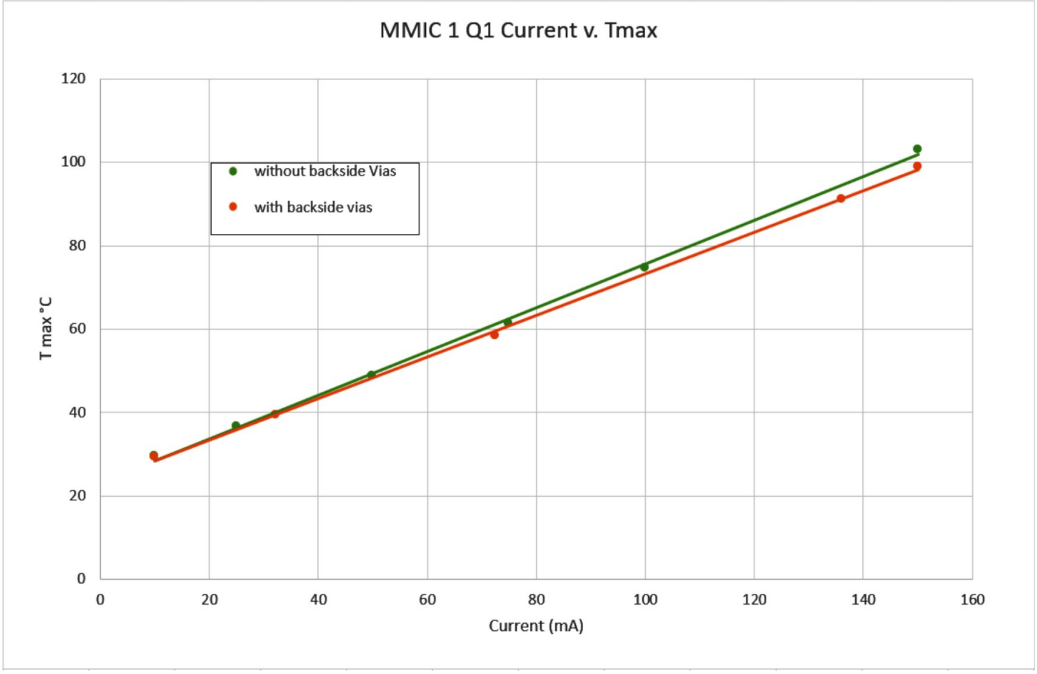

Figure 8: MMIC 5 Q1 plot of current versus maximum temperature. The backside vias are 68 um from the gates.

Liquid Crystal Measurements of Temperature

Liquid crystal solutions change the polarization of reflected light when the designated clearing temperature of the solution has been reached. Such change is manifest in the color of the solution as viewed through a polarizer. For this work, we used liquid crystals with clearing temperatures of 60 °C and 95 °C. We first painted a thin layer of liquid crystal solution onto the surface of each MMIC around the FET. After the solution was allowed to set for 30 seconds, the FET was biased on. In all measurements, the drain voltage was fixed at 5 V, and the gate voltage was increased from pinch-off in order to regulate the drain current through the FET. We focused the microscope directly over the gate fingers to look for the change in polarity, thus indicating we had reached the clearing temperature. We used the results of the initial simulations to set the drain current such that the FET would be close to the clearing temperature of the liquid crystal, and then fine-tuned the current in small increments until we could see the polarity flip close to the gate. We then noted the lowest drain current that caused a polarity flip within the FET device at the specific clearing temperature. This technique was repeated for up to three FETs of each type and the results were averaged together. In Table 2 below, we present the results of these measurements.

MMIC #	FET Size	Identifier	Crystal Type	Average Measured Current at Clearing Temperature:
MMIC1	8x80	Q1	60 °C	84.54 mA
	12x100	Q2	60 °C	126.02 mA
	6x120	Q3	60 °C	81.86 mA
	6x170	Q4	60 °C	96 mA
	8x80	Q1	95 °C	145.97 mA
	12x100	Q2	95 °C	224.35 mA
	6x120	Q3	95 °C	173.41 mA
	6x170	Q4	95 °C	174.25 mA
MMIC2	4x50	Q1	60 °C	37.9 mA
	4x100	Q2	60 °C	59.09 mA
	4x50	Q1	95 °C	65.25 mA
	4x100	Q2	95 °C	101.02 mA
MMIC3	8x50	Q1	60 °C	67.38 mA
	8x50	Q2	60 °C	71.95 mA
	8x50	Q3	60 °C	69.053 mA
	8x50	Q2	95 °C	116.835 mA
	8x50	Q3	95 °C	118.4 mA
MMIC4	6x75	Q1	60 °C	63.053 mA
	6x75	Q2	60 °C	61.52 mA
	6x75	Q1	95 °C	105.39 mA
	6x75	Q2	95 °C	111.023 mA
MMIC5	8x80	Q1	60 °C	63.05 mA
	8x80	Q1	95 °C	93.05 mA

Figure 8: MMIC 5 Q1 plot of current versus maximum temperature. The backside vias are 68 um from the gates.

Comparison of Measured vs. Simulated

In order to effectively analyze the data, we divided the measurements into two groups. Group A was for the 60 °C clearing temperature, whereas Group B was for the 95 °C clearing temperature. For each device, we entered the average measured current from Table 2 into the thermal simulation tool and then determined the maximum junction temperature. These simulation results were then compared to the crystal clearing temperature. One important measurement variable not easily controlled was the room temperature within our lab. Over the time scale of our measurements, the lab varied by approximately ±2 °C from the thermostat setting of 21 °C. In order to account for this, each simulation was performed with baseplate temperatures of 18.8 °C, 21 °C, and 23.3 °C. The results are reflected with error bars for each simulation as shown below in figures 10 and 11 for Groups A and B, respectively.

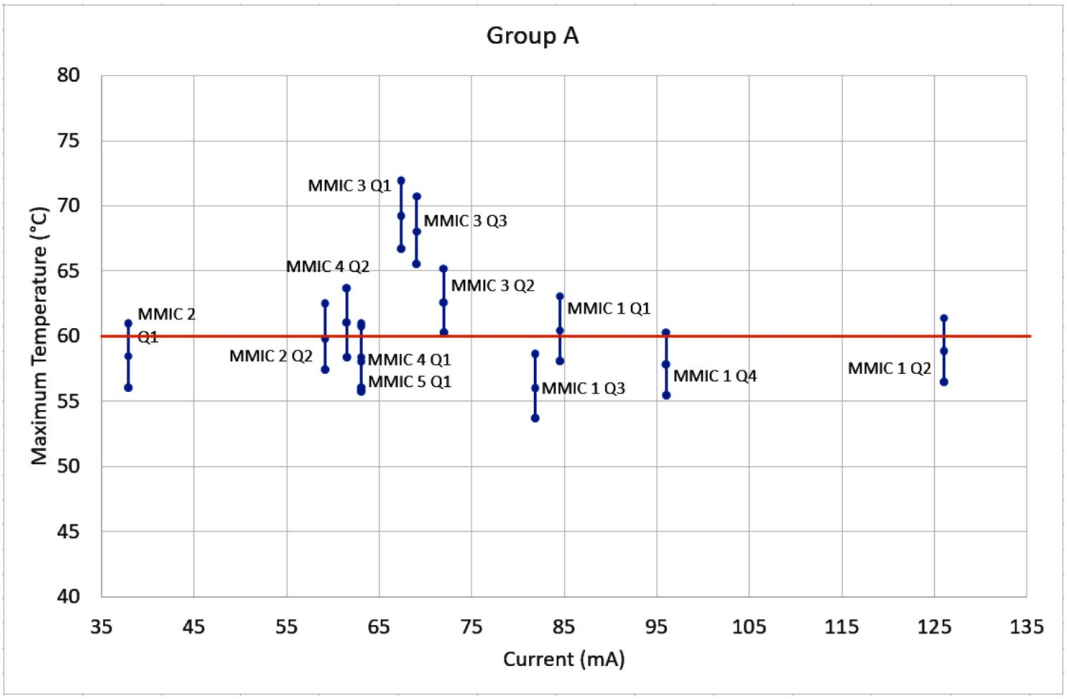

Figure 10: Measurement versus simulation for Group A FET devices (60 °C clearing temperature)

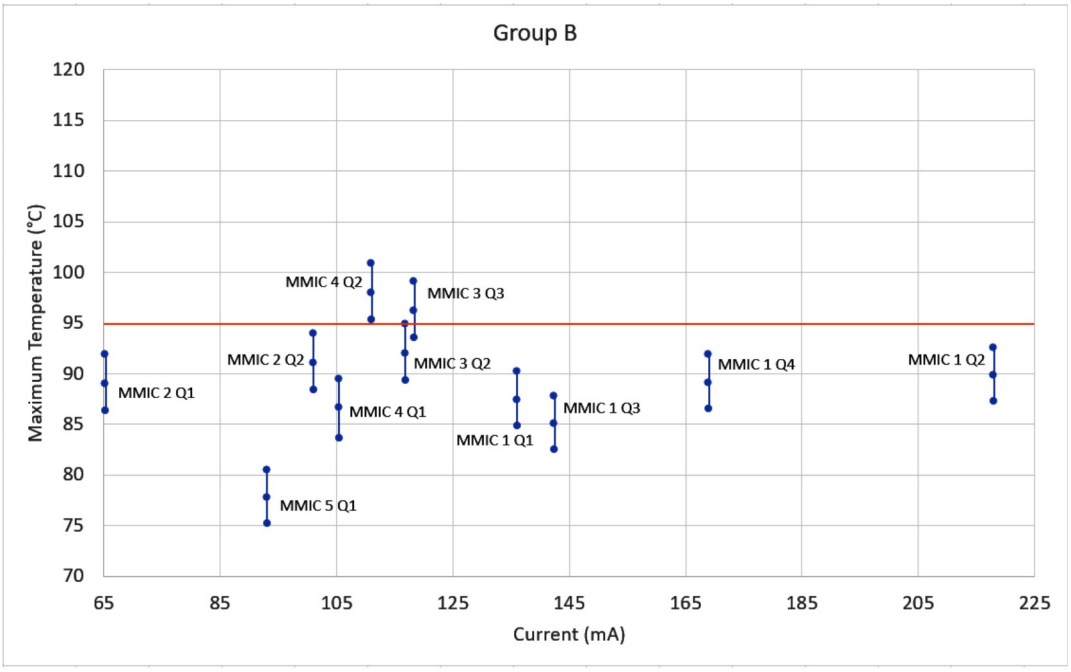

Figure 11: Measurement versus simulation for Group B FET devices (95 °C clearing temperature)

We note a number of observations from these graphs. First, the simulations match the measurements much better in Group A (60 °C) as opposed to Group B (95 °C). At the higher junction temperature, one would expect the surrounding environment to play a more significant role in regulating the temperature, and these effects were not included in the simulation.

Second, in Figure 10, it is clear that simulations of MMIC 3 devices Q1 and Q3 are less accurate than the other devices. These particular FETs utilize airbridges over the gates, and these structures prevent us from examining the entire gate. The noted polarity change within the liquid crystal was therefore somewhat outside the central gate area, which means the temperature at the middle of the FET was much higher than the clearing temperature.

Finally, we note liquid crystal measurements have an inherent subjectivity built into the results. Instead of displaying an obvious binary change from clear to black as portions of the FET cross the clearing temperature, the color fades in a more subtler manner. Therefore, determining that the clearing point has been reached can be a difficult decision process. We found that the most effective way to use liquid crystal was as follows: increase the current in large increments until most of the FET is black, as this will indicate the device is well above the clearing temperature. Then, decrease the current in small increments while focusing on one small area near the center FET gate. When a binary change is seen in this small space, the current is then recorded. The current can be increased and decreased in small amounts around this value to assure that this measurement is replicable. Such a process helps set a standard for when the clearing temperature has been reached. However, different FETs react differently to the liquid crystal so it is difficult to utilize the same standard across multiple die. This is demonstrated in the graph of group B. The simulated temperature values for MMIC 1 Q1-Q4 are similar to each other, but noticeably different than the clearing temperature of 95 °C. While the same location was examined on each of these FETs during the measurement, this particular location must not have been optimal.

Conclusions

In this paper, we have considered the junction temperatures of a number of different GaAs FET devices. Liquid crystal measurement techniques were used to determine the required drain current such that the FET junction reached a preset clearing temperature, and these results were then used to drive simulations of the devices. In general, the thermal simulation tool predicted the maximum junction temperature to within 0.8 °C at 60 °C and within 5 °C at 95 °C. These temperatures represent a 40 °C and 75 °C rise above the backplate temperature, respectively. We also demonstrated that substrate vias very close to the FET gates (~6.5 um) can lower the junction temperature by up to 4% as compared to those FETs without such vias. Such experimental validation gives us heightened confidence we can use simulation tools to predict the maximum junction temperature and therefore gain a clear understanding of the reliability of GaAs MMICs.

About the Author

Emma Fournier is an undergraduate Chemical Engineering student at Tulane University in New Orleans, Louisiana. She will be completing a B.S.Chem.E. in 2022. She is currently completing a summer internship at Custom MMIC, working on projects related to thermal analysis.

References

1. J.A. Mittereder, J.R. Roussos, M.T. Karanikolas, and W.T. Anderson, "Comparison of Statistical Distributions for the Analysis of GaAs MMIC Life Test Data," *1997 GaAs Reliability Workshop Proceedings*, October 1997, pp. 54-61.
2. C. Costrini, A. Cetronio, P. Romanini, G. Breglio, A. Irace, M. Riccio, "50 W X-band GaN MMIC HPA: Effective Power Capability and Transient Thermal Analysis," *The 40th European Microwave Conference*, September 2010, pp.1650-1653.
3. K.J. Negus, R.W. Franklin, and M.M. Yovanovich, "Thermal Modeling and Experimental Techniques for Microwave Bipolar Devices" *Fifth Annual IEEE Semiconductor Thermal and Temperature Measurement Symposium*, February 1989, pp.63-72.
4. Roberto Coccioli, Kevin Nary, and Phil Canfield, "Multi-scale Thermal Analysis of GaAs RF Device," *Semiconductor Thermal Measurement and Management IEEE 21st Annual IEEE Symposium*, March 2005.
5. John L. Wright, B.W. Marks, and K.D. Decker, "Modeling of MMIC Devices for Determining MMIC Channel Temperatures During Life Tests," *Seventh IEEE Semiconductor Thermal Measurement and Management Symposium*, February 1991, pp. 131-139.