

### Product Overview

Qorvo's QPA1314D is a high power MMIC amplifier fabricated on Qorvo's production 0.15 um GaN on SiC process (QGaN15). QPA1314D is targeted to the 13.75-14.5 GHz Satcom band. Linear power is 20 W with 25 dBc third order intermodulation distortion products. It provides 55 W of saturated output power with 22.5 dB of large signal gain while achieving 37% power-added efficiency. Operating frequency can extend to 12.75 – 15.35 GHz if desired.

To simplify system integration, the QPA1314D is fully matched to 50 ohms with DC grounded I/O ports for optimum ESD performance. Also, there are on-chip blocking capacitors following the DC grounds on the input and output ports.

The QPA1314D is ideal for supporting communications and radar applications in both commercial and military markets.

The QPA1314D is 100% DC and RF tested on-wafer to ensure compliance to electrical specifications.

Lead-free and RoHS compliant

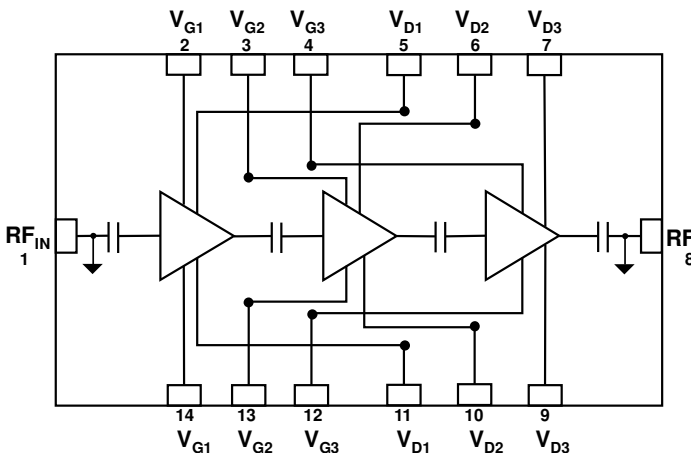


### Key Features

- Frequency Range: 13.75 – 14.5 GHz
- Extended Frequency Range: 12.75 – 15.35 GHz
- $P_{SAT}$  ( $P_{IN} = 25$  dBm): 47.5 dBm
- PAE ( $P_{IN} = 25$  dBm): 37 %
- IM3 ( $P_{OUT}/Tone = 40$  dBm): -25 dBc
- Small Signal Gain: 29 dB
- Bias:  $V_D = +24$  V,  $I_{D12} = 168$  mA,  $I_{D3} = 512$  mA  
 $V_G = -2.3$  V typ range.
- Die Dimensions: 4.78 x 6.71 x 0.10 mm

*Performance is typical across frequency. Please reference electrical specification table and data plots for more details.*

### Functional Block Diagram



### Applications

- Satellite Communications
- Datalinks

### Ordering Information

Part No.	Description
QPA1314D	55 Watt GaN PA
QPA1314DEVB	Evaluation Board for QPA1314D



### Absolute Maximum Ratings

Parameter	Value / Ra
Drain Voltage (V <sub>D</sub> )	29.5 V
Gate Voltage Range (V <sub>G</sub> )	-6 V to 0 V
Drain Current (I <sub>D1</sub> )	0.96 A
Drain Current (I <sub>D2</sub> )	1.96 A
Drain Current (I <sub>D3</sub> )	7.56 A
Drain Current (I <sub>D_TOTAL</sub> )	10.48 A
Gate Current (I <sub>G</sub> )	See p. 25
Power Dissipation (P <sub>DISS</sub> ), 85 °C	130 W
Input Power (P <sub>IN</sub> ), 50 Ω, CW, V <sub>D</sub> = 24 V, I <sub>D12</sub> = 228 mA, I <sub>D3</sub> = 512 mA, T <sub>BASE</sub> = 85 °C	31 dBm
Input Power (P <sub>IN</sub> ), 3:1 VSWR, CW, V <sub>D</sub> = 24 V, I <sub>D12</sub> = 228 mA, I <sub>D3</sub> = 512 mA, T <sub>BASE</sub> = 85 °C	31 dBm
Mounting Temperature (30 seconds)	320 °C
Storage Temperature	-55 to +150

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

### Electrical Specifications

Parameter	Conditions <sup>(1)</sup> <sup>(2)</sup>	Min	Typ.	Max	Units
Operational Frequency Range		13.75		14.5	GHz
Output Power at Saturation, P <sub>SAT</sub>	P <sub>IN</sub> = 25 dBm, Frequency = 12.75 – 13.75 GHz <sup>(3)</sup>	47	48		dBm
	P <sub>IN</sub> = 25 dBm, Frequency = 13.75 – 14.5 GHz	46.7	47.5		
	P <sub>IN</sub> = 25 dBm, Frequency = 14.5 – 15.35 GHz <sup>(3)</sup>	45	47		
Power Added Efficiency, PAE	P <sub>IN</sub> = 25 dBm		37		%
Large Signal Gain	P <sub>IN</sub> = 25 dBm		22.5		dB
3 <sup>RD</sup> Intermodulation Products, IM3	P <sub>OUT</sub> /Tone = 40 dBm		-25		dBc
5 <sup>RD</sup> Intermodulation Products, IM5			-40		
Small Signal Gain, S21	P <sub>IN</sub> = -30 dBm		29		dB
Input Return Loss, IRL			20		
Output Return Loss, ORL			7		
P <sub>SAT</sub> Temperature Coefficient	T <sub>DIFF</sub> = 25 °C to 85 °C; P <sub>IN</sub> = 25 dBm		-0.04		dBm/°C
S21 Temperature Coefficient	T <sub>DIFF</sub> = 25 °C to 85 °C		-0.10		dB/°C

Notes:

1. Test conditions unless otherwise noted: CW, V<sub>D</sub> = 24 V, I<sub>D12</sub> = 168 mA, I<sub>D3</sub> = 512 mA, V<sub>G</sub> = -2.3 V +/- 0.6V typical, T<sub>BASE</sub> = +25°C, Z<sub>0</sub> = 50 Ω
2. T<sub>BASE</sub> is back side of 20 mil CuMo carrier plate with AuSn die attached
3. Extended frequency range

### Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V <sub>D</sub> )		24	24	V
Drain Current, Quiescent (I <sub>D12</sub> )		168		mA
Drain Current, Quiescent (I <sub>D3</sub> )		512		mA
Drain Current, RF (I <sub>D_Drive</sub> Total)		See plot page 4,6,9,12		mA
Gate Voltage Typ. Range (V <sub>G</sub> )		-1.7 to -2.9		V
Gate Current, RF (I <sub>G_Drive</sub> )		See plot page 5,6		mA
Input Power @ Saturation, (P <sub>IN</sub> )*		T <sub>BASE</sub> -40°C: 25		dBm
		T <sub>BASE</sub> +25°C: 25		
		T <sub>BASE</sub> +85 °C: 29		
Operating Temp. Range (T <sub>BASE</sub> *)	-40		+85	°C

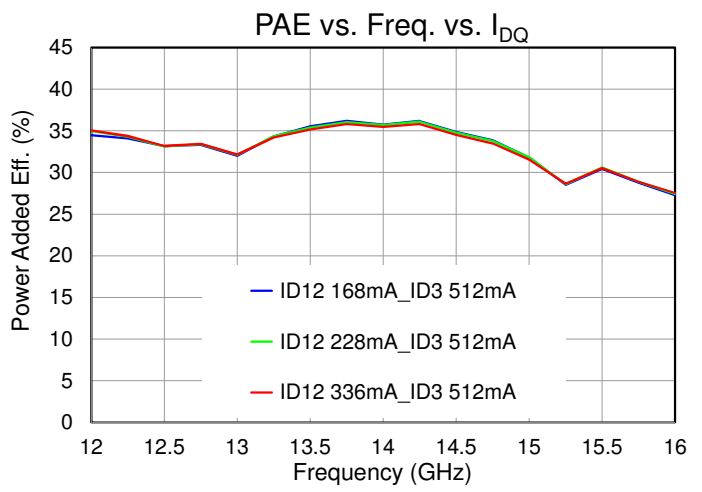
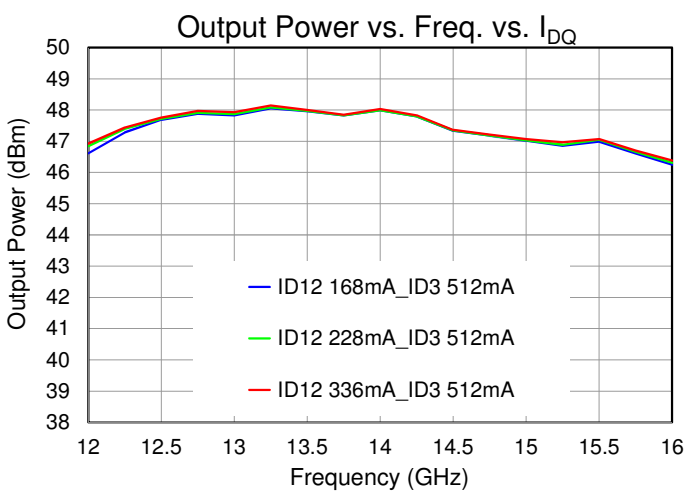
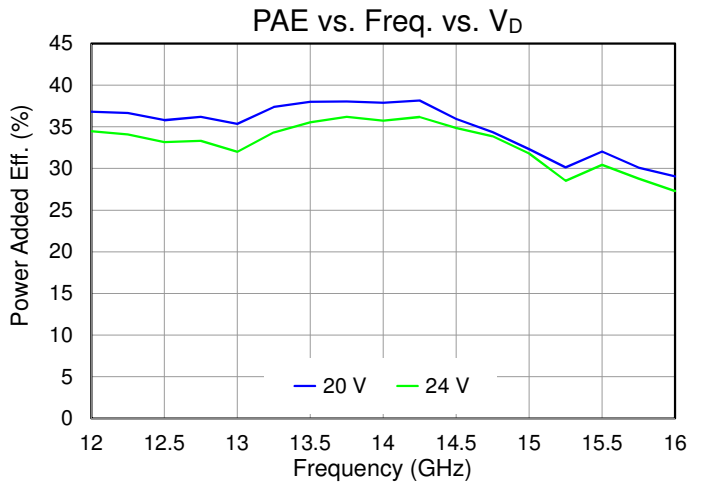
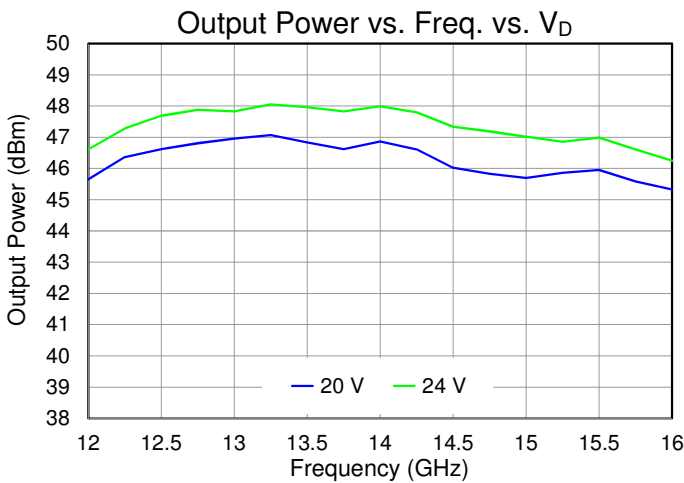
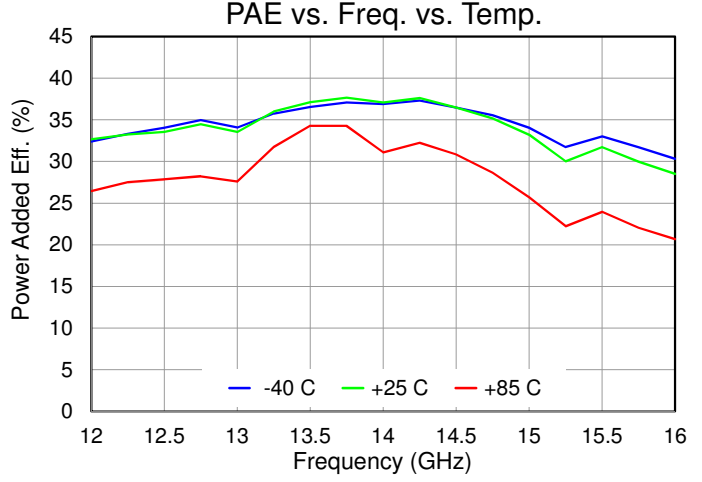
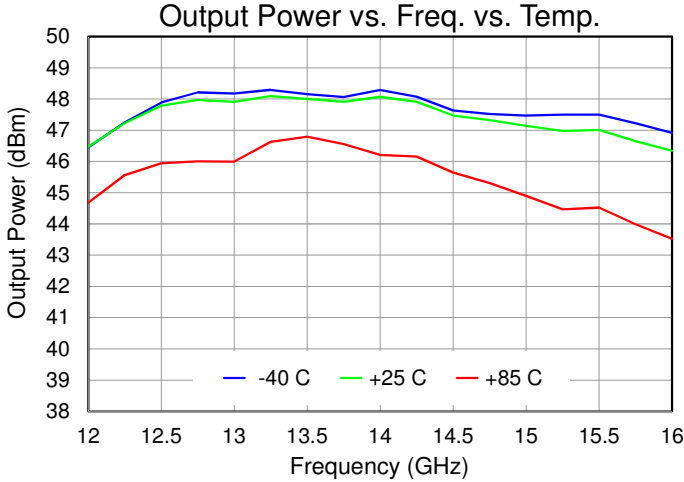
\* See plots page 7

T<sub>BASE</sub> is back side of 20 mil CuMo carrier plate with AuSn solder

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

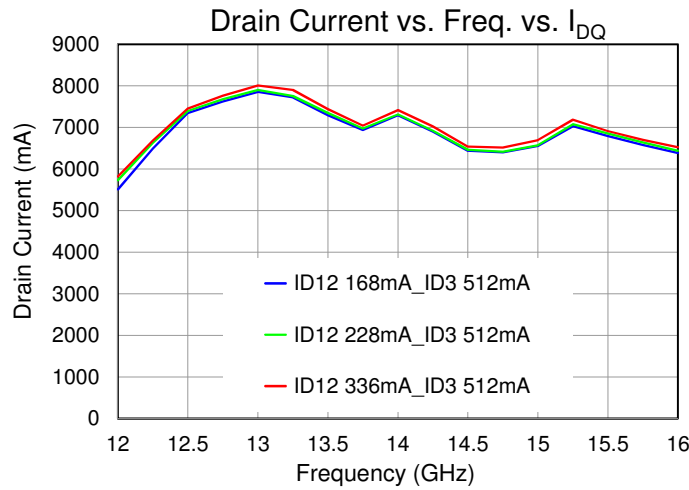
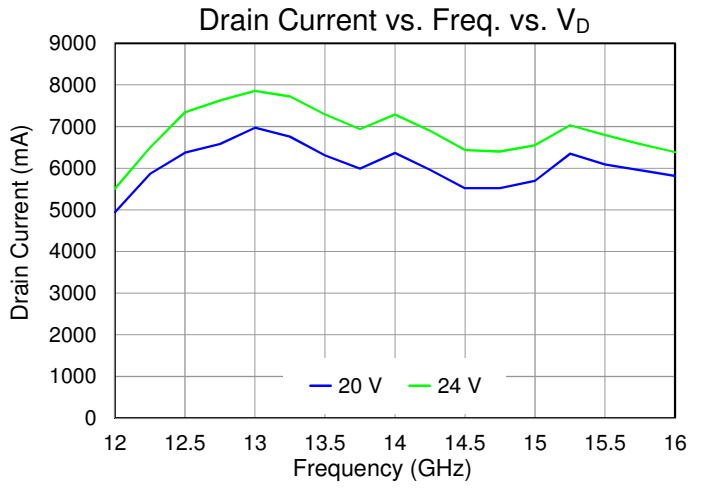
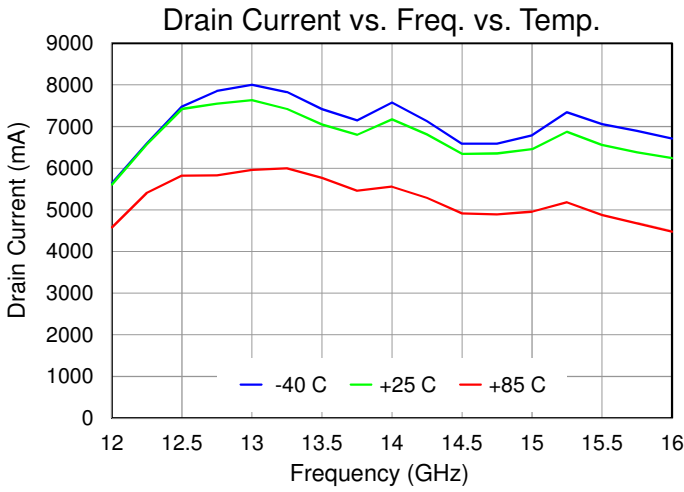
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $I_{D12} = 168\text{ mA}$ ,  $I_{D3} = 512\text{ mA}$ ,  $P_{IN} = 25\text{ dBm}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



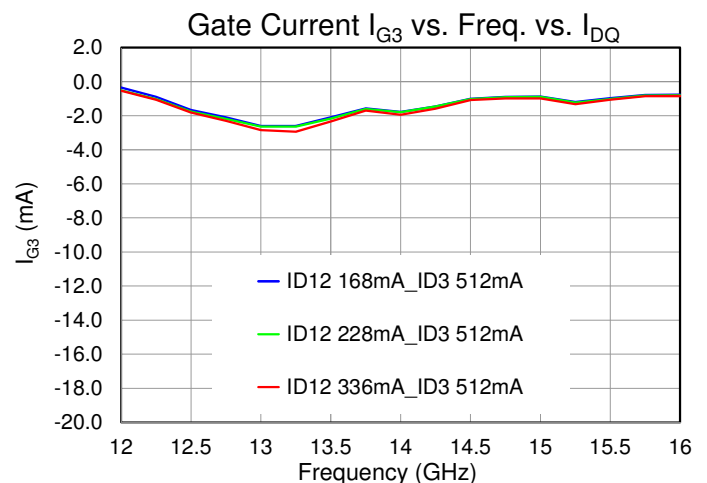
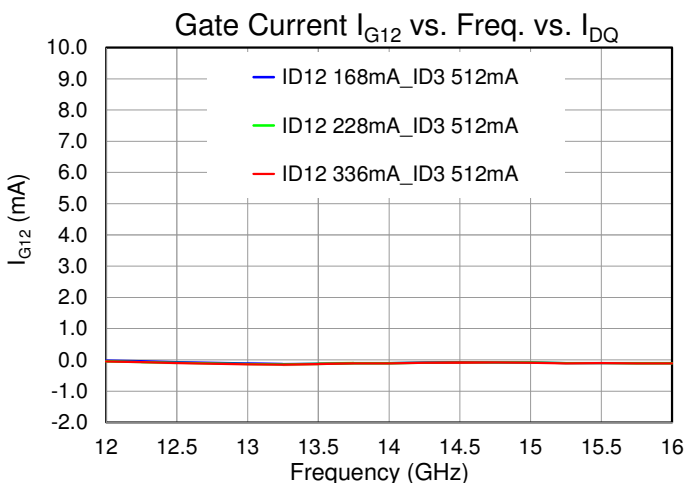
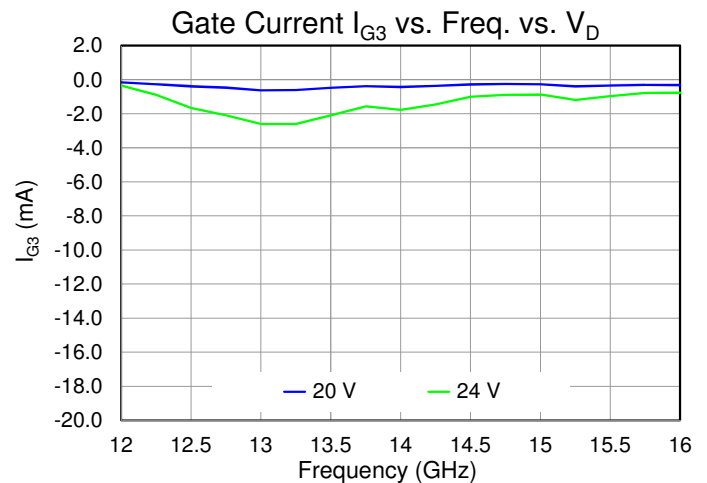
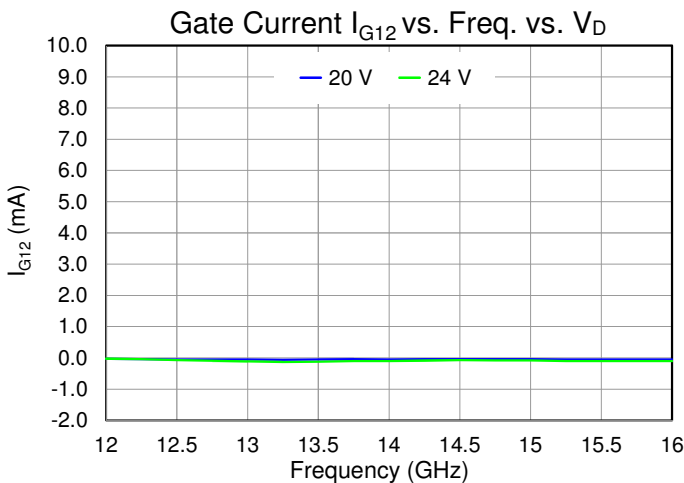
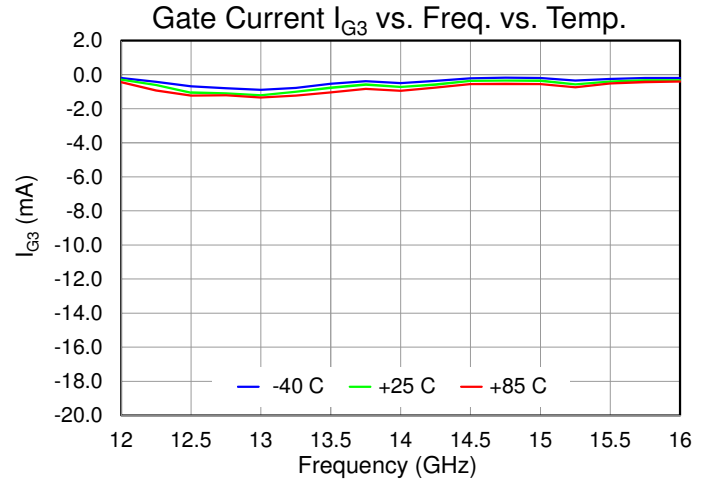
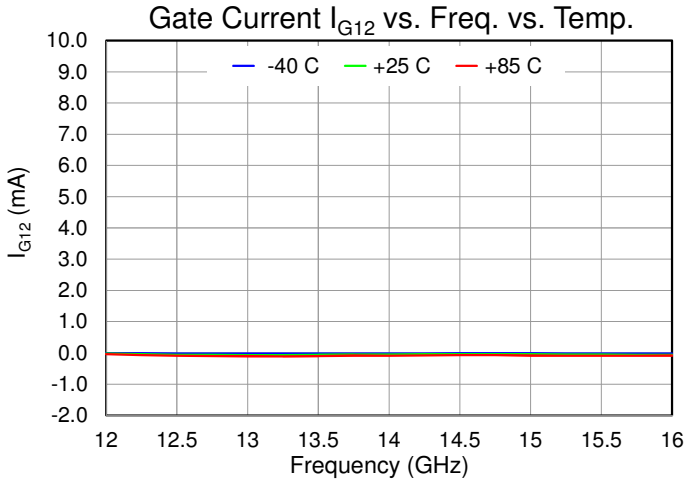
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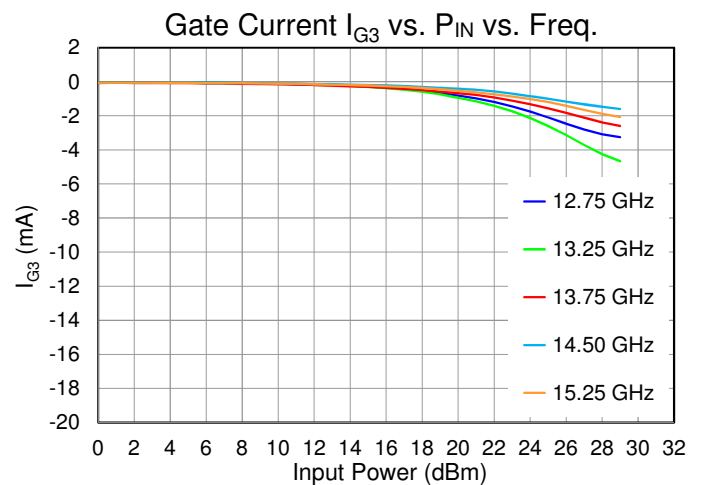
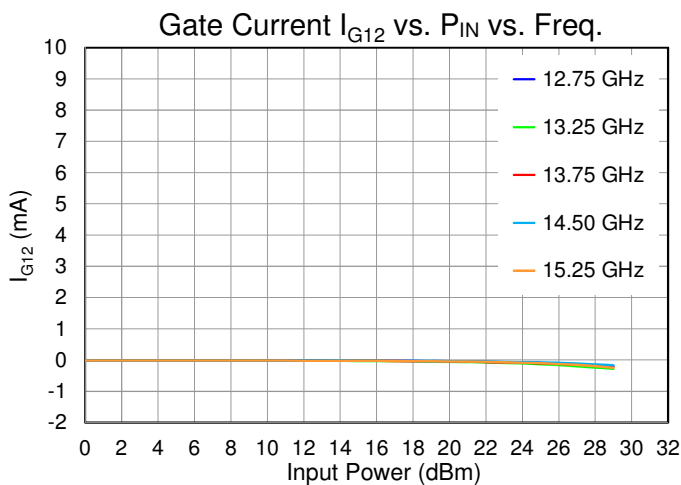
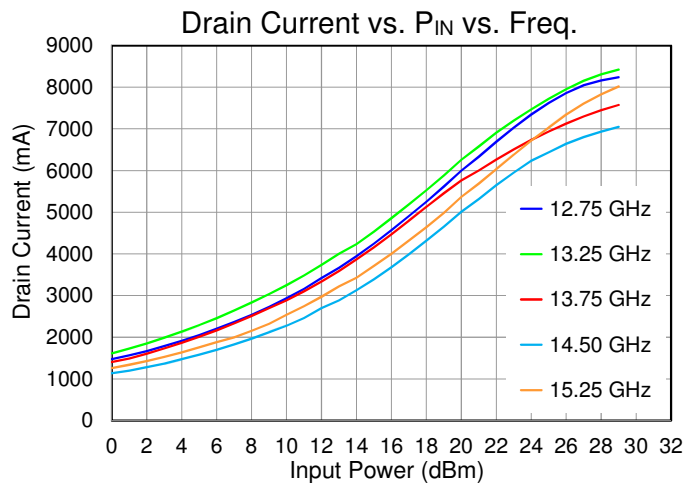
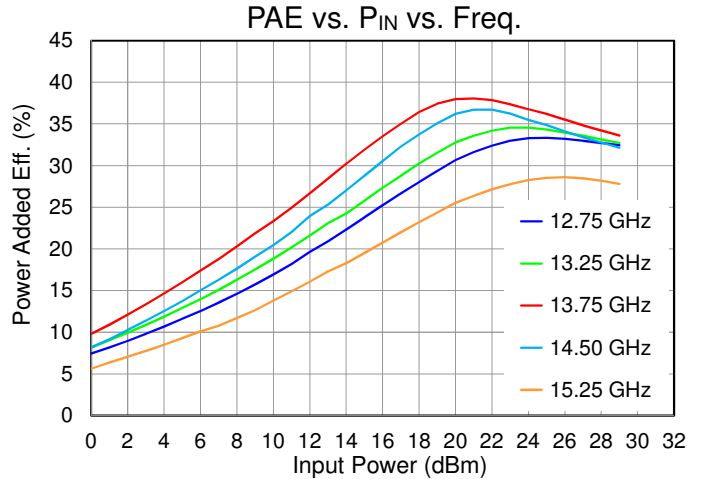
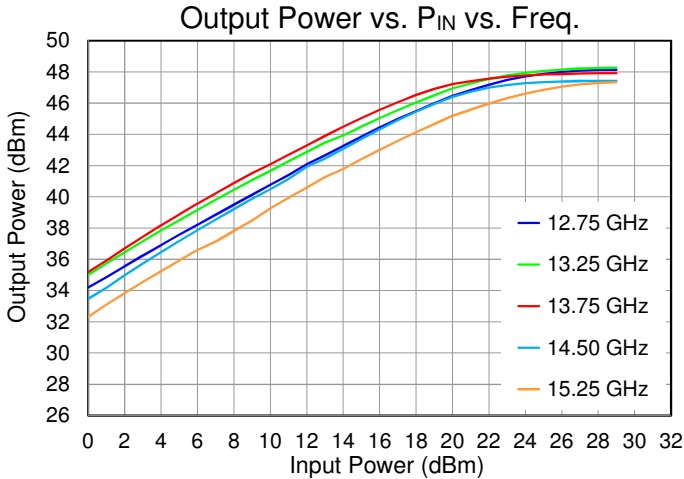
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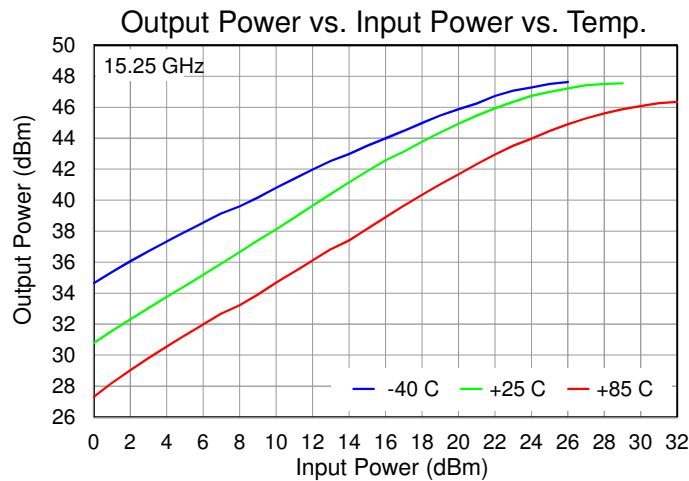
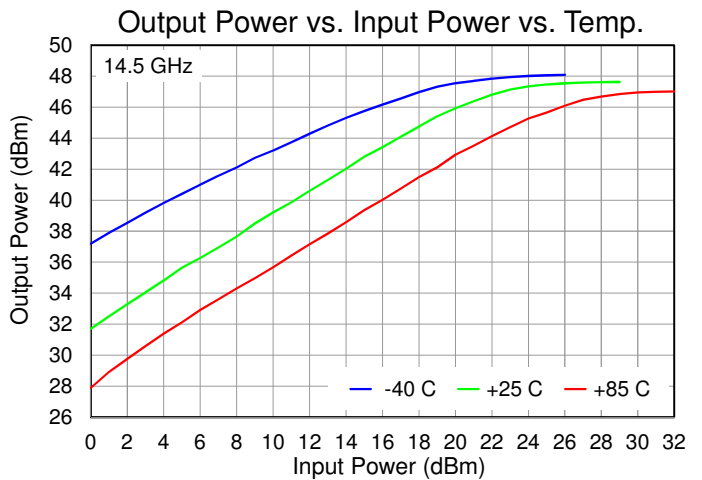
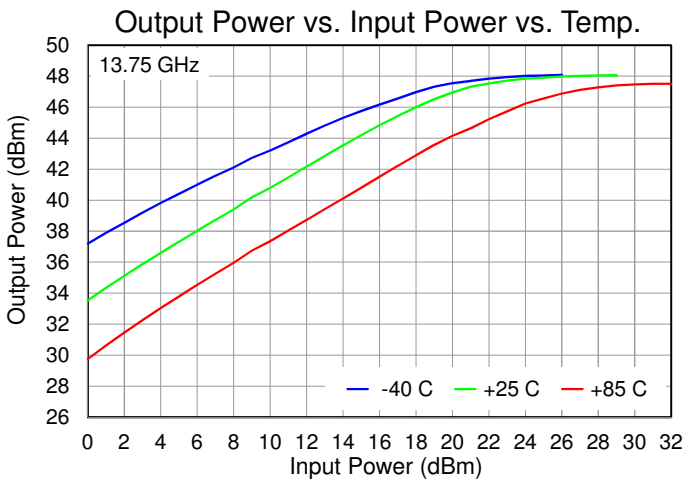
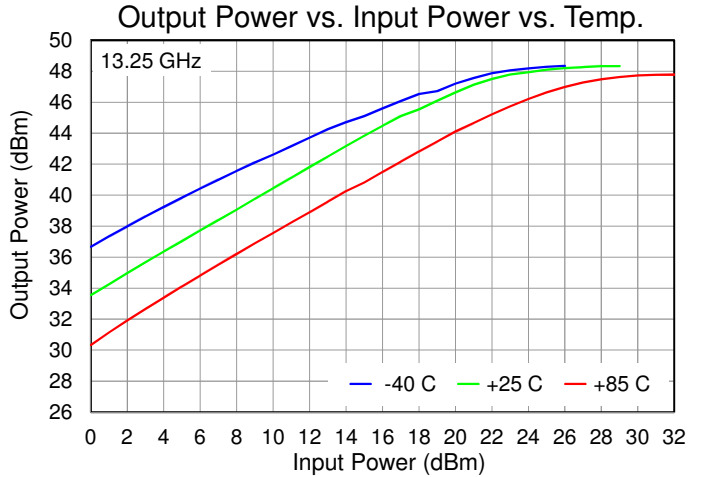
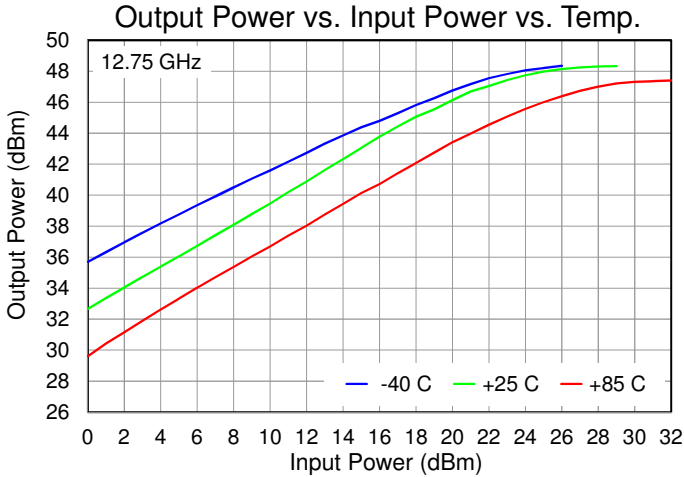
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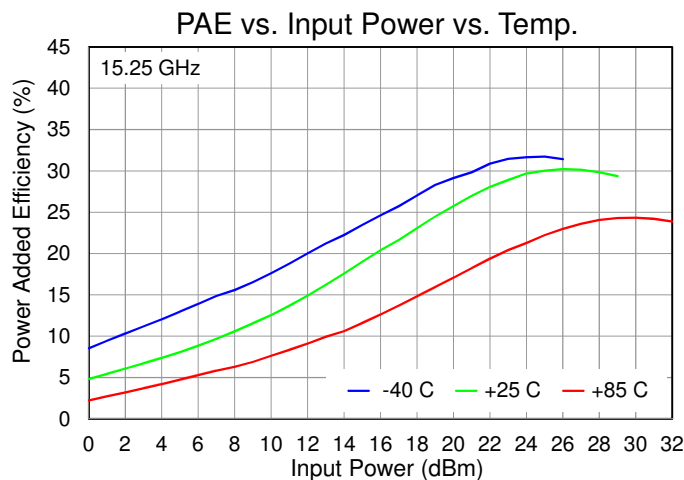
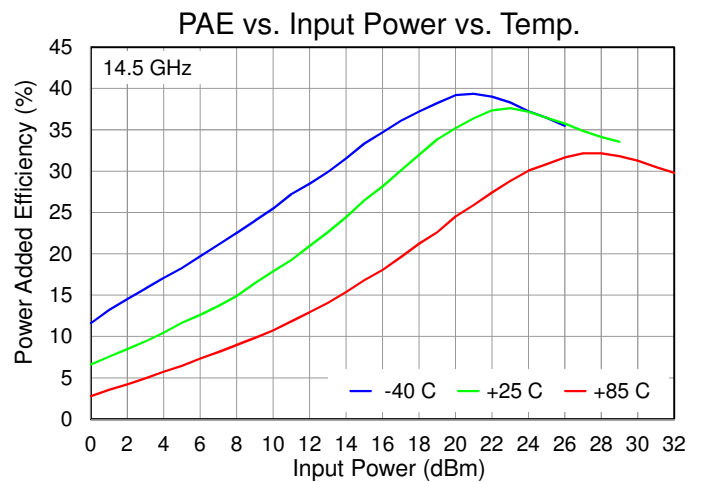
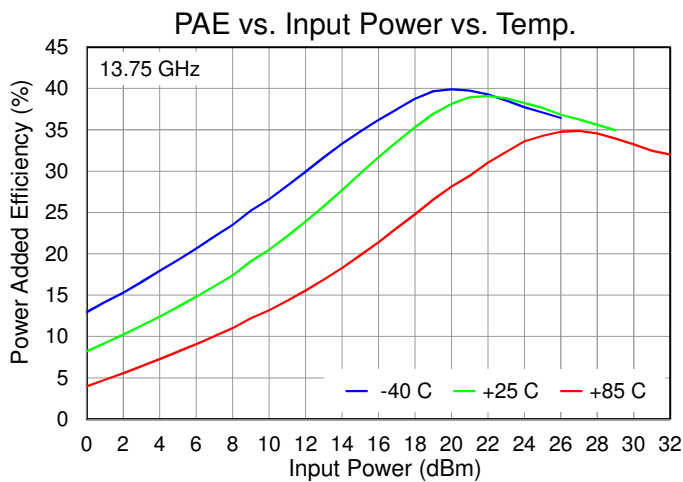
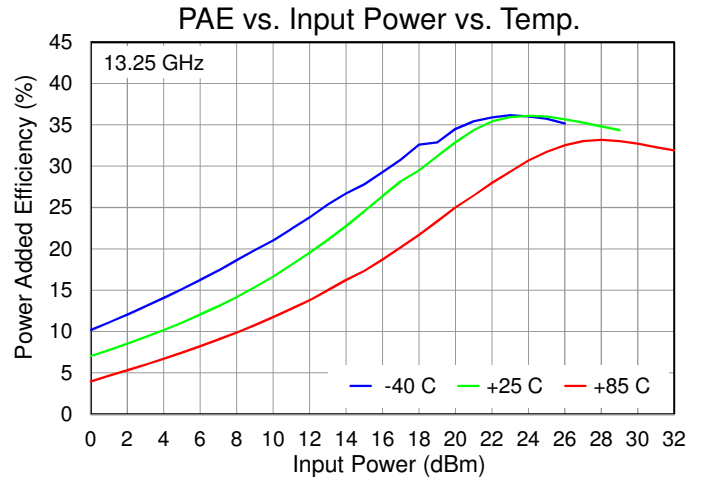
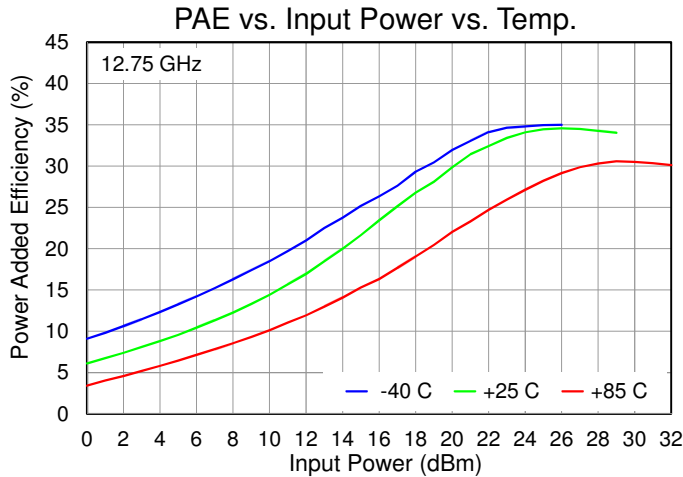
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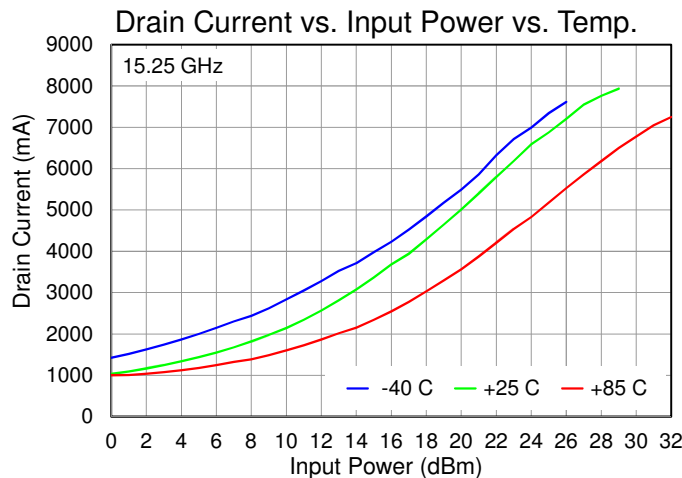
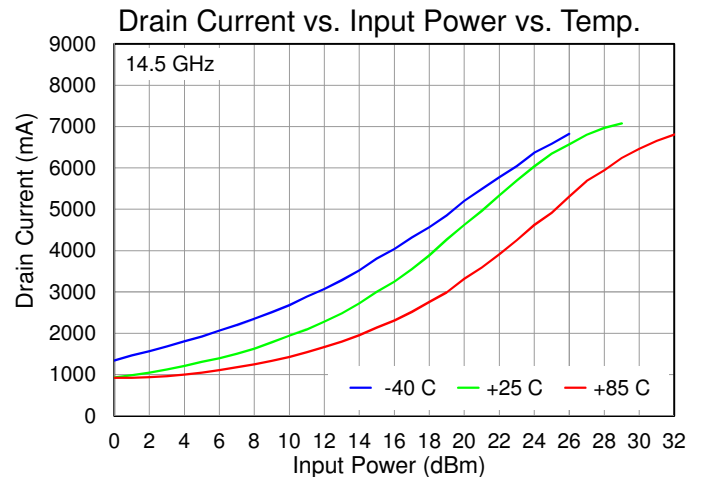
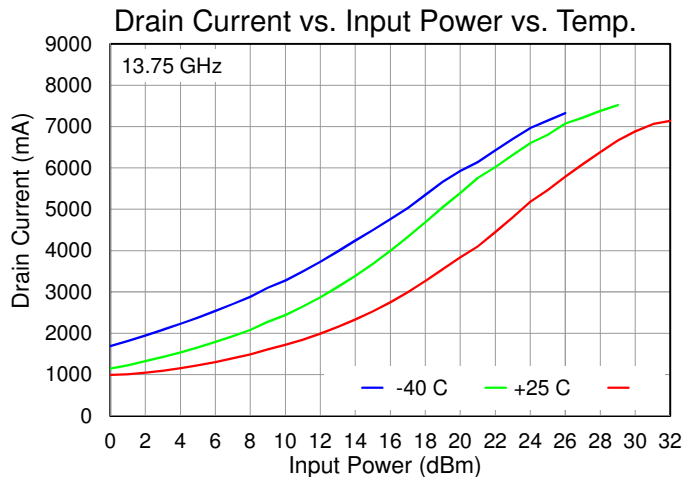
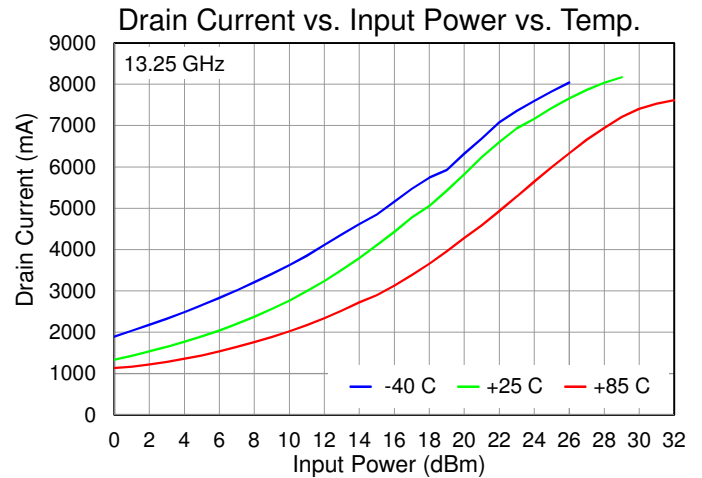
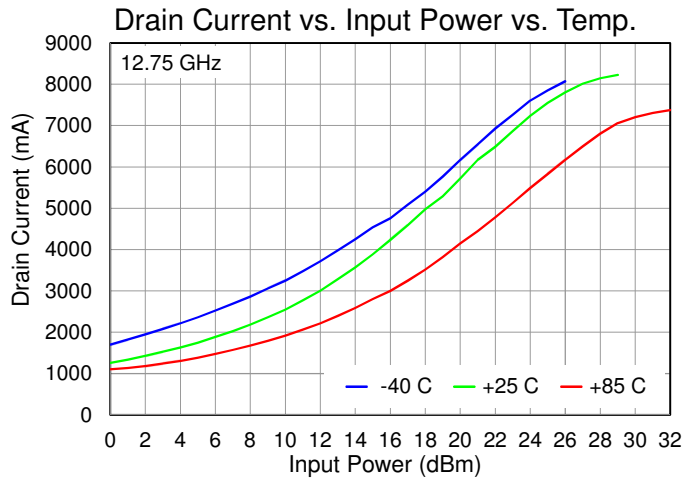
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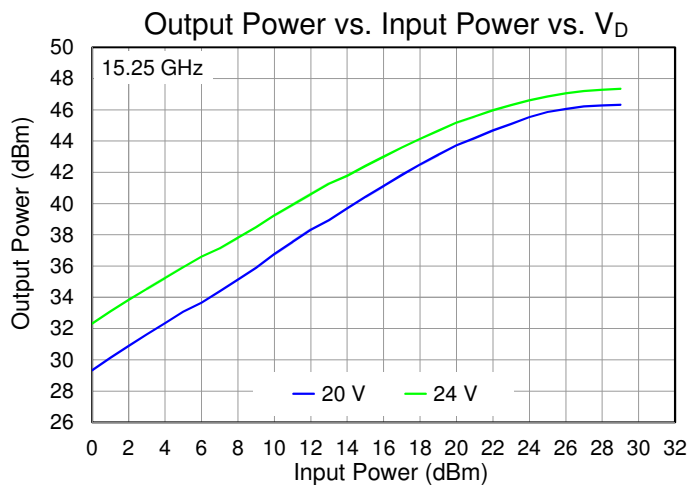
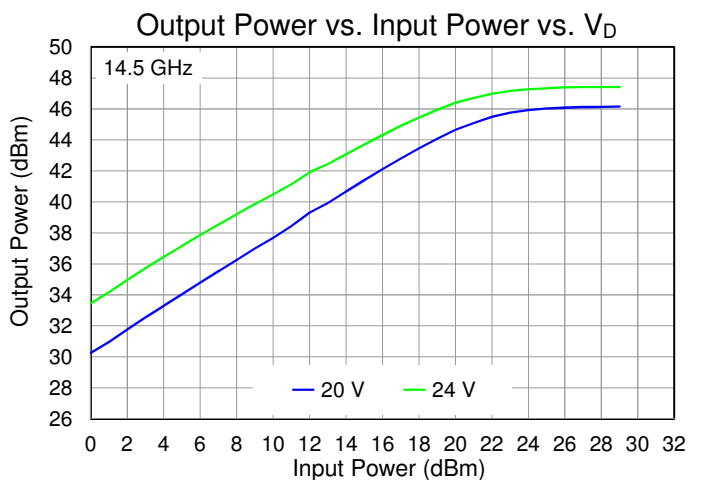
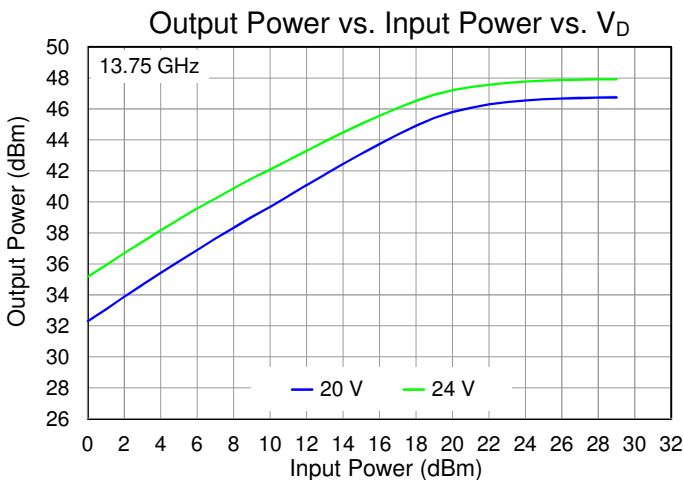
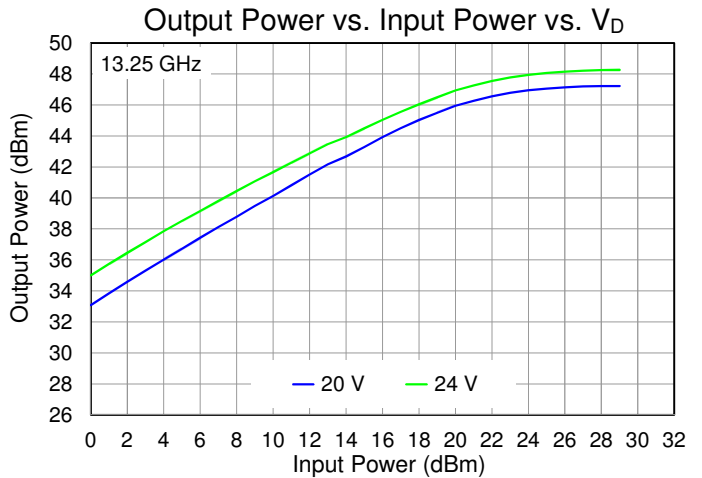
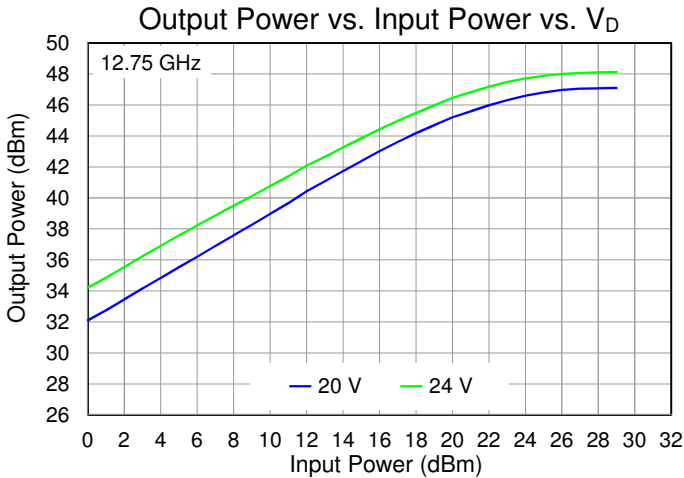
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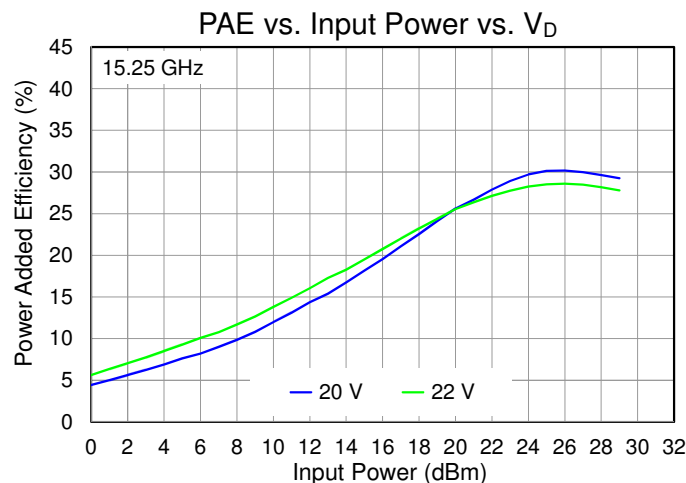
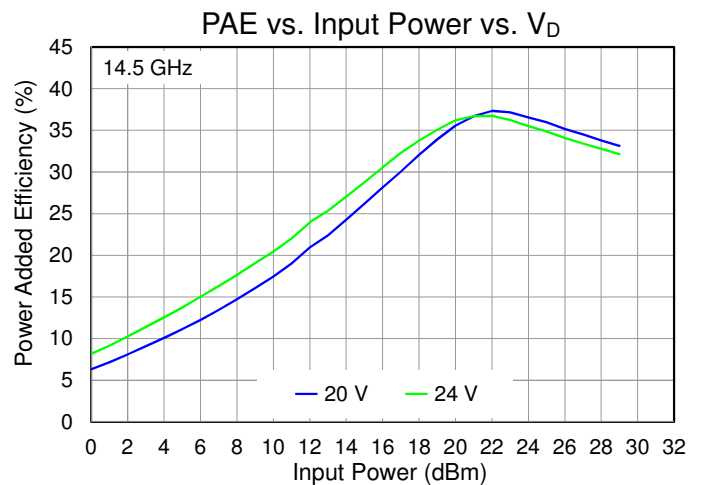
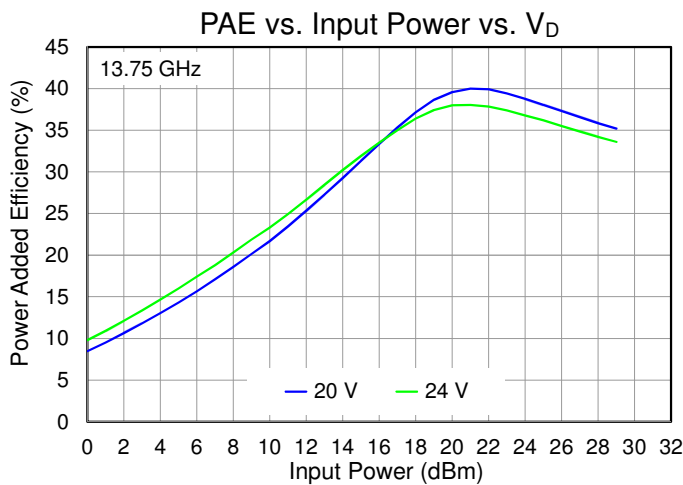
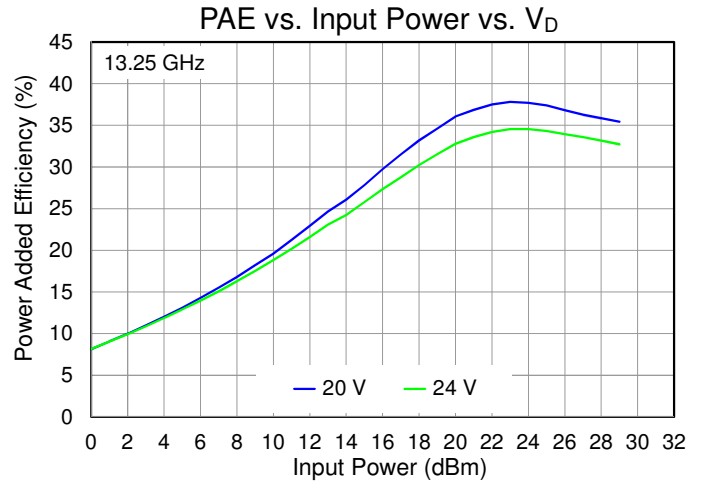
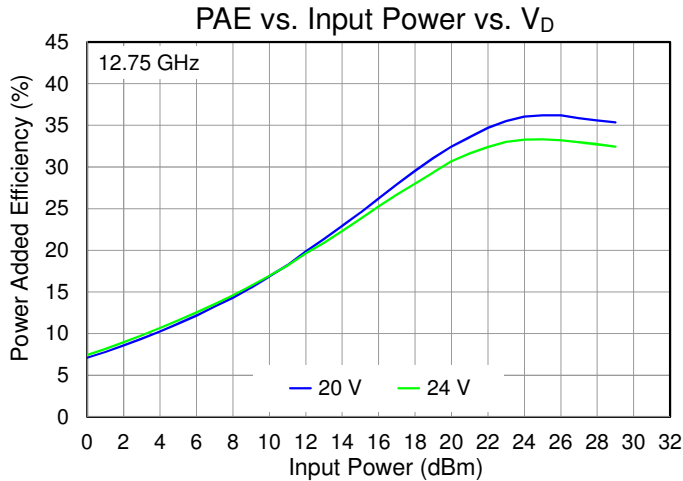
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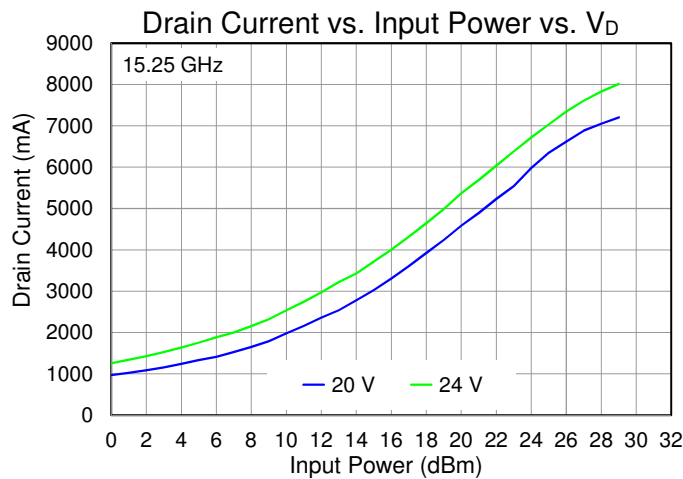
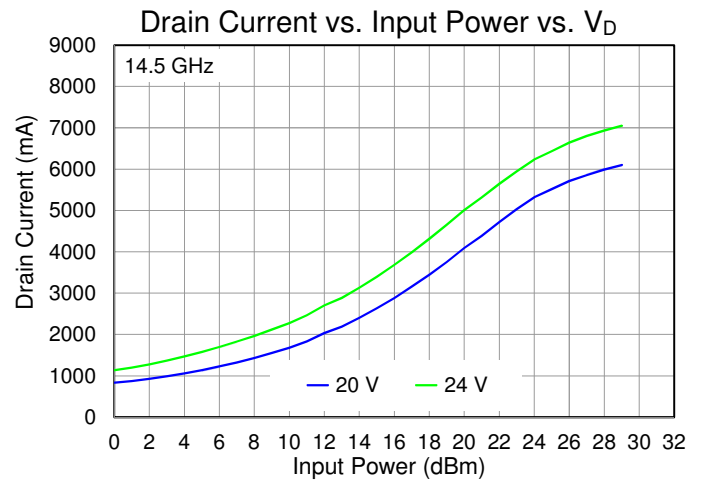
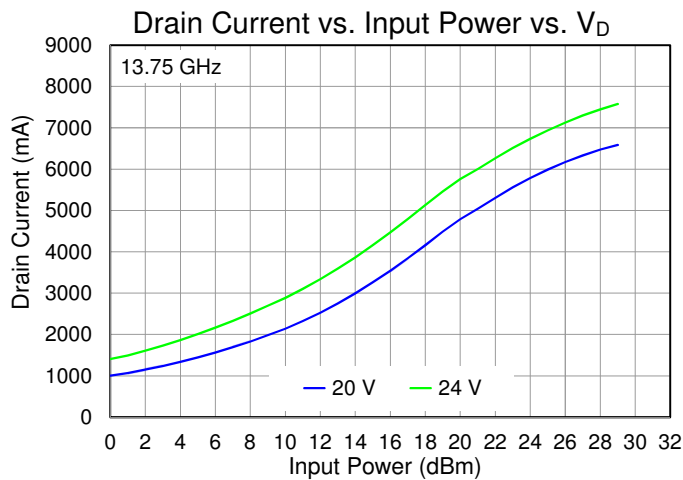
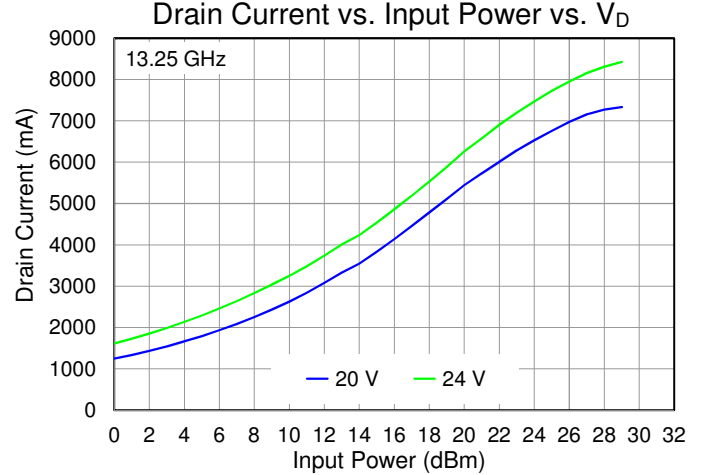
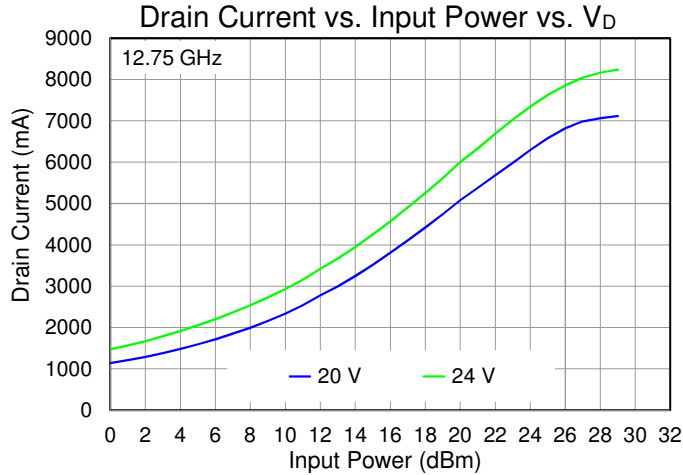
Performance Plots – Large Signal

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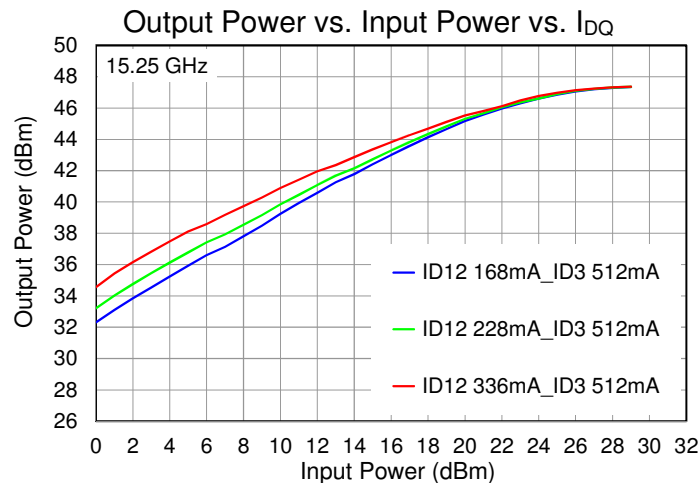
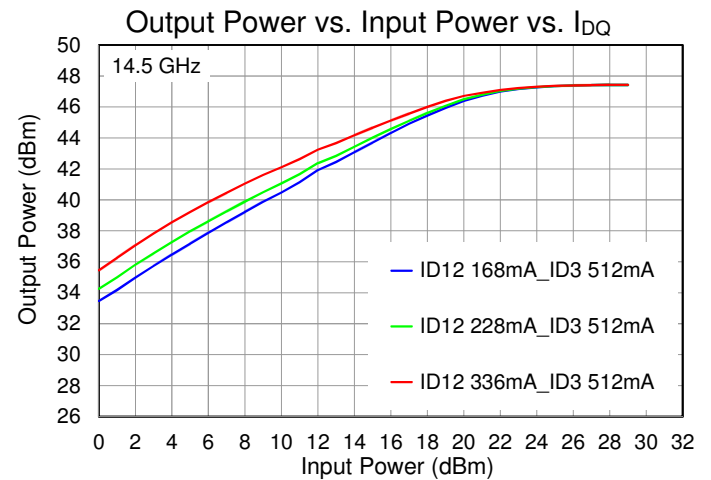
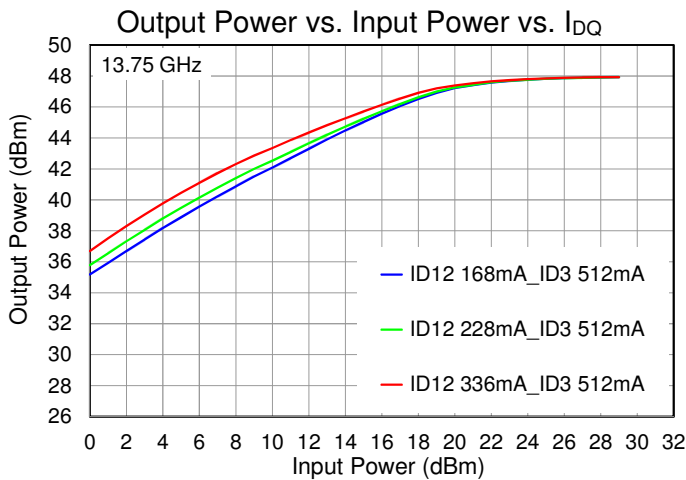
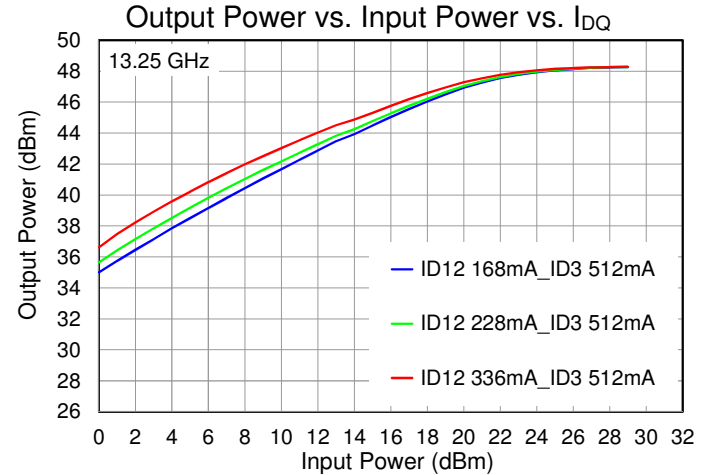
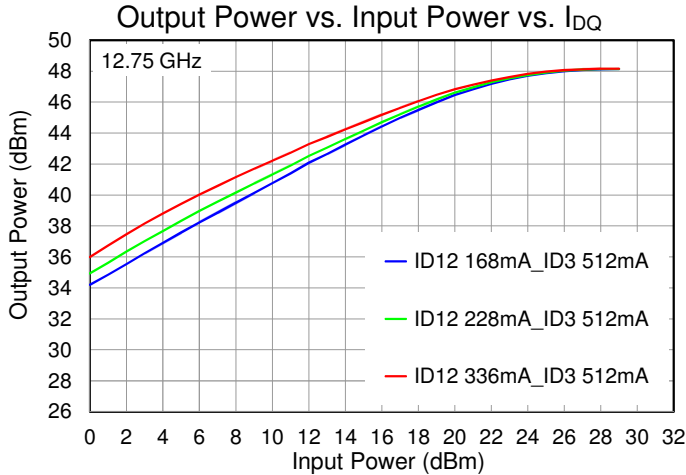
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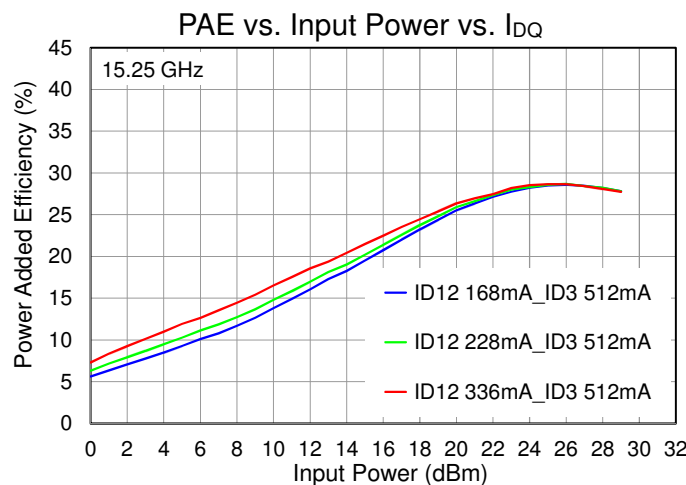
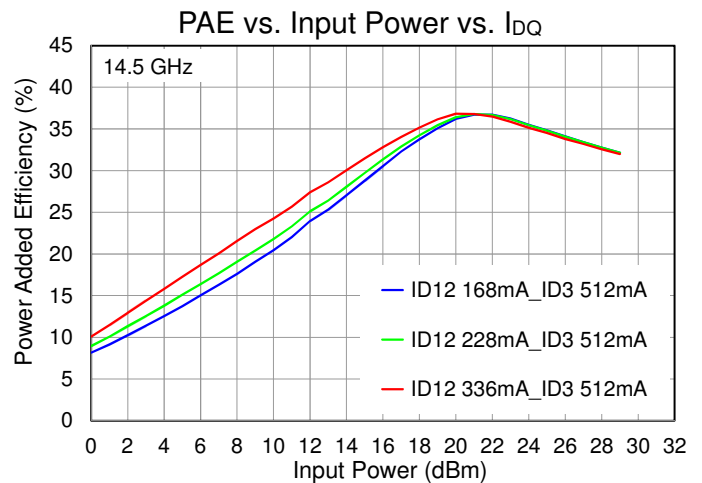
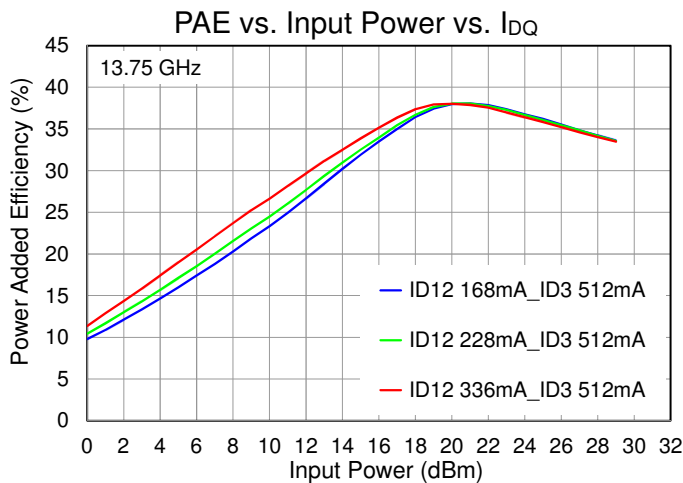
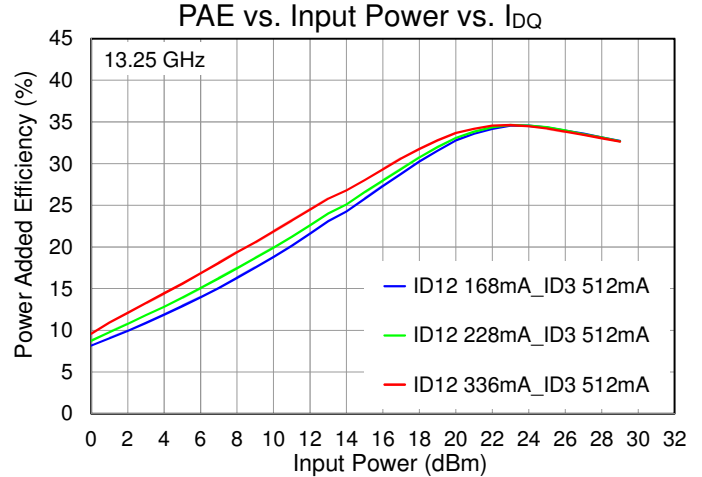
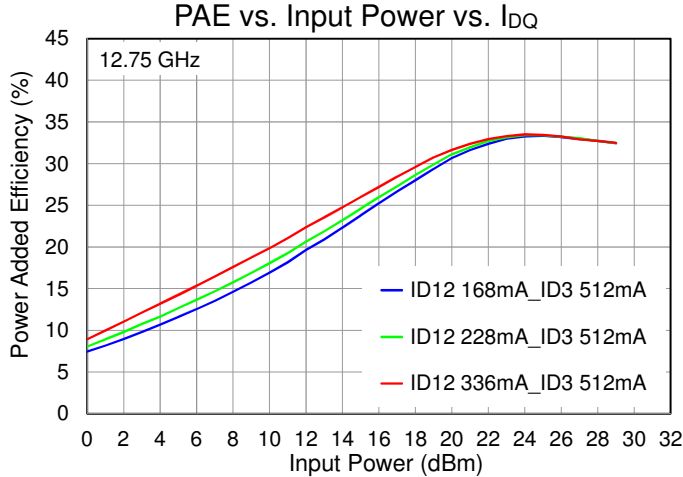
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $I_{D12} = 168\text{ mA}$ ,  $I_{D3} = 512\text{ mA}$ ,  $P_{IN} = 25\text{ dBm}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



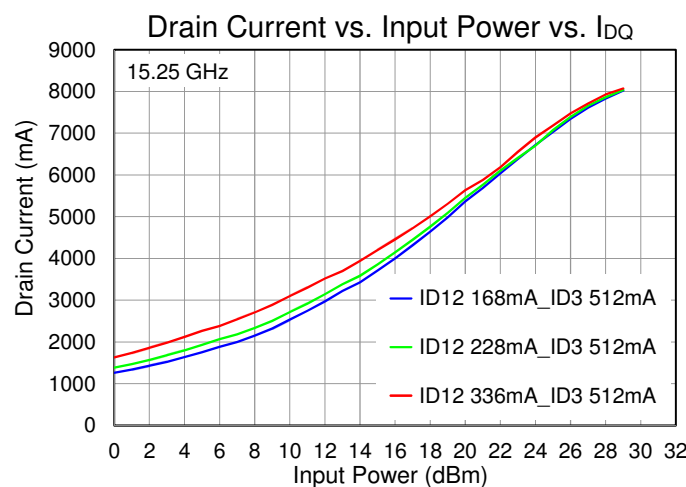
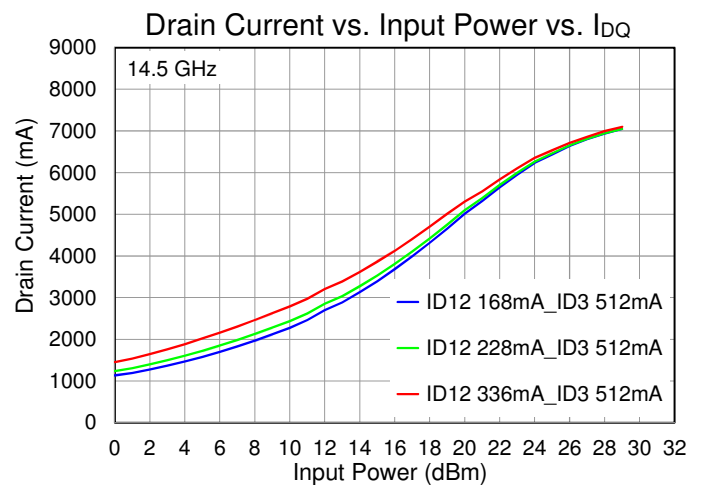
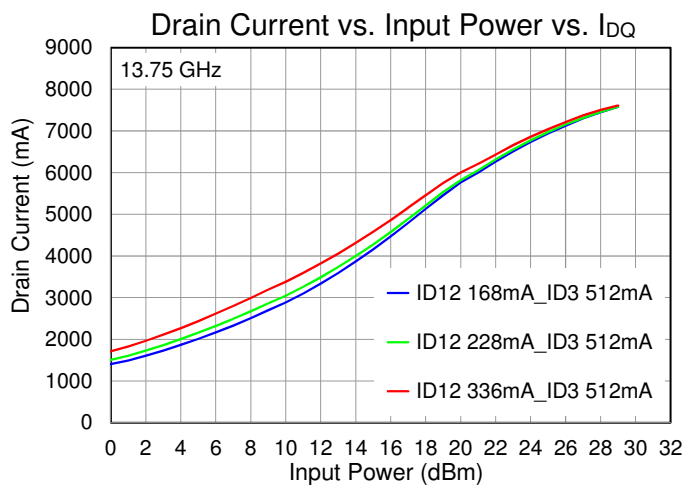
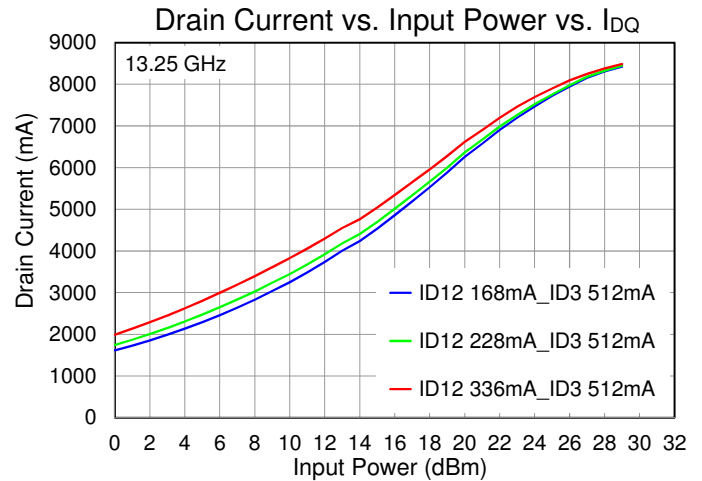
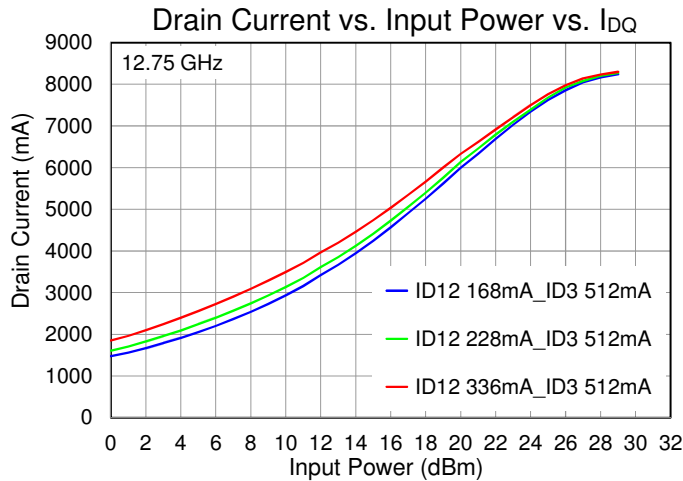
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $I_{D12} = 168\text{ mA}$ ,  $I_{D3} = 512\text{ mA}$ ,  $P_{IN} = 25\text{ dBm}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



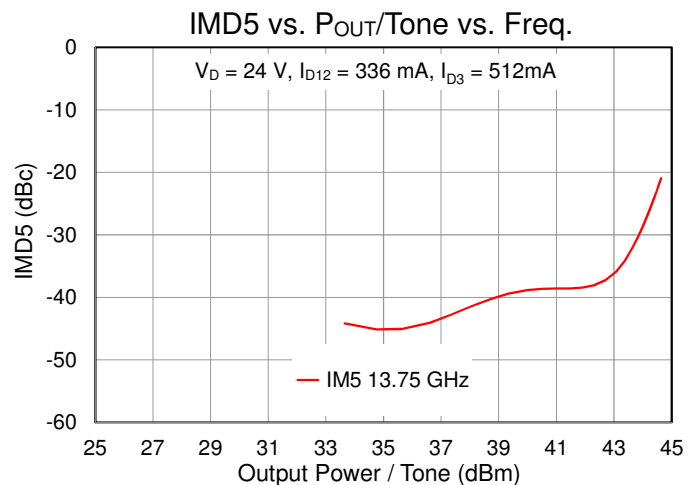
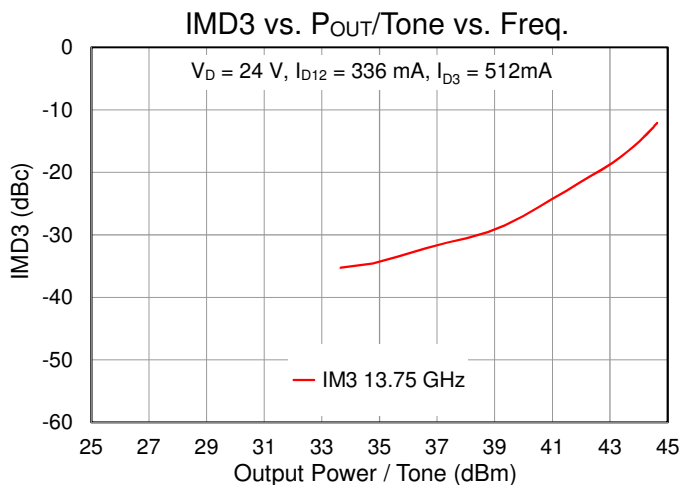
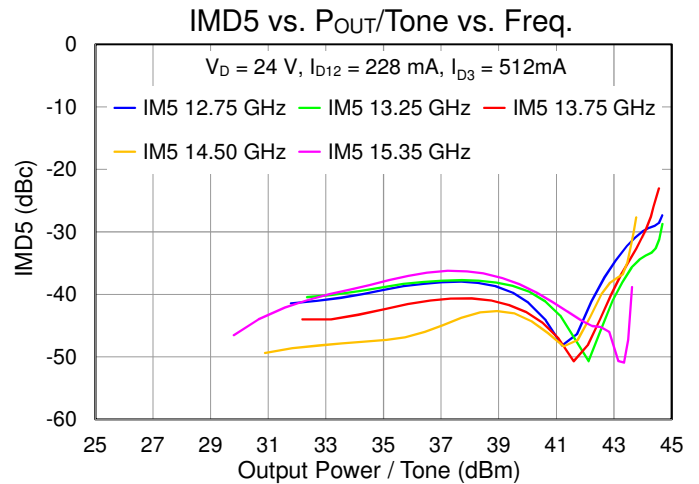
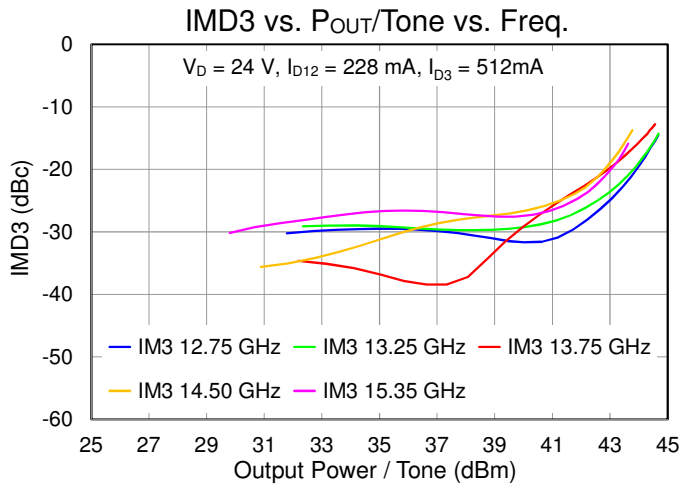
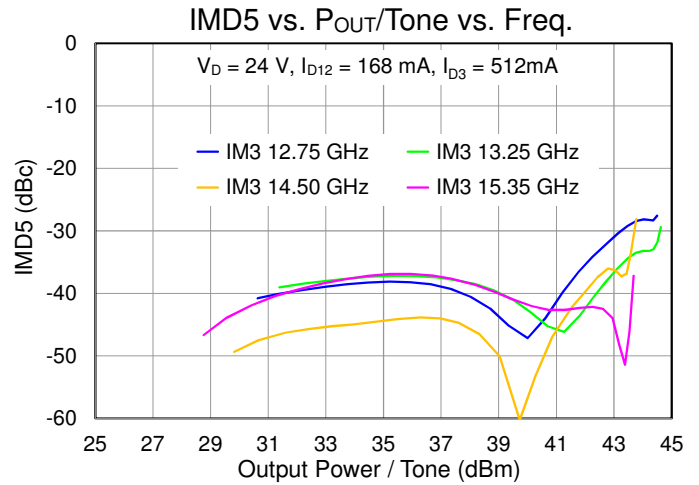
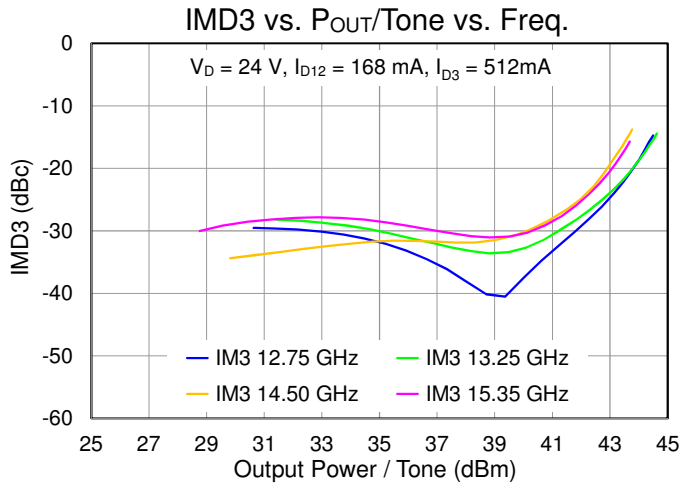
## Performance Plots – Large Signal

Test conditions, unless otherwise noted: **CW**,  $V_D = 24\text{ V}$ ,  $I_{D12} = 168\text{ mA}$ ,  $I_{D3} = 512\text{ mA}$ ,  $P_{IN} = 25\text{ dBm}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



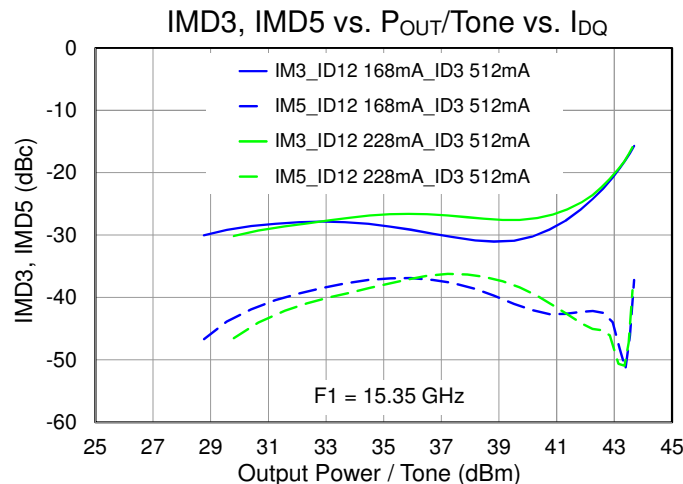
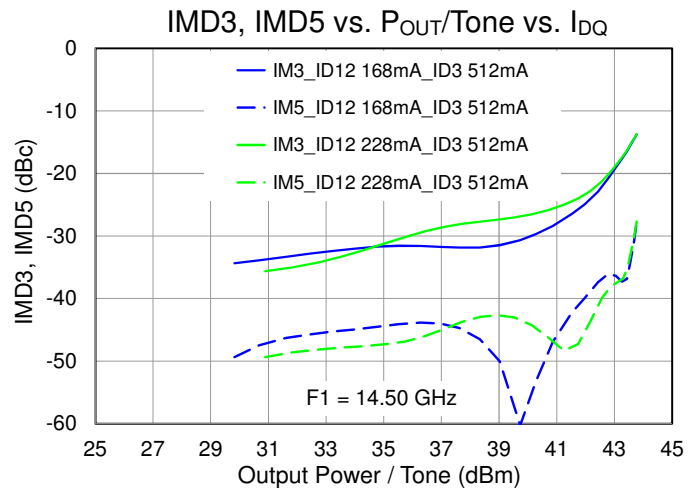
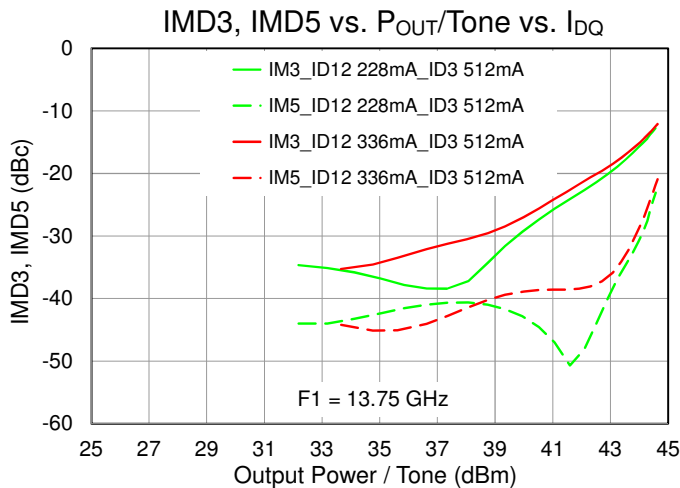
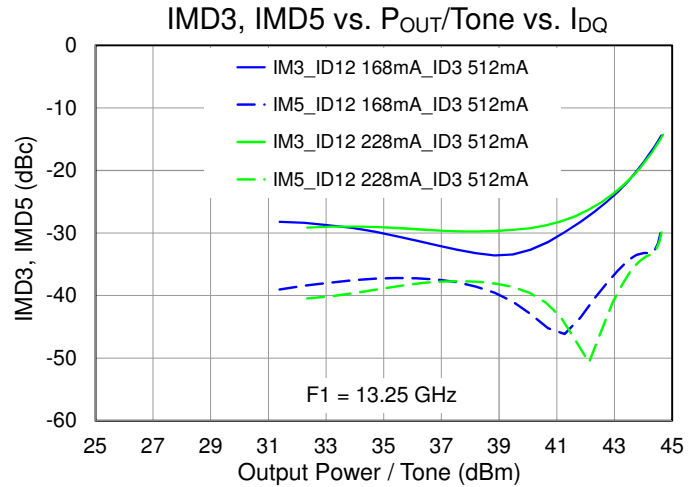
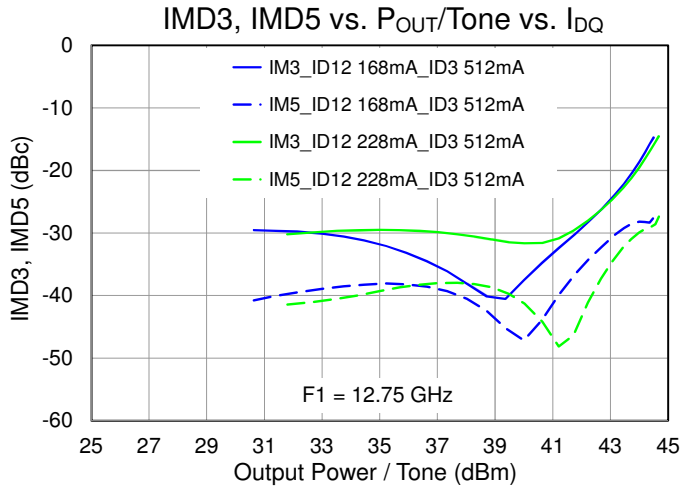
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $\Delta f = 10\text{ MHz}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



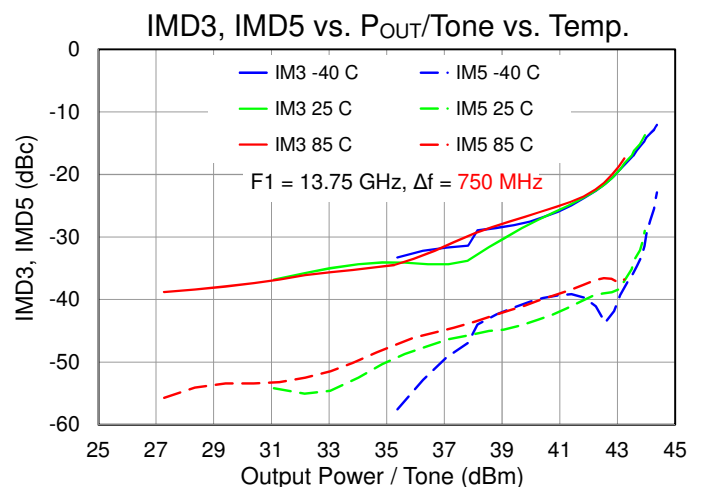
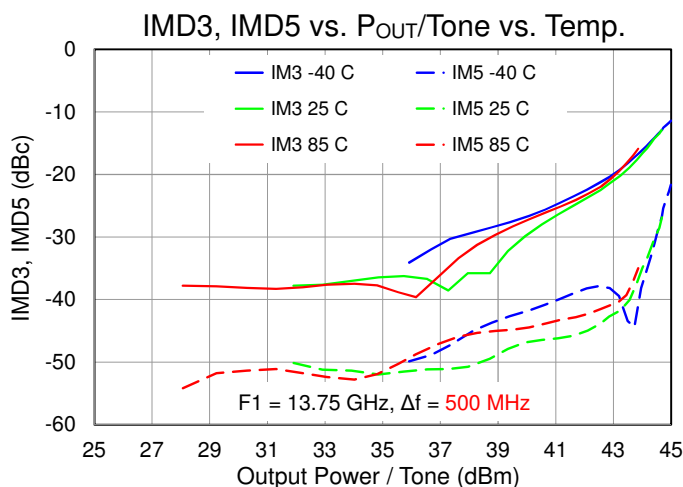
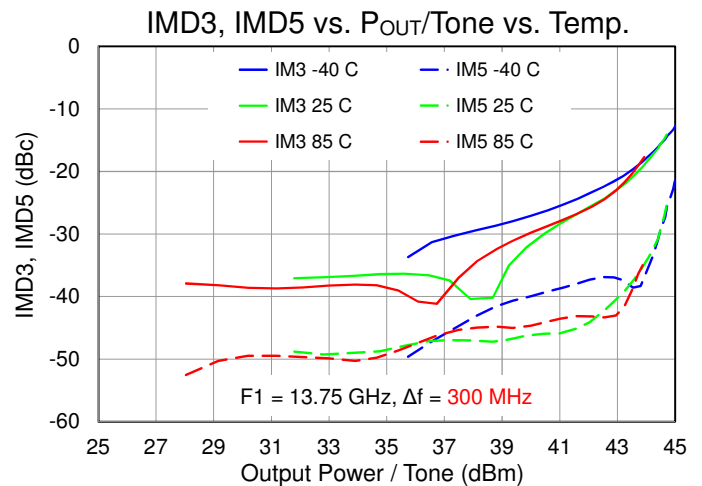
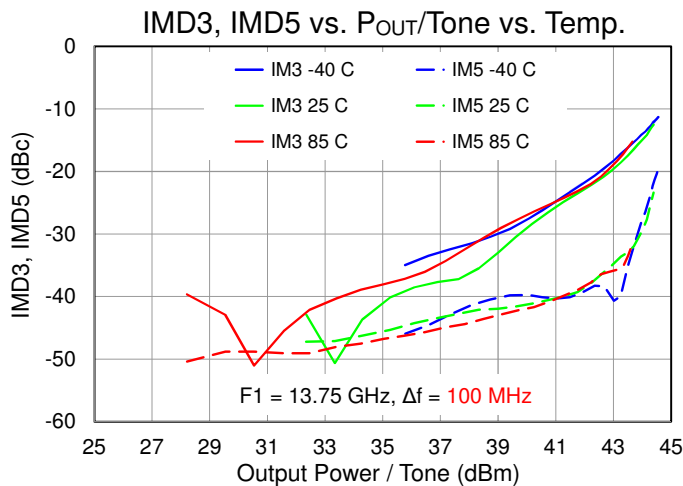
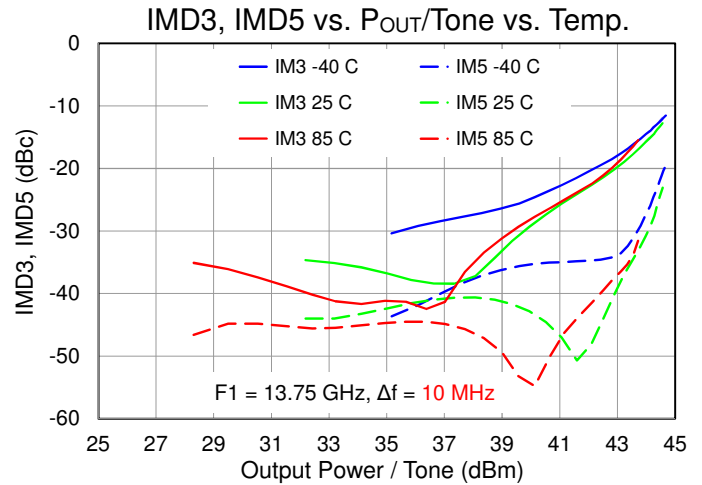
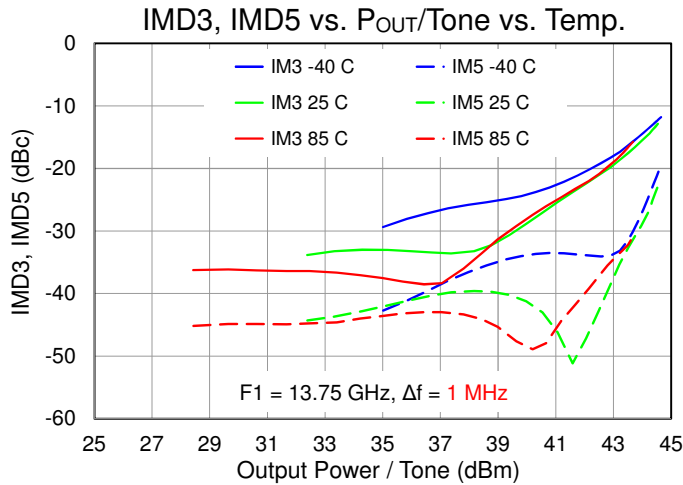
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $\Delta f = 10\text{ MHz}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



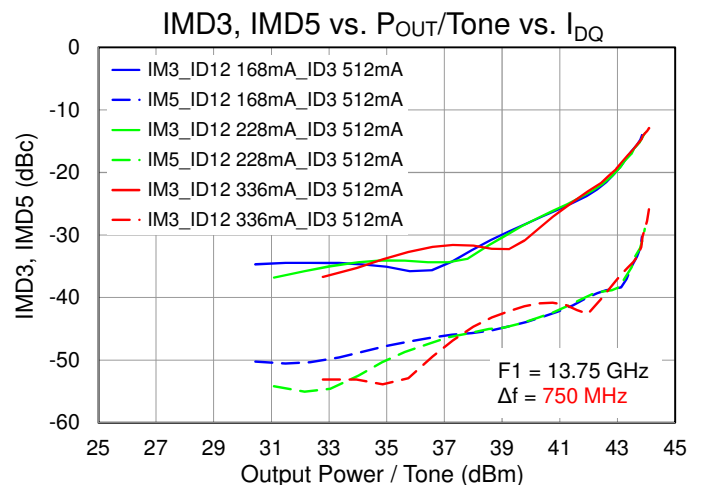
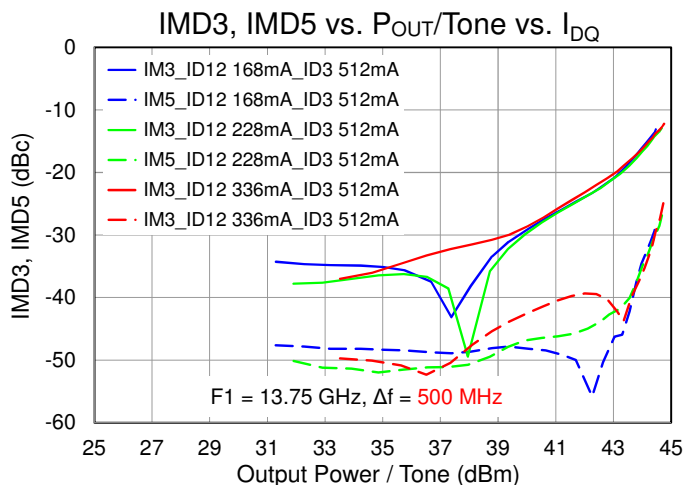
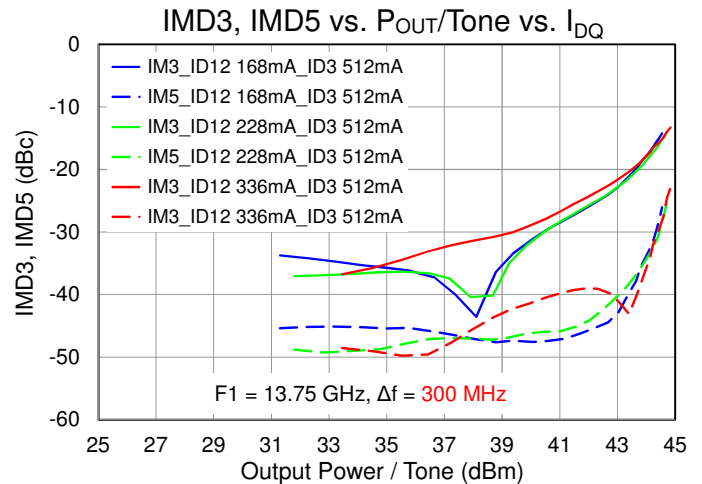
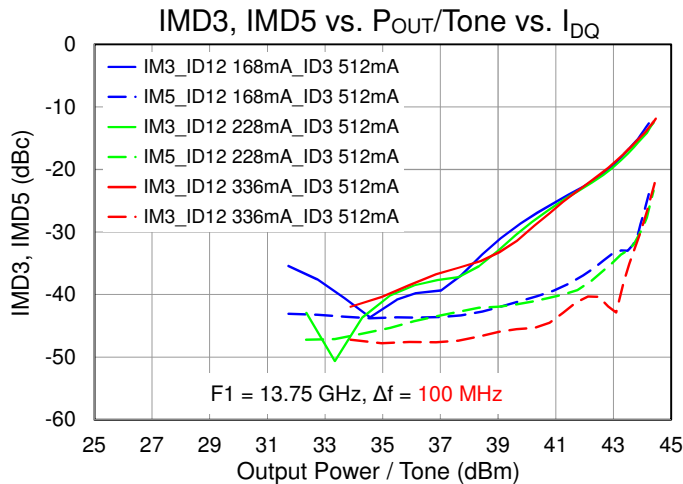
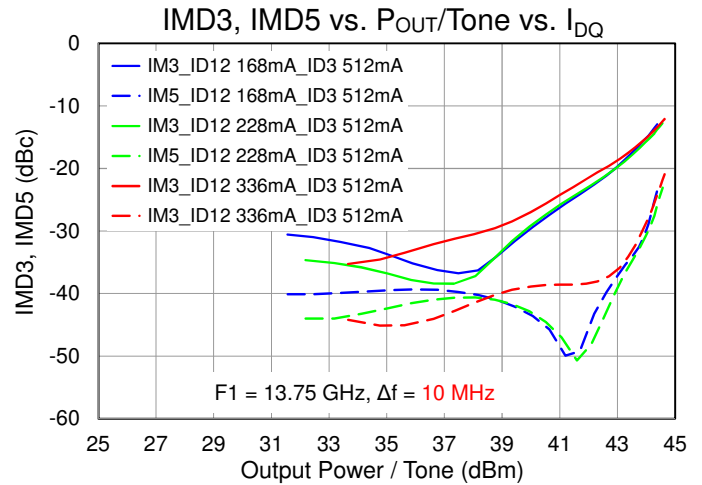
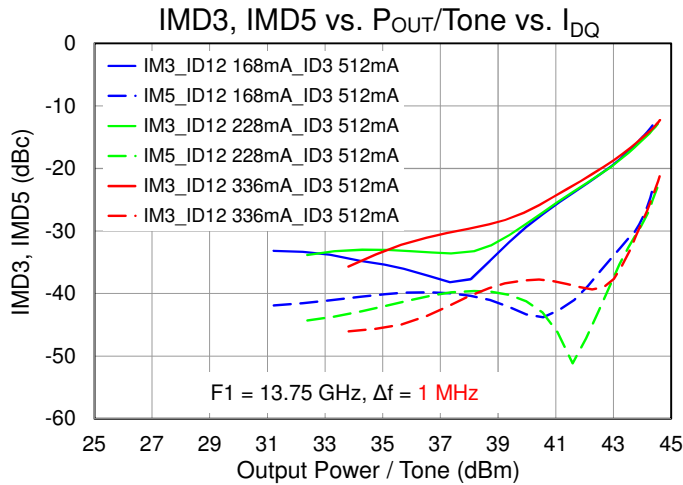
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $I_{D12} = 238\text{ mA}$ ,  $I_{D3} = 512\text{ mA}$ ,  $T_{BASE}$  is backside of 20 mil CuMo carrier plate



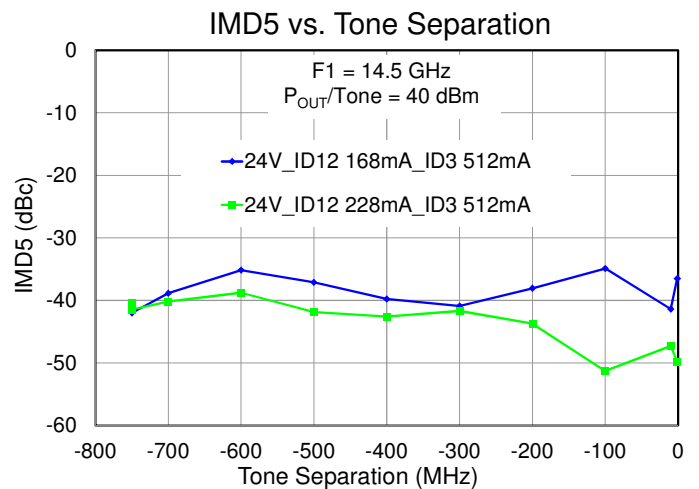
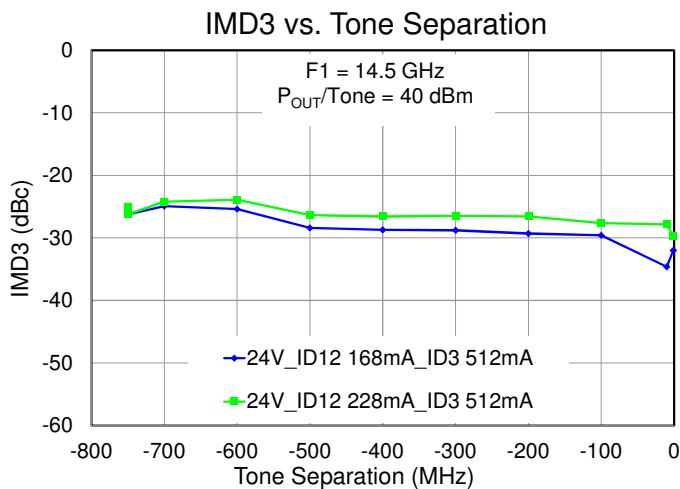
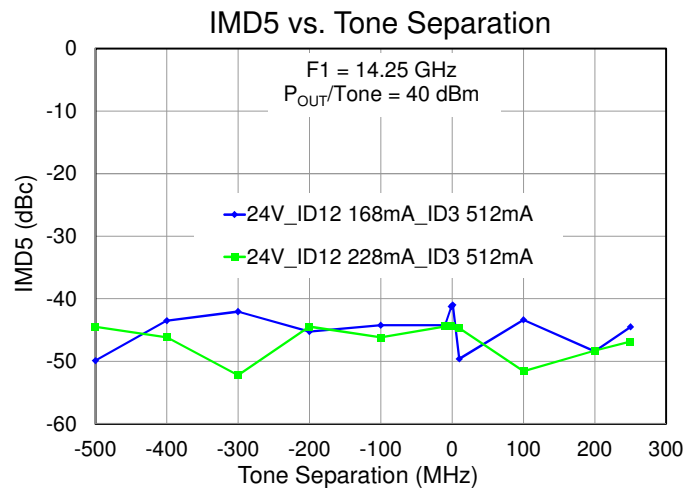
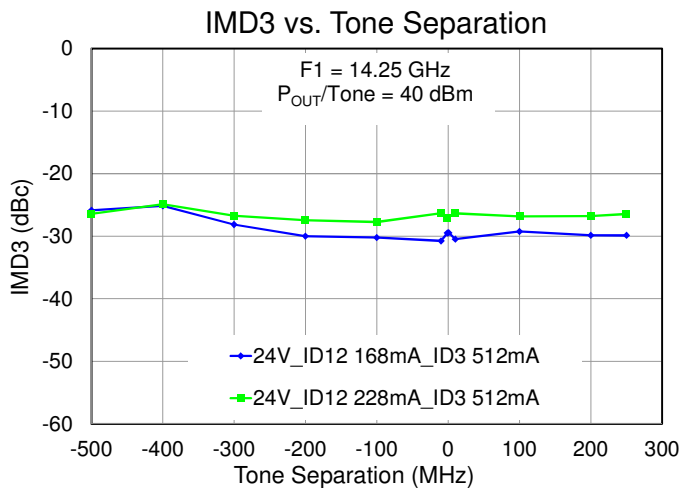
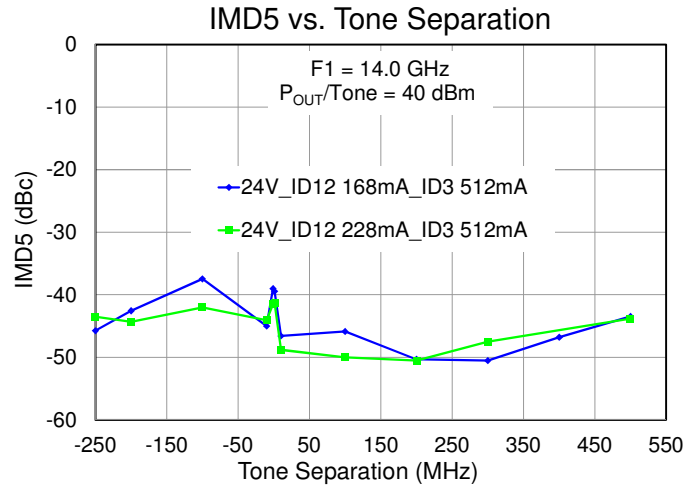
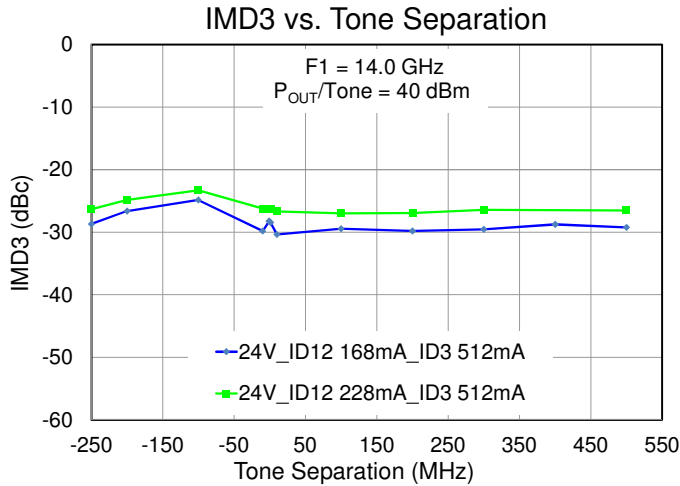
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



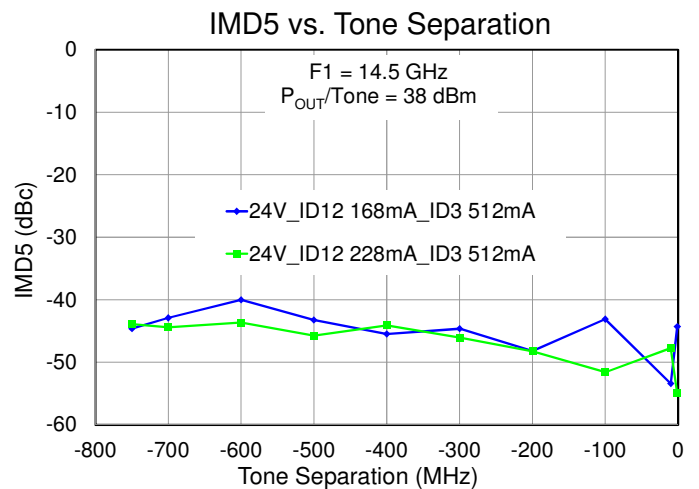
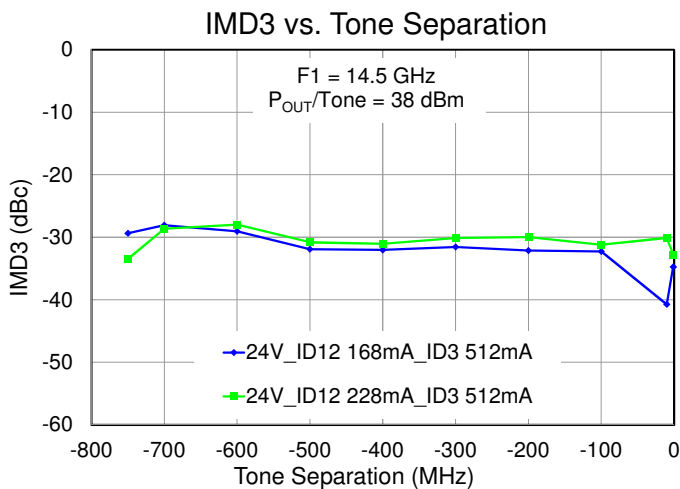
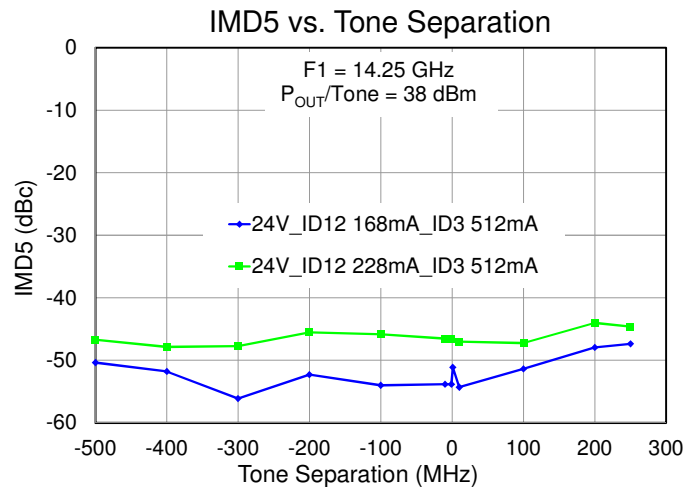
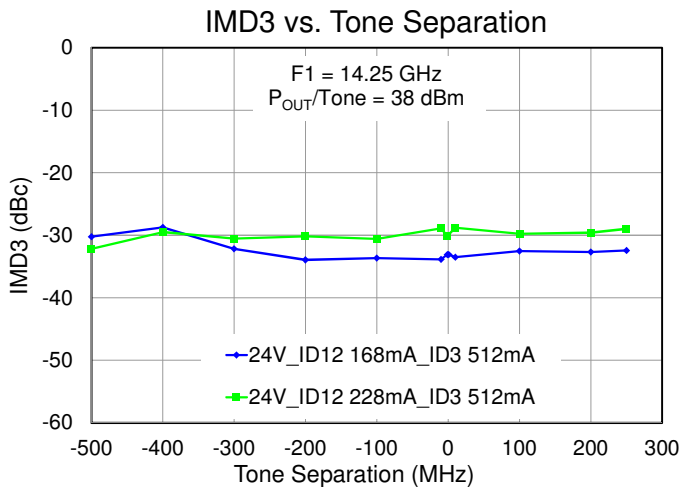
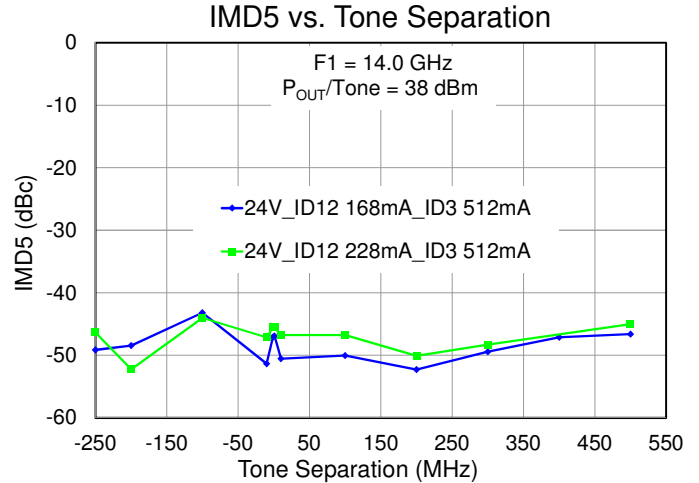
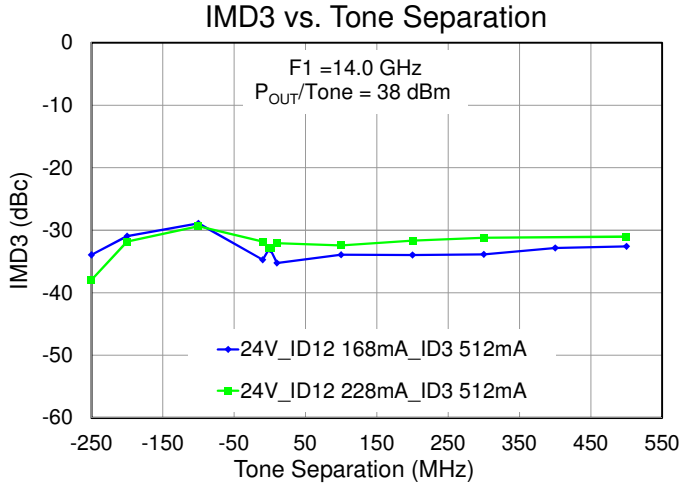
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



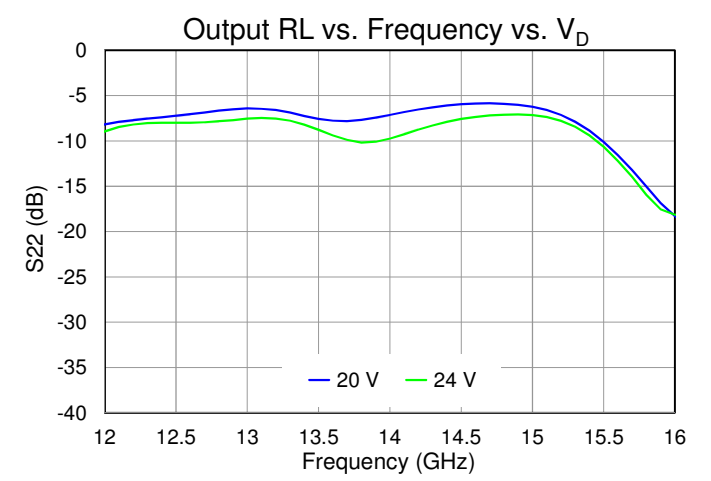
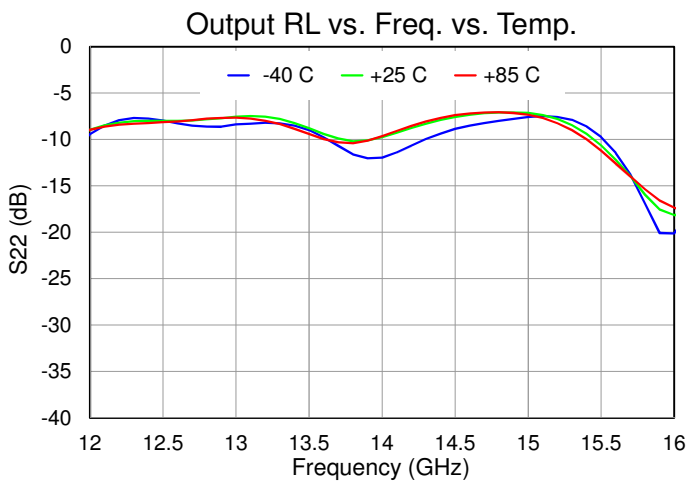
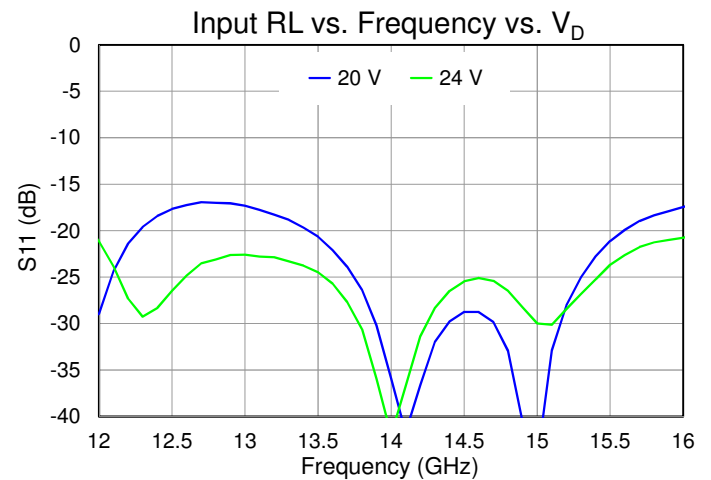
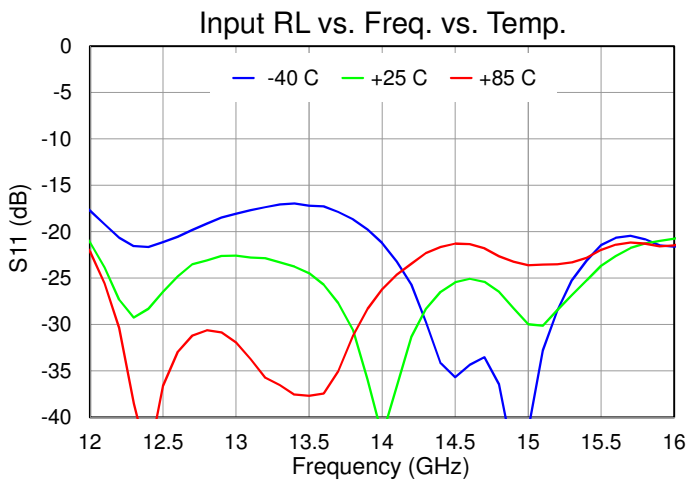
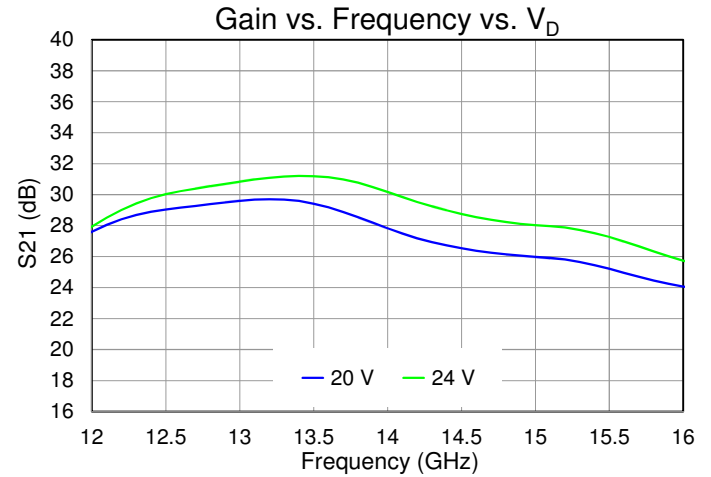
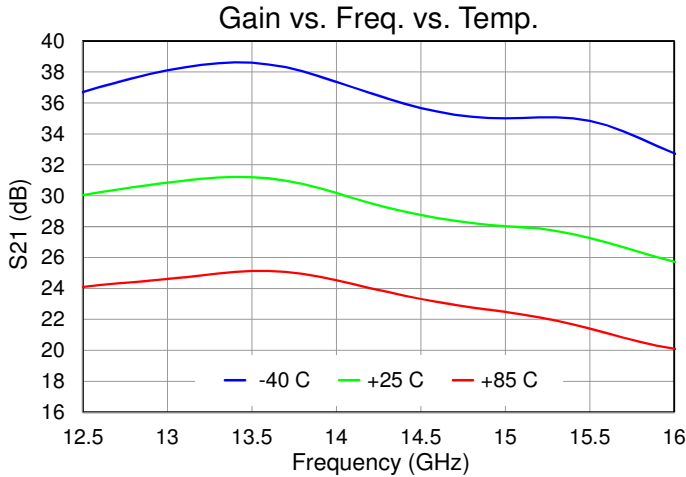
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



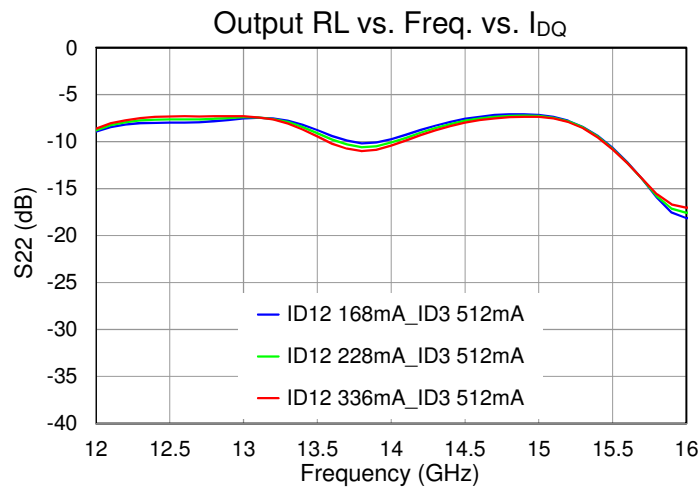
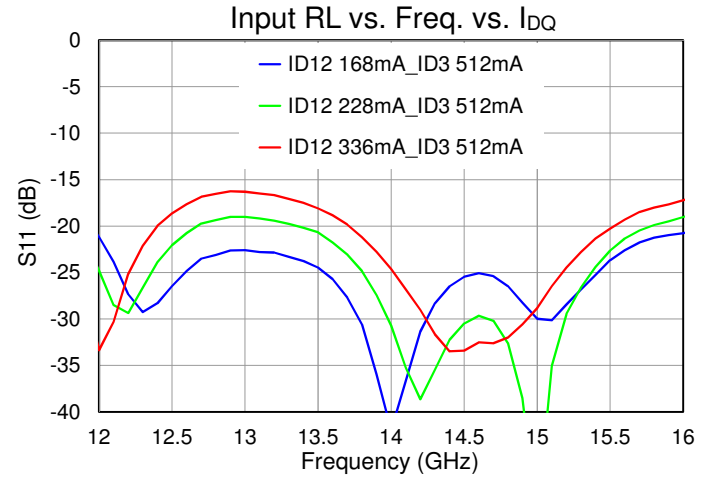
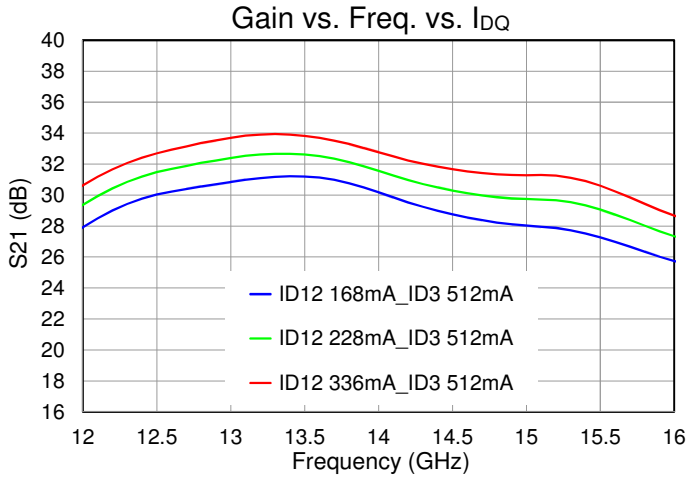
Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $I_{D12} = 168\text{ mA}$ ,  $I_{D3} = 512\text{ mA}$ ,  $P_{IN} = -30\text{ dBm}$ ,  $T_{BASE} = +25\text{ }^\circ\text{C}$  (backside of 20 mil CuMo carrier plate)



Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW,  $V_D = 24$  V,  $P_{IN} = -30$  dBm,  $T_{BASE} = +25$  °C (backside of 20 mil CuMo carrier plate)



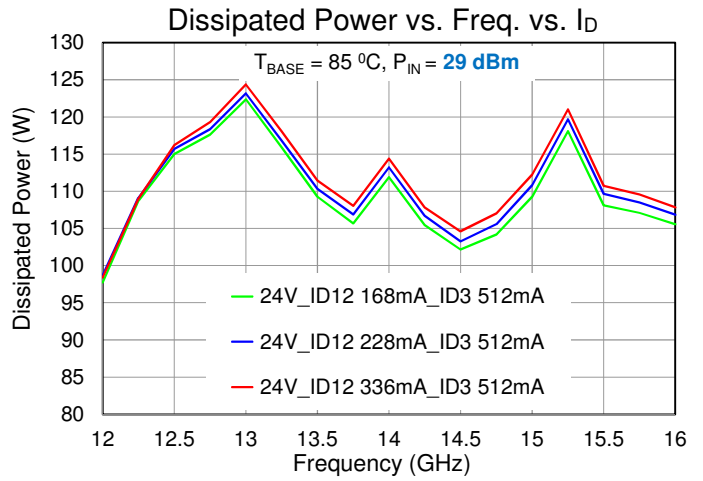
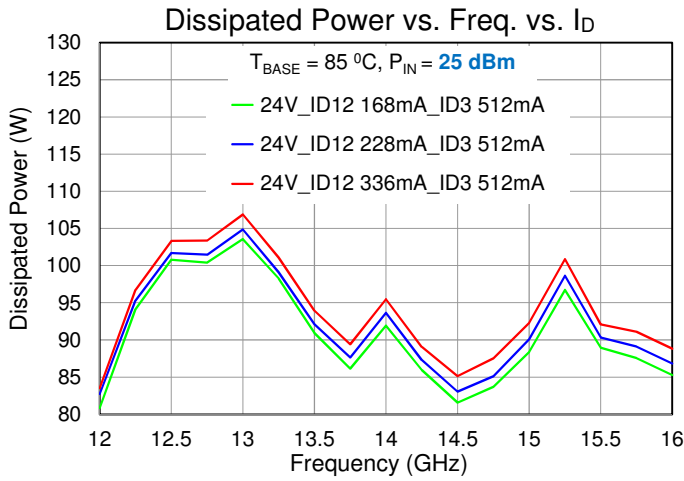
## Thermal and Reliability Information

Parameter	Test Conditions	Value	Units
Thermal Resistance, $\theta_{JC}$ <sup>(1)</sup>	Quiescent, no RF	0.70	$^{\circ}\text{C}/\text{W}$
Channel Temperature, $T_{CH}$ <sup>(2)</sup>	$T_{BASE} = 85^{\circ}\text{C}$ , $V_D = 24\text{ V}$ , $I_{D12} = 168\text{ mA}$ , $I_{D3} = 512\text{ mA}$ $P_{DISS} = 16.3\text{ W}$	96	$^{\circ}\text{C}$
Thermal Resistance, $\theta_{JC}$ <sup>(1)</sup>	<b>For 13.75 – 14.5 GHz:</b> $P_{IN} = 25\text{ dBm}$ , $T_{BASE} = 85^{\circ}\text{C}$ , CW, $V_D = 24\text{ V}$ , $I_{D12} = 168\text{ mA}$ , $I_{D3} = 512\text{ mA}$ , Freq = 14 GHz, $I_{D\_DRIVE}$ Total = 5560 mA, $P_{OUT} = 46.2\text{ dBm}$	0.73	$^{\circ}\text{C}/\text{W}$
Channel Temperature, $T_{CH}$ <sup>(2)</sup>	$P_{DISS} = 91.9\text{ W}$	152	$^{\circ}\text{C}$
Thermal Resistance, $\theta_{JC}$ <sup>(1)</sup>	<b>For 13.75 – 14.5 GHz</b> $P_{IN} = 25\text{ dBm}$ , $T_{BASE} = 85^{\circ}\text{C}$ , CW, $V_D = 24\text{ V}$ , $I_{D12} = 228\text{ mA}$ , $I_{D3} = 512\text{ mA}$ , Freq = 14 GHz, $I_{D\_DRIVE}$ Total = 5680 mA, $P_{OUT} = 46.3\text{ dBm}$	0.73	$^{\circ}\text{C}/\text{W}$
Channel Temperature, $T_{CH}$ <sup>(2)</sup>	$P_{DISS} = 93.7\text{ W}$	153	$^{\circ}\text{C}$
Thermal Resistance, $\theta_{JC}$ <sup>(1)</sup>	<b>For extended 12.75 – 15.35 GHz:</b> $P_{IN} = 25\text{ dBm}$ , $T_{BASE} = 85^{\circ}\text{C}$ , CW, $V_D = 24\text{ V}$ , $I_{D12} = 168\text{ mA}$ , $I_{D3} = 512\text{ mA}$ , Freq = 13 GHz, $I_{D\_DRIVE}$ Total = 5960 mA, $P_{OUT} = 46\text{ dBm}$	0.74	$^{\circ}\text{C}/\text{W}$
Channel Temperature, $T_{CH}$ <sup>(2)</sup>	$P_{DISS} = 104\text{ W}$	162	$^{\circ}\text{C}$
Thermal Resistance, $\theta_{JC}$ <sup>(1)</sup>	<b>For extended 12.75 – 15.35 GHz:</b> $P_{IN} = 25\text{ dBm}$ , $T_{BASE} = 85^{\circ}\text{C}$ , CW, $V_D = 24\text{ V}$ , $I_{D12} = 228\text{ mA}$ , $I_{D3} = 512\text{ mA}$ , Freq = 13 GHz, $I_{D\_DRIVE}$ Total = 6028 mA, $P_{OUT} = 46\text{ dBm}$	0.74	$^{\circ}\text{C}/\text{W}$
Channel Temperature, $T_{CH}$ <sup>(2)</sup>	$P_{DISS} = 105\text{ W}$	163	$^{\circ}\text{C}$
Thermal Resistance, $\theta_{JC}$ <sup>(1)</sup>	<b>For 13.75 – 14.5 GHz:</b> $P_{IN} = 29\text{ dBm}$ , $T_{BASE} = 85^{\circ}\text{C}$ , CW, $V_D = 24\text{ V}$ , $I_{D12} = 168\text{ mA}$ , $I_{D3} = 512\text{ mA}$ , Freq = 14 GHz, $I_{D\_DRIVE}$ Total = 6925 mA, $P_{OUT} = 47.4\text{ dBm}$	0.75	$^{\circ}\text{C}/\text{W}$
Channel Temperature, $T_{CH}$ <sup>(2)</sup>	$P_{DISS} = 112\text{ W}$	169	$^{\circ}\text{C}$
Thermal Resistance, $\theta_{JC}$ <sup>(1)</sup>	<b>For extended 12.75 – 15.35 GHz:</b> $P_{IN} = 29\text{ dBm}$ , $T_{BASE} = 85^{\circ}\text{C}$ , CW, $V_D = 24\text{ V}$ , $I_{D12} = 168\text{ mA}$ , $I_{D3} = 512\text{ mA}$ , Freq = 13 GHz, $I_{D\_DRIVE}$ Total = 7275 mA, $P_{OUT} = 47.2\text{ dBm}$	0.76	$^{\circ}\text{C}/\text{W}$
Channel Temperature, $T_{CH}$ <sup>(2)</sup>	$P_{DISS} = 123\text{ W}$	179	$^{\circ}\text{C}$

**Notes:**

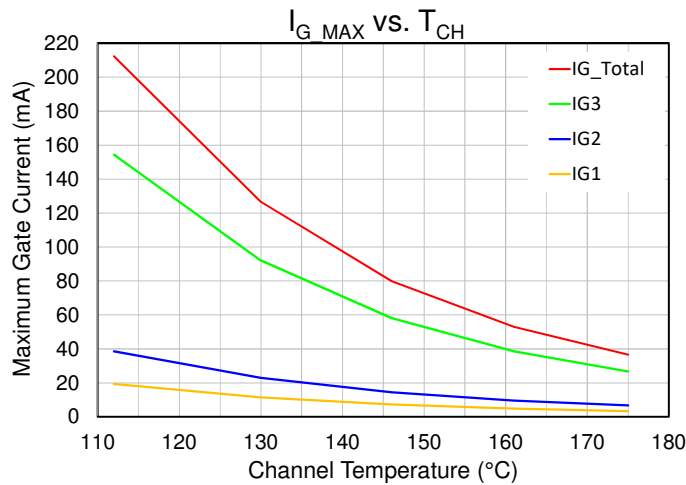
1. Thermal resistance determined to the back of 20 mil carrier plate CuMo with AuSn die attached
2. Channel temperature indicated is an IR scan equivalent temperature. Thermal resistance is calculated using this value. Additional information can be found in the Qorvo Applications Note "GaN Device TCHMAX Theta-JC and Reliability Estimates," located here <https://www.qorvo.com/products/d/da006480>

Dissipated Power and Maximum Gate Current



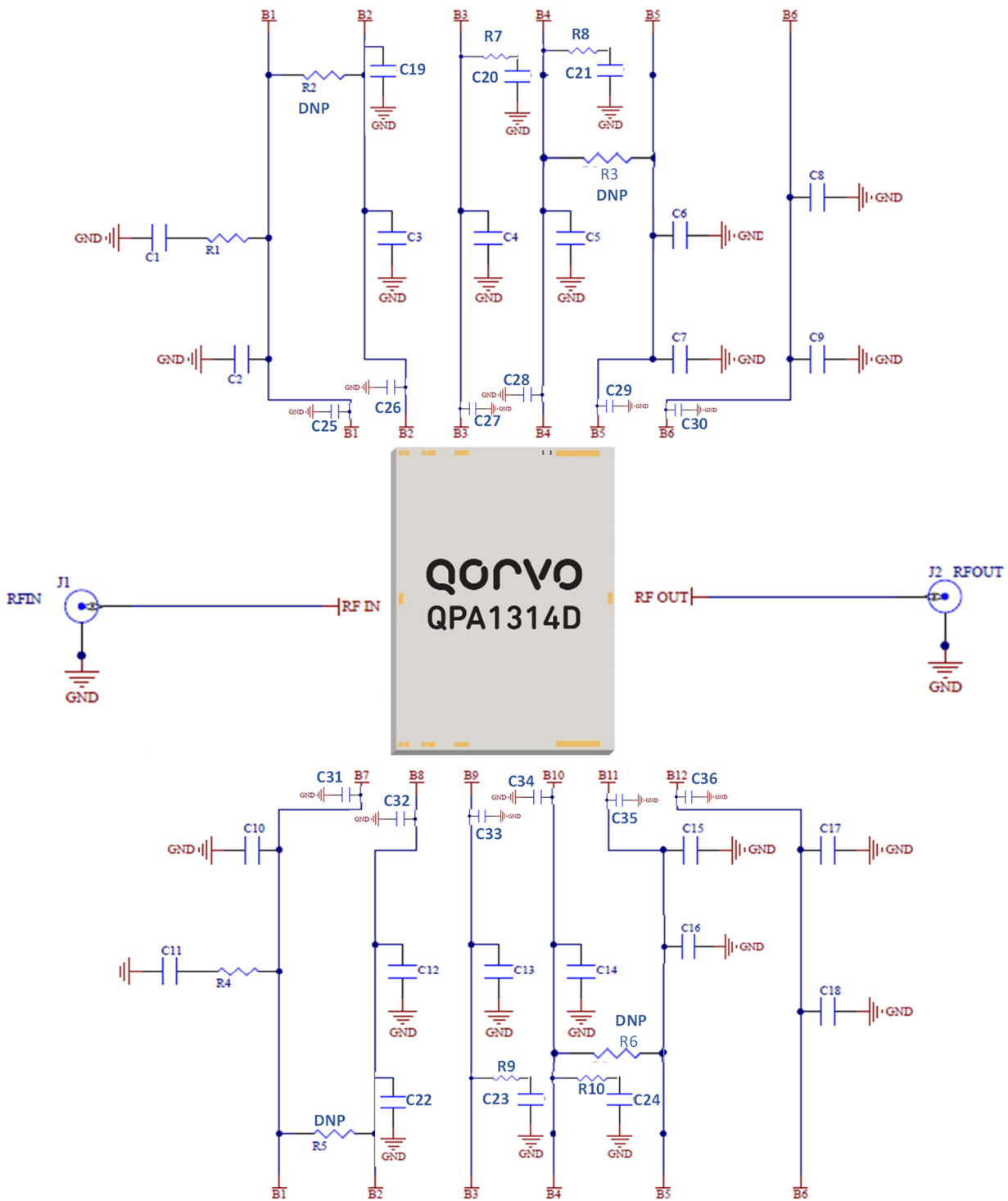
Test conditions, unless otherwise noted: CW,  $V_D = 24\text{ V}$ ,  $I_{D12} = 168, 228\text{ mA}$ ,  $I_{D3} = 512\text{ mA}$ ,  $P_{IN} = 25, 29\text{ dBm}$ ,  $T_{BASE} = +85\text{ }^\circ\text{C}$ ,  $T_{BASE}$  is back side of 20 mil CuMo carrier plate with AuSn die attached

Maximum Gate Current



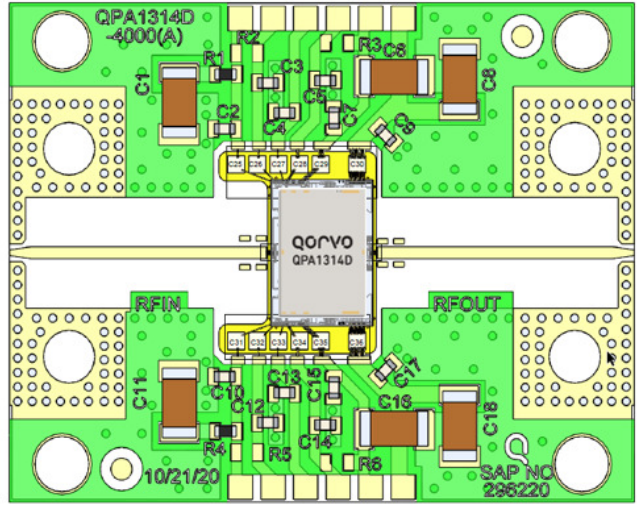
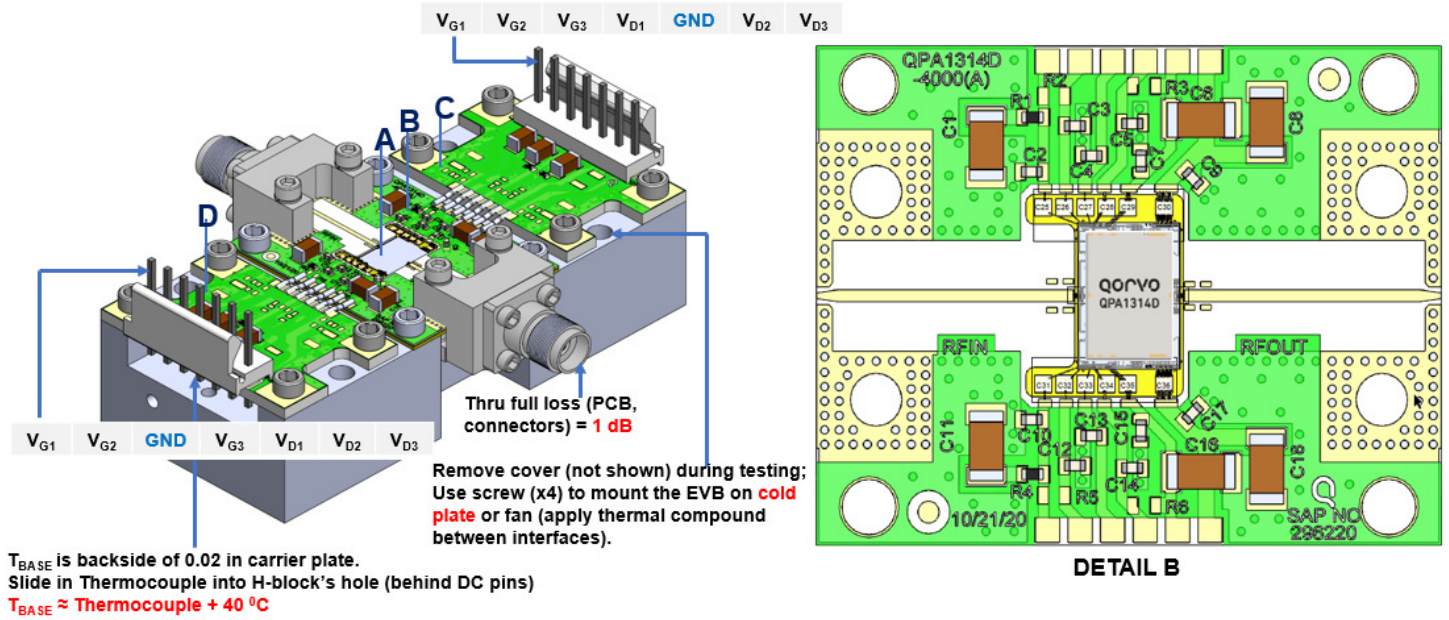
Channel Temperature is an IR scan equivalent

**Applications Information**

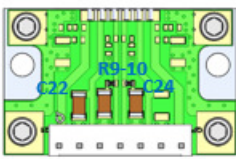
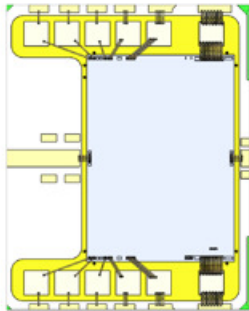
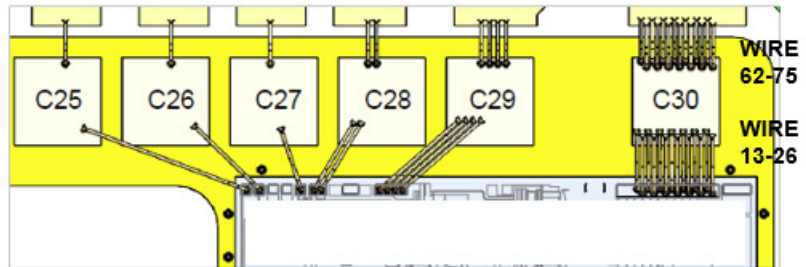
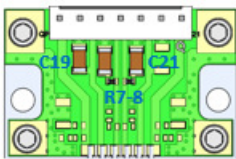


DC can be applied from top, or bottom, or both sides of the dies;  
External bypassing required on both sides

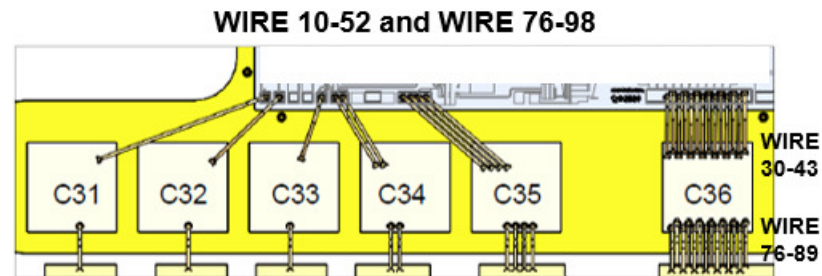
Evaluation Board (EVB) Layout



V<sub>G1</sub> V<sub>G2</sub> V<sub>G3</sub> V<sub>D1</sub> GND V<sub>D2</sub> V<sub>D3</sub>



V<sub>G1</sub> V<sub>G2</sub> GND V<sub>G3</sub> V<sub>D1</sub> V<sub>D2</sub> V<sub>D3</sub>



## Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1, C6, C8, C11, C16, C18 – C24	12	10 uF	CAP, 10uF, 20%, 50V, 20%, X5R, 1206	
C2 – C5, C7, C9 – 10, C12 – C15, C17	12	0.01 uF	CAP, 0.01uF, ±10%, 50V, X7R, 0402	
C25 – C36	12	10 nF	CAP, 10nF, ±15%, 30V, SLC, 0303	
R1, R4, R7 – R10	6	0 Ω	RES, 0 Ohm, JMPR, 0402	
PCB_MMIC	1		PCB for MMIC, Taconics RF-35HTC 0.01", 0.5oz Ni/Pd/Au plating both sides, total thickness 0.14"	Qorvo, Custom
PCB,_Bias	2		PCB for DC Bias	Qorvo, Custom
H1, H2	2		CONN, HDR, Male-vert, 7 PIN, 1 RAW, MTA	
J1, J2	2		Connector, RF 2.9mm, F, Pin 0.005, Diel 0.029	Southwest Microwave 1092-01A-5
CP	1		Carrier Plate, CuMo, 0.9 x 1.15 x 0.02T	Qorvo, Custom
H-Block	1		H-Block, Copper C110, 1.14 x 2.49 x 0.59T	Qorvo, Custom
S1 – S4	4		Screw, Cap, Socket Head, 2-56X1/8"	
S5 – S12	8		Screw, Cap, Socket Head, 2-56X3/16"	
AuSn			AuSn Solder preform	
Epoxy			Epoxy preform	
Ablebond			Epoxy, Ablebond 84-1LMI	
Solder			Paste, solder, Syntech, Sn63/Pb37	
TC			Thermal Compound, Silver 5GR	Artic Silver 5 AS5-5G

## Bias-Up Procedure

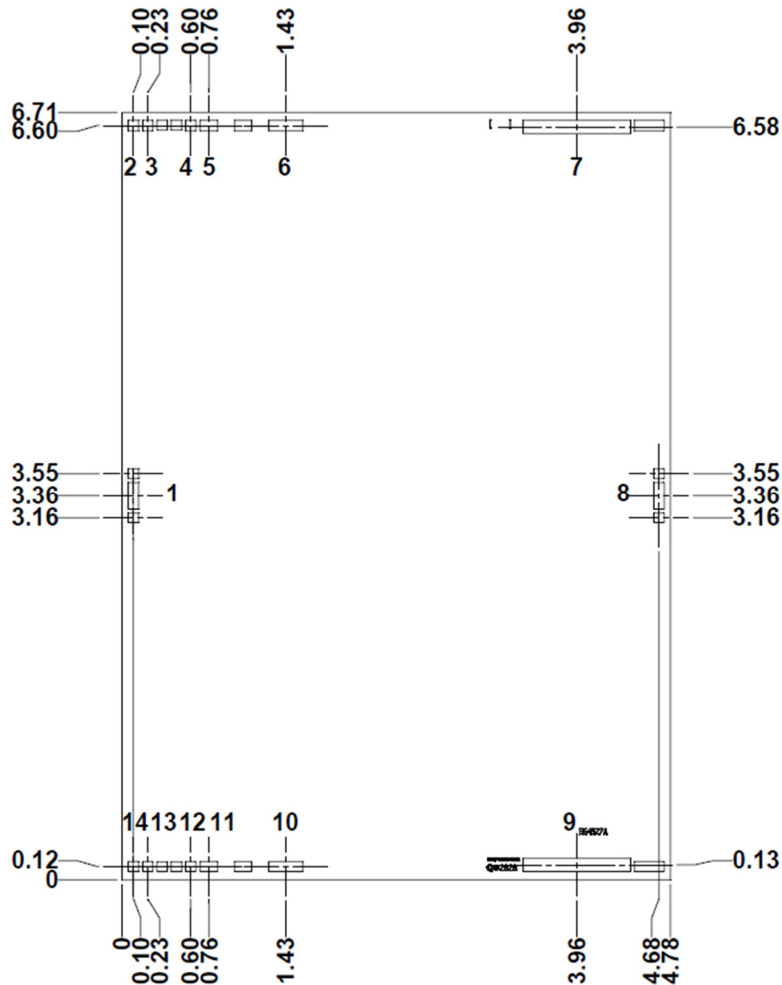
1. Set  $I_D$  limit to 9.5 A,  $I_G$  limit to 15 mA
2. Set  $V_{G12}$  to  $-5.0$  V;  $V_{G3}$  to  $-5.0$  V
3. Set  $V_D$  +24 V. Ensure  $I_{DQ} \sim 0$  mA
4. Adjust  $V_{G12}$  more positive until  $I_{D12} = 168$  mA;  
Adjust  $V_{G3}$  more positive until  $I_{D3} = 512$  mA;  
 $V_G \approx -2.3$  V +/- 0.6V typical range
5. Apply RF signal

## Bias-Down Procedure

1. Turn off RF signal
2. Reduce  $V_G$  to  $-5.0$  V. Ensure  $I_{DQ} \sim 0$  mA
3. Set  $V_D$  to 0 V
4. Turn off  $V_D$  supply
5. Turn off  $V_G$  supply

If using three (3) bias supplies for  $V_D$ ,  $V_{G12}$ ,  $V_{G3}$ : combining all three  $V_D$  together, combining  $V_{G1}$  and  $V_{G2}$  as  $V_{G12}$ , adjusting  $V_{G12}$  to achieve  $I_D = I_{D12}$ , then adjusting  $V_{G3}$  to achieve  $I_{D3}$  where  $I_D = I_{D12} + I_{D3}$

Mechanical Information



Dimensions: mm; Thickness: 0.10 mm; Die x, y size tolerance: ± 0.050; Ground is backside of die

Bond Pad Description

Pad No.	Symbol	Pad Size (mm)	Description
1	RF <sub>IN</sub>	0.09 x 0.24	RF Input. Matched to 50 Ω, DC blocked, DC shorted to ground
2, 14	V <sub>G1</sub>	0.09 x 0.09	Gate voltage for stage 1*
3, 13	V <sub>G2</sub>	0.09 x 0.09	Gate voltage for stage 2*
4, 12	V <sub>G3</sub>	0.09 x 0.09	Gate voltage for stage 3*
5, 11	V <sub>D1</sub>	0.15 x 0.09	Drain voltage for stage 1*
6, 10	V <sub>D2</sub>	0.30 x 0.09	Drain voltage for stage 2*
7, 9	V <sub>D4</sub>	0.94 x 0.12	Drain voltage for stage 3*
8	RF <sub>OUT</sub>	0.09 x 0.24	RF Output. Matched to 50 Ω, DC blocked, DC shorted to ground

\* External bypassing required; refer to page 26 for recommendation

## Assembly Notes

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Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300 °C to 3–4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonic are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001



Caution!

ESD-Sensitive Device

## Solderability

Use only AuSn (80/20) solder, and limit exposure to temperatures above 300 °C to 3–4 minutes, maximum.

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- SVHC Free
- PFOS Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Tel: 1-844-890-8163

Email: [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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