APPLICATION NOTE

Application Note 103

Amplifier Biasing Techniques

Introduction

Application Note 103 describes a single-supply biasing scheme for a number of Custom MMIC amplifiers that nominally require two positive bias voltages, one for the drain and one for the gate. Following a list of pertinent amplifiers, we present the recommended biasing scheme with two supplies followed by the alternate scheme with a single supply.

Applicable Custom MMIC Amplifiers

This application applies only to the list of Custom MMIC amplifiers presented below in Table 1. NOTE: This biasing scheme is NOT approved for amplifiers outside of this list, including all of the GaN amplifiers and any others which require a negative gate voltage. For all other amplifiers, please refer to the recommended biasing scheme as printed on the respective data sheet.

CMD159	CMD171P4	CMD207	CMD247	CMD298
CMD160	CMD173	CMD228	CMD274P4	CMD298C4
CMD160C4	CMD173P4	CMD228P4	CMD275	CMD299
CMD161	CMD187	CMD229	CMD275P4	CMD299K4
CMD162	CMD187C4	CMD229P4	CMD283C3	CMD311P34
CMD163	CMD188	CMD245	CMD284	CMD319C3
CMD163C4	CMD189P3	CMD245C4	CMD284P4	CMD320C3
CMD169P4	CMD190	CMD246	CMD295	CMD326
CMD170P4	CMD206	CMD246C4	CMD295C4	CMD327

Table 1. List Of CMDS Amplifiers Covered By This Application Note.

Biasing Approach

The preferred dual biasing scheme for the amplifiers in Table 1 is printed on the respective data sheets, and is repeated below for reference:

Turn ON procedure:

Apply the drain voltage Vdd and set it to +XX V then apply gate voltage Vgg and set it to +YY V.

Biasing Approach (cont.)

Turn OFF procedure:

Turn off the gate voltage Vgg and then turn off the drain voltage Vdd.

The recommended biasing procedure has been proven to be robust, and should be used whenever possible. However, the amplifiers listed in Table 1 do allow for simultaneous biasing (applying Vdd and Vgg at the same time), and the use of a single voltage supply.

To utilize the single supply approach, a resistor must be connected between the Vdd and Vgg ports of the amplifier. In Figure 1 below, we present an example of this technique as applied to the CMD163C4 low noise amplifier.

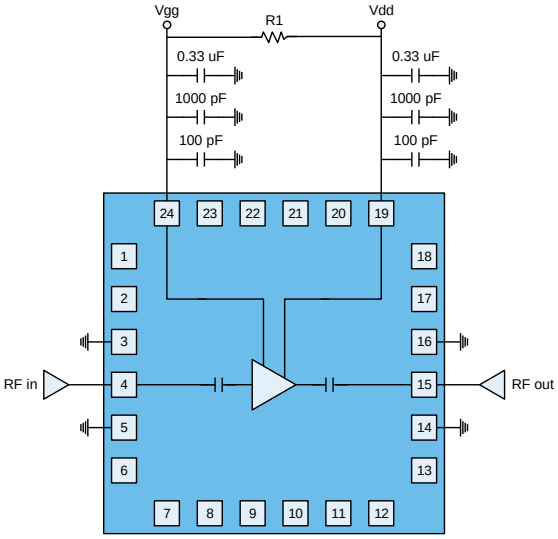

Figure 1. Schematic Of The CMD163C4 Configured For A Single Supply. Bias Is Applied To The Vdd Port.

In this figure, we have connected resistor R1 between the Vdd and Vgg ports, and connected a single voltage supply is connected to the Vdd port.

The value of R1 can be calculated based upon the applied drain voltage Vdd, the required gate voltage Vgg, and the required gate current, Igg. The relationship between these variables is given below in Equation 1.

$$R1 \sim \frac{Vdd - Vgg}{Igg} \quad (Eq.1)$$

CMD163C4 Single Supply Bias Example

In our example, the CMD163C4 requires Vdd = 4 V, Vgg = 3 V, and Igg = 5 mA. Using Equation 1, the calculated value of R1 is 200 Ohms. The actual value of R1 may be limited by standard available resistors, but should be as close to the calculated value as possible. Some experimentation in resistor values may be necessary to generate the required gate voltage and current.

In terms of implementing R1, it is important to choose a resistor with a rating above the expected power dissipation. In this example, R1 must dissipate approximately 5 mW of power, which is well within 0.125 W power dissipation rating of standard axial leaded resistors and chip resistors. Finally, we note it is important to keep all the bypassing and decoupling capacitors on both the Vdd and Vgg ports as shown in the data sheet.

In Table 2 below, we present the bias conditions for the amplifiers as listed in Table 1, along with the calculated value of R1, rounded to the nearest standard value. A “0” Ohm resistor can be replaced by a short circuit.

CMD #	Vdd [V]	Vgg [V]	Igg [mA]	Target Idd [mA]	R1 [Ω]
159	3.0	1.5	2.8	29	560
160	3.0	1.5	2.4	26	680
160C4	3.0	1.5	2.4	26	680
161	3.0	1.5	2.8	20	560
162	2.0	2.0	4.7	25	0
163	4.0	3.0	5.1	120	220
163C4	4.0	3.0	5.1	120	220
169P4*	7.0	3.0	19.2	375	220
170P4*	7.0	3.0	19.0	365	220
171P4*	7.0	3.0	0.6	380	6800
173	8.0	3.0	0.9	78	5600
173P4	8.0	3.0	0.9	78	5600
187	3.0	2.0	0.7	115	1500
187C4	3.0	2.0	0.7	115	1500
188	2.0	2.0	5.4	20	0
189P3	1.5	1.5	2.9	20	0
190	2.0	2.0	5.0	25	0
206	4.0	3.0	0.9	32	1200
207	4.0	3.0	2.7	270	390
228	4	4	5	45	0
228P4	4	4	5	45	0
229	4	4	5.8	45	0
229P4	4	4	5.8	45	0
245	5	3	5.1	76	390
245C4	5	3	5.1	76	390
246	5	3	4.4	48	470
246C4	5	3	4.4	48	470
247	3	3	3.8	28	0
274P4	5	3	5.0	86	390
275	5	3	3.7	74	560
275P4	5	3	3.7	74	560

CMD163C4 Single Supply Bias Example

CMD #	Vdd [V]	Vgg [V]	Igg [mA]	Target Idd [mA]	R1 [Ω]
283C3	3	1.5	0.5	42	3000
284	8	3	1.2	108	3900
284P4	8	3	1.2	108	3900
295	3	2	1.0	145	1000
295C4	3	2	1.0	145	1000
298	3	1.5	0.8	27	1800
298C4	3	1.5	0.8	27	1800
299	3	3	2.3	33	0
299K4	3	3	2.3	33	0
311P34	5	5	1.5	40	0
319C3	3.0	1.5	2.0	30	820
320C3	3.0	1.5	2.0	32	820
326	5.0	3.0	3.3	180	560
327	5.0	3.0	3.6	100	560

Table 2 Summary of bias conditions and R1 value for CMDS amplifiers using a single supply.

NOTE: In parts marked with a (*), Vgg is referred to as Venable on the datasheet.

CMD163C4 Single Supply Bias Example (cont.)

In Figure 3 below, we present a comparison of the preferred dual biasing scheme to the use of a single supply for the CMD163C4 amplifier. Here, we compare the measurements of the S-parameters. We note the measurements using the single supply agree very well with the dual supply approach, as expected.

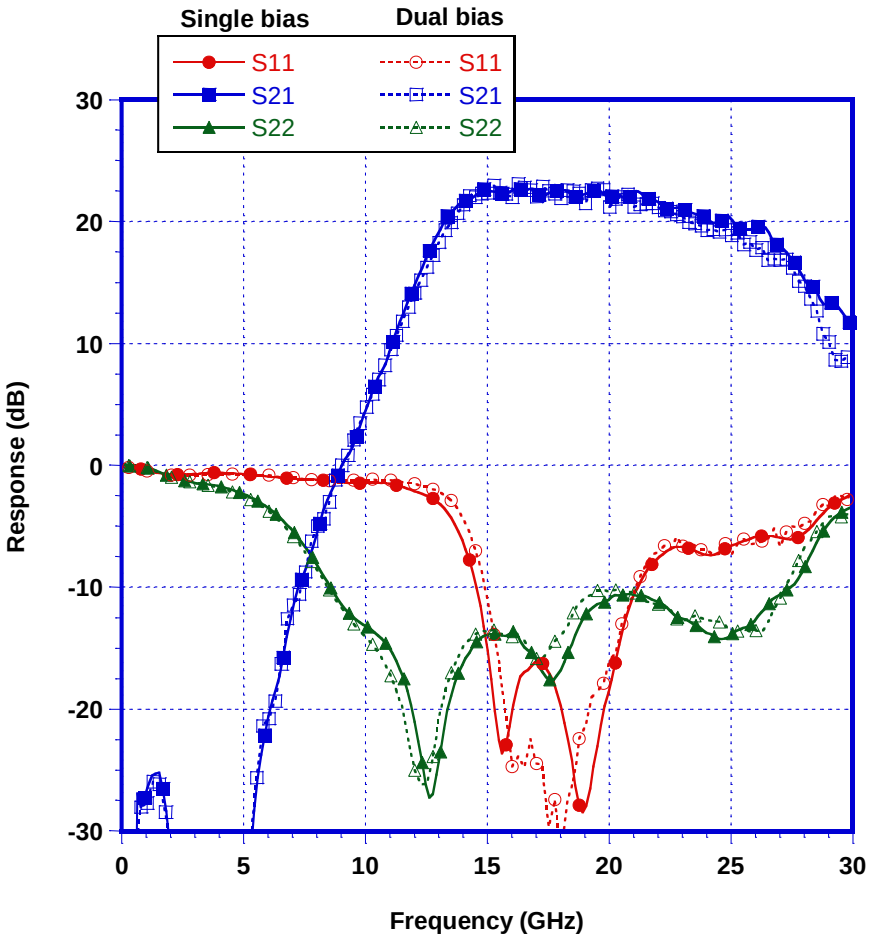

Figure 3. Comparison of the S-parameters for the CMD163C4 using the single and dual bias schemes. Vdd = 4 V, Vgg = 3 V.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

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