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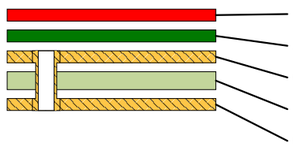
## LAYER STACK LEGEND



| Material | Layer | Thickness | Dielectric Material | Type | Comment |
|---|---|---|---|---|---|
| | Top Overlay | | | Legend | HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK. |
| Surface Material | Top Solder | 0.0004in | Solder Resist | Solder Mask | LPI (LIQUID PHOTO-IMAGEABLE) OR LDI (LASER DIRECT IMAGEABLE), GREEN. |
| **Copper** | **Top Layer** | **0.0014in** | | **Signal** | **FINISH THICKNESS = 0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH** |
| *Core* | | *0.0100in* | *RO4350* | *Dielectric* | |
| **Copper** | **Bottom Layer** | **0.0014in** | | **Signal** | **FINISH THICKNESS = 0.5oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH** |

**Total thickness: 0.0132in**

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS
   COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
   METAL1 (TOP) AND METAL2 (BOTTOM)
   GOLD PLATE PER MIL-G-45204, TYPE III, GRADE A, 5 TO 40 µin, OVER NICKEL PER QQ-N-290, 50 TO 100 µin.
4. CONTROLLED IMPEDANCE: TOP LAYER
   TRACE WIDTH: 0.015 GAP: 0.006
   REFERENCE PLANE: 2
5. FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) ±10%
6. COPPER IS PULLED BACK 0.003in. GROUND PLANE ONLY FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM). NO PULL BACK ON TAPER. THESE VALUES ARE CRITICAL AND MUST BE INSPECTED.
7. TOLERANCE: PC BOARD OUTLINE: ±0.005in.
8. BURRS SHALL NOT EXCEED 0.002in.
9. VIA PLATING/FILLING:
   A. ALL 0.012in VIAS ARE TO BE NON-CONDUCTIVE EPOXY FILLED, OVER-PLATED AND PLANARIZED.
   B. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.00075 ± 0.0004in. MIN. THICKNESS
10. METAL 1 (TOP) AND METAL 2 (BOTTOM) AFTER OVERPLATING AND PLANARIZATION SHALL HAVE A MAX ALLOWABLE NEGATIVE FEATURE OF 0.0008in. AND A MAX ALLOWABLE POSITIVE FEATURE OF 0.0003in.
11. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
12. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
13. ALL HOLES TO BE LOCATED WITHIN ±0.001 OF CAD DATABASE.
14. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
15. DELIVER BOARDS BAGGED AS: SINGLES
16. NO ELECTRICAL TEST NEEDED.

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

| | | | |
|---|---|---|---|
| UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES | SAP MATERIAL NUMBER: 300403 | | qorvo™ |
| TOLERANCES<br>.XX = ±.01<br>.XXX = ±.005<br>.XXXX = ±.0010<br>ANGLES = ± 0.5° | APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE | DATE | TITLE: QPL3050 EVALUATION PCB DESIGN PACKAGE |
| | DESIGNER J.CHAN | 3-2-2022 | |
| INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009 | ENGR. M.KELLY | | |
| | PDE CONTROLLED | | SIZE B · DOCUMENT NUMBER: QPL3050-4000 · PROTOTYPE INSTANCE: [2] · REV. 2 |
| THIRD ANGLE PROJECTION | CAGE CODE 1CVM1 | | SHEET 1 OF 6 · CAD: ALTIUM DESIGNER · SCALE: 2:1 |
| DO NOT SCALE DRAWING | | | Current Date & Time: 3/2/2022 2:34 PM |

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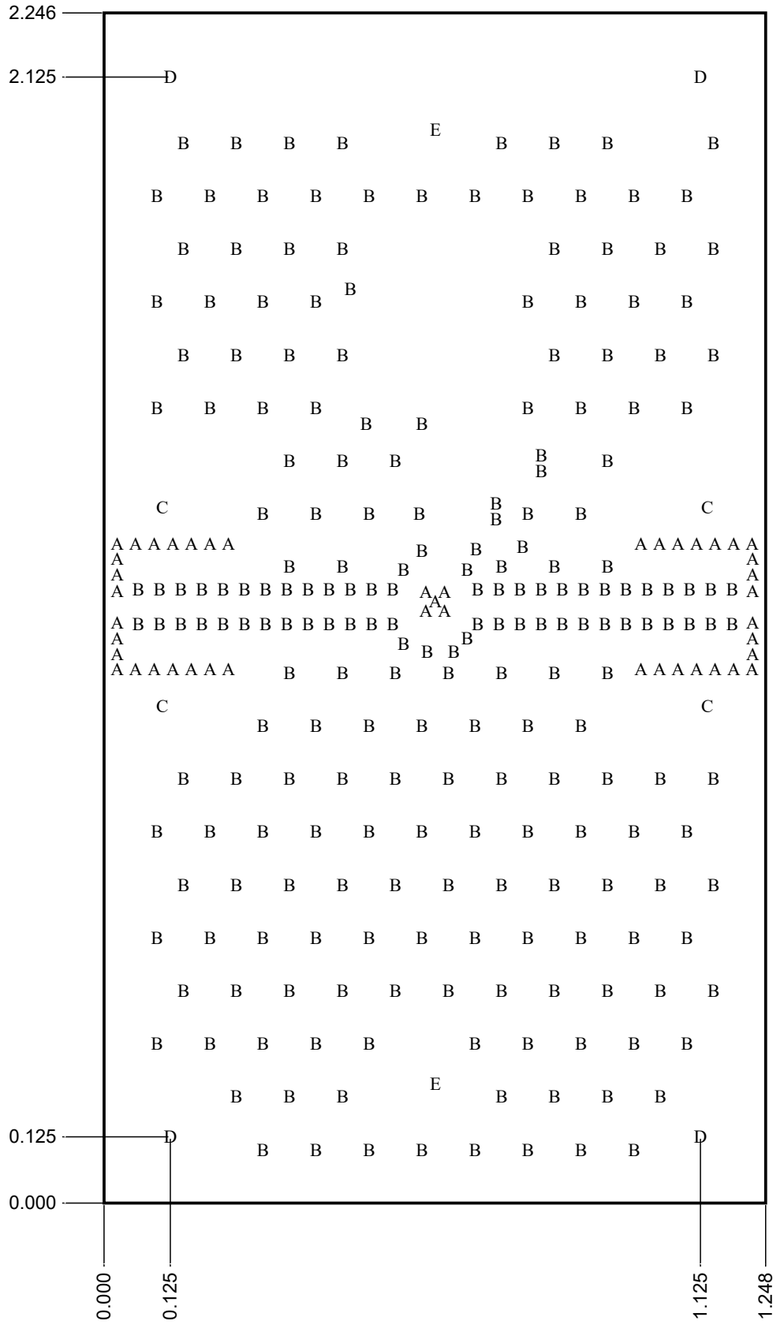


## Drill Table

| Symbol | Count | Hole Size | Plated | Drill Layer Pair |
|---|---|---|---|---|
| A | 45 | 0.012 | Plated | Top Layer - Bottom Layer |
| B | 228 | 0.015 | Plated | Top Layer - Bottom Layer |
| C | 4 | 0.086 | Plated | Top Layer - Bottom Layer |
| D | 4 | 0.100 | Plated | Top Layer - Bottom Layer |
| E | 2 | 0.120 | Plated | Top Layer - Bottom Layer |
| | 283 Total | | | |



| SIZE | CAGE CODE | DWG. NO. | PROTOTYPE INSTANCE: | REV. |
|---|---|---|---|---|
| B | 1CVM1 | QPL3050-4000 | [2] | 2 |

SHEET 2 OF 6 | CAD: ALTIUM DESIGNER | SCALE: 2:1

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FOR-001456 REV B

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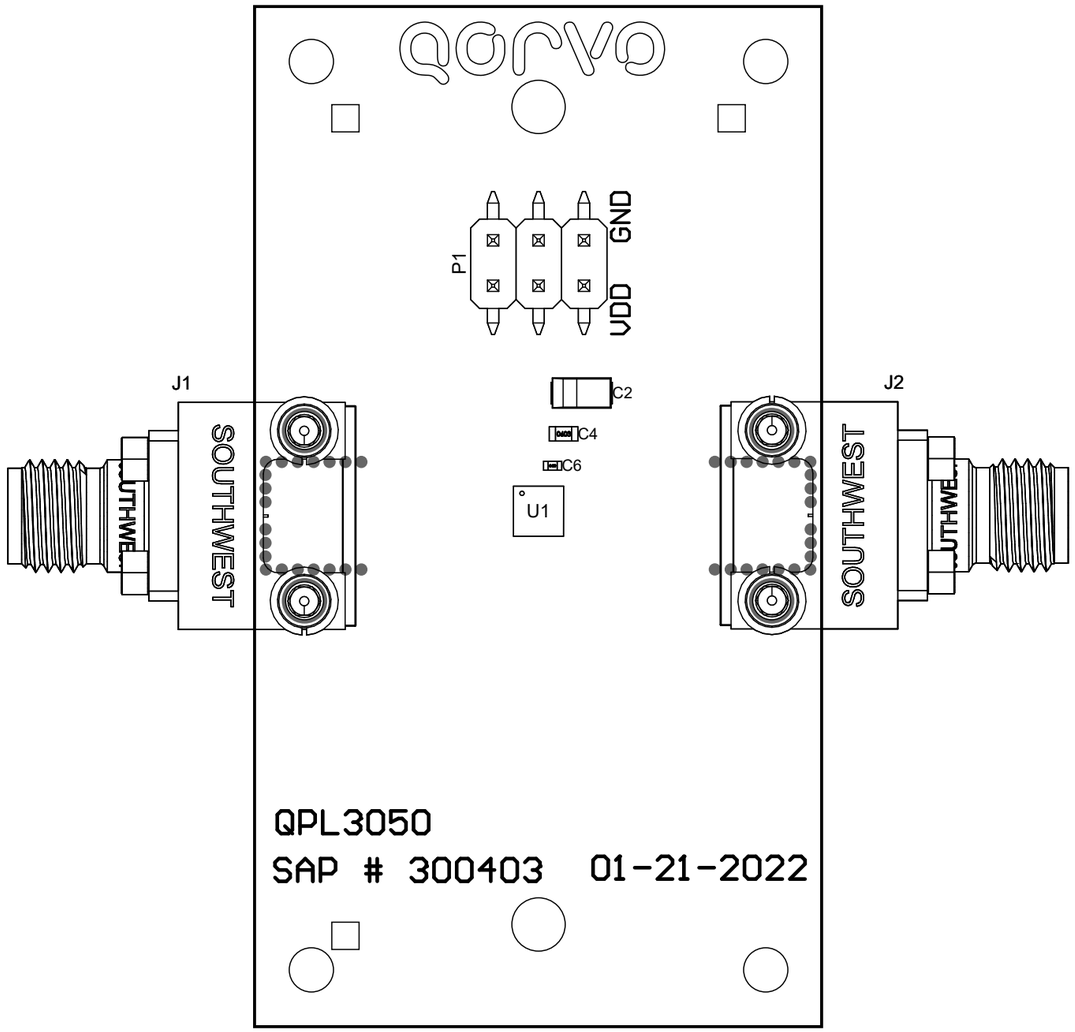
## ASSEMBLY NOTES:

17. WORKMANSHIP & SOLDER PER IPC-A-610C, CLASS 2.
18. PARTS WITH * FOLLOWING THE REFERENCE DESIGNATOR IN THE BOM ARE NOT TO BE POPULATED ON PCBA.
19. QORVO DEVICES (DUT) MAY REQUIRE BAKING PER IPC/JEDEC J-STD-020 FOR A MINIMUM OF 24 HOURS AT 125 +5/-0 DEGREES C. ASSEMBLY MUST TAKE PLACE WITHIN 12 HOURS OF BAKE COMPLETION.
20. MANUFACTURERS' PART NUMBERS ARE SUBJECT TO CHANGE BY THE MANUFACTURERS FOLLOWING THE ISSUE OF THIS DOCUMENT, AND ARE THEREBY INCLUDED FOR REFERENCE ONLY. CONTACT QORVO CORORATE ENGINEERING MATERIALS WITH QUESTIONS REGARDING SPECIFIC MANUFACTURERS' PART NUMBERS.
21. SHADED LINES ON THE BOM INDICATE APPROVED ALTERNATE COMPONENTS.
22. SMA CONNECTORS ARE MOUNTED ON BOTTOM SIDE OF BOARD. SMB'S ARE MOUNTED ON TOP SIDE OF BOARD.
23. TAKE CARE NOT TO ADD TOO MUCH SOLDER WHEN ASSEMBLING J1 AND J2 (IF PRESENT).

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| | DESIGNER | J.CHAN | 3-2-2022 |
| | ENGR. | M.KELLY | |
| INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009 | PDE CONTROLLED | | |
| THIRD ANGLE PROJECTION | CAGE CODE | 1CVM1 | |
| DO NOT SCALE DRAWING | | | |

| EAR | WARNING - THIS DOCUMENT CONTAINS TECHNICAL DATA WHOSE EXPORT IS UNDER CONTROL OF THE UNITED STATES DEPARTMENT OF COMMERCE UNDER THE EXPORT ADMINISTRATION REGULATIONS (15 CFR 730-774). DIVERSION CONTRARY TO U.S. LAW IS PROHIBITED. INFORMATION AND GUIDANCE ON EXPORT CONTROL REQUIREMENTS CAN BE FOUND AT www.BIS.doc.GOV |
|---|---|

qorvo™

TITLE:
# QPL3050 EVALUATION PCB DESIGN PACKAGE

| SIZE | DOCUMENT NUMBER: | PROTOTYPE INSTANCE: | REV. |
|---|---|---|---|
| B | QPL3050-4000 | [2] | 2 |

| SHEET 3 OF 6 | CAD: ALTIUM DESIGNER | SCALE: 2:1 |
|---|---|---|

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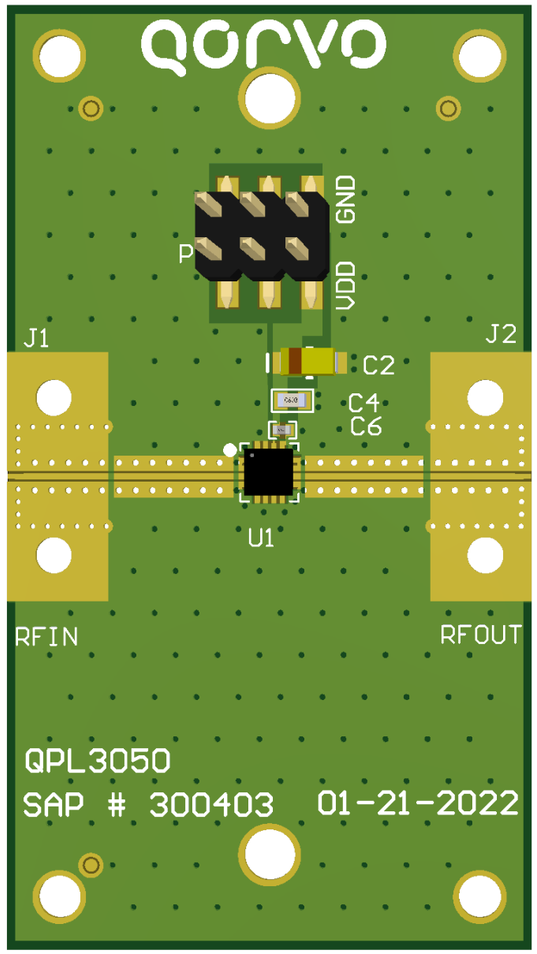
FOR-001456 REV B

# TOP VIEW (POPULATED)




| | | | | | | |
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| | | SHEET 4 OF 6 | CAD: ALTIUM DESIGNER | | SCALE: 2:1 | |

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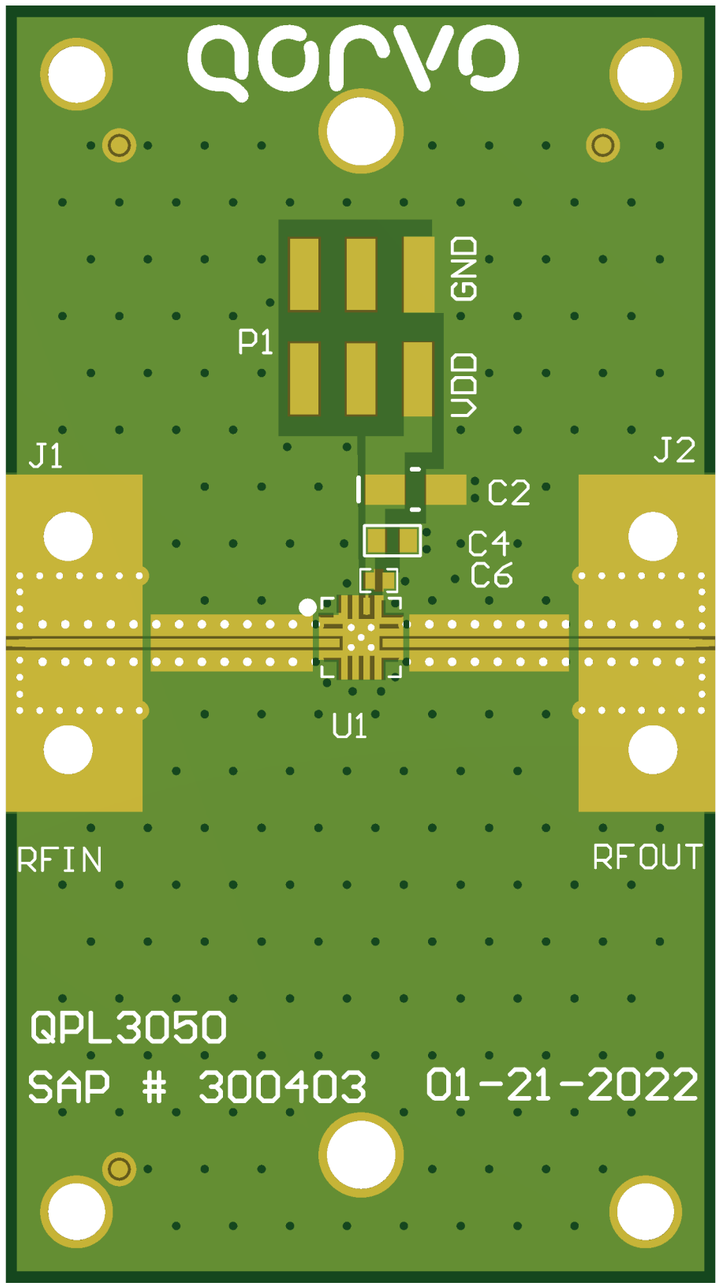
FOR-001456 REV B

## TOP VIEW




| | | | | | | |
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| | | SHEET 5 OF 6 | CAD: ALTIUM DESIGNER | | SCALE: 2:1 | |

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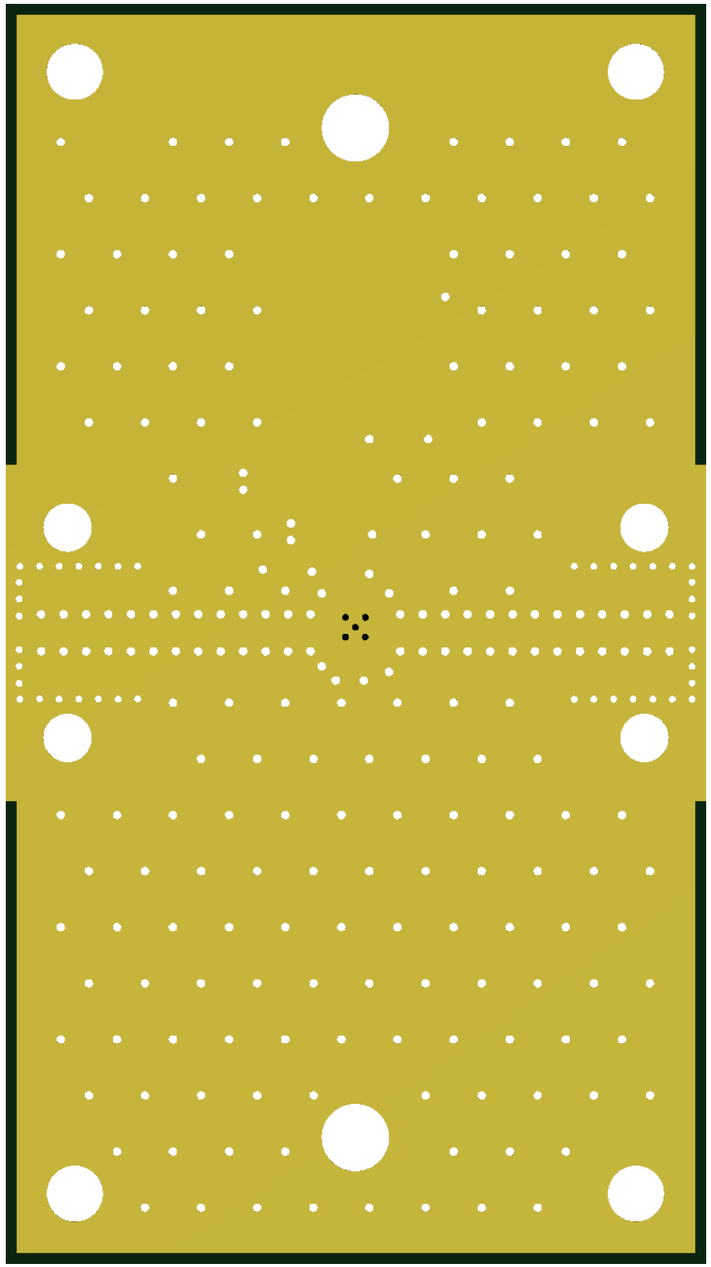
FOR-001456 REV B

# BOTTOM VIEW



| | | | | | | | |
|---|---|---|---|---|---|---|---|
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| | | SHEET 6 OF 6 | CAD: ALTIUM DESIGNER | | SCALE: 2:1 | | |

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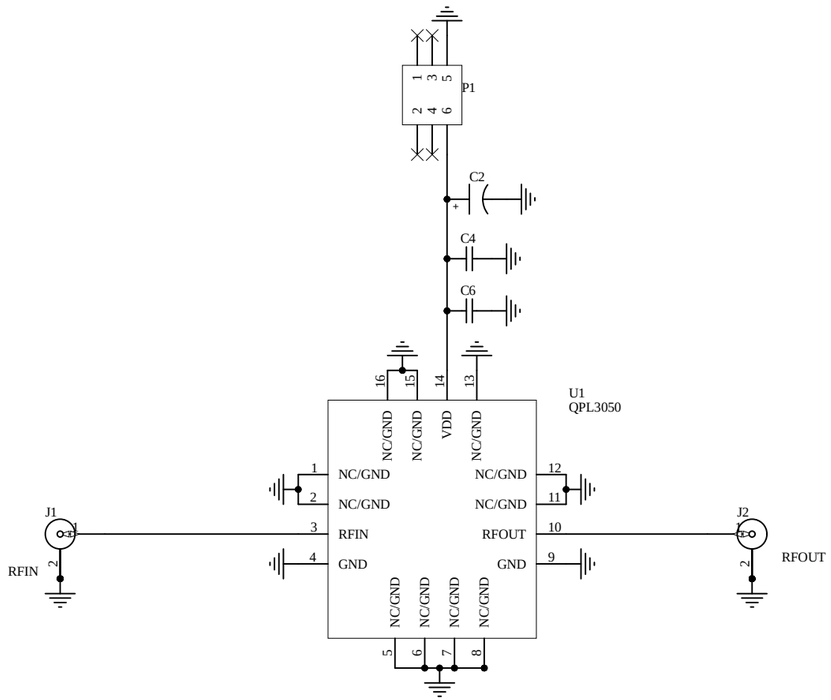
FOR-001456 REV B

| REVISION HISTORY | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVAL |
| 2 | INITIAL RELEASE | 3-2-2021 | M.KELLY |

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FD1 FIDUCIAL_30

FD2 FIDUCIAL_30

FD3 FIDUCIAL_30

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PDE CONTROLLED

CAGE CODE 1CVM1

SAP MATERIAL NUMBER: 300403

| APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE | | DATE |
|---|---|---|
| DESIGNER | J.CHAN | 3-2-2021 |
| ENGR. | M.KELLY | |

TITLE: QPL3050 EVALUATION PCB DESIGN PACKAGE

| SIZE | DOCUMENT NUMBER: | PROTOTYPE INSTANCE: | REV. |
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| B | QPL3050-4000 | [2] | 2 |

SCALE: NTS

SHEET 1 OF 1

FOR-001456 REV B