






SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD
SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

Layer Stack Legend

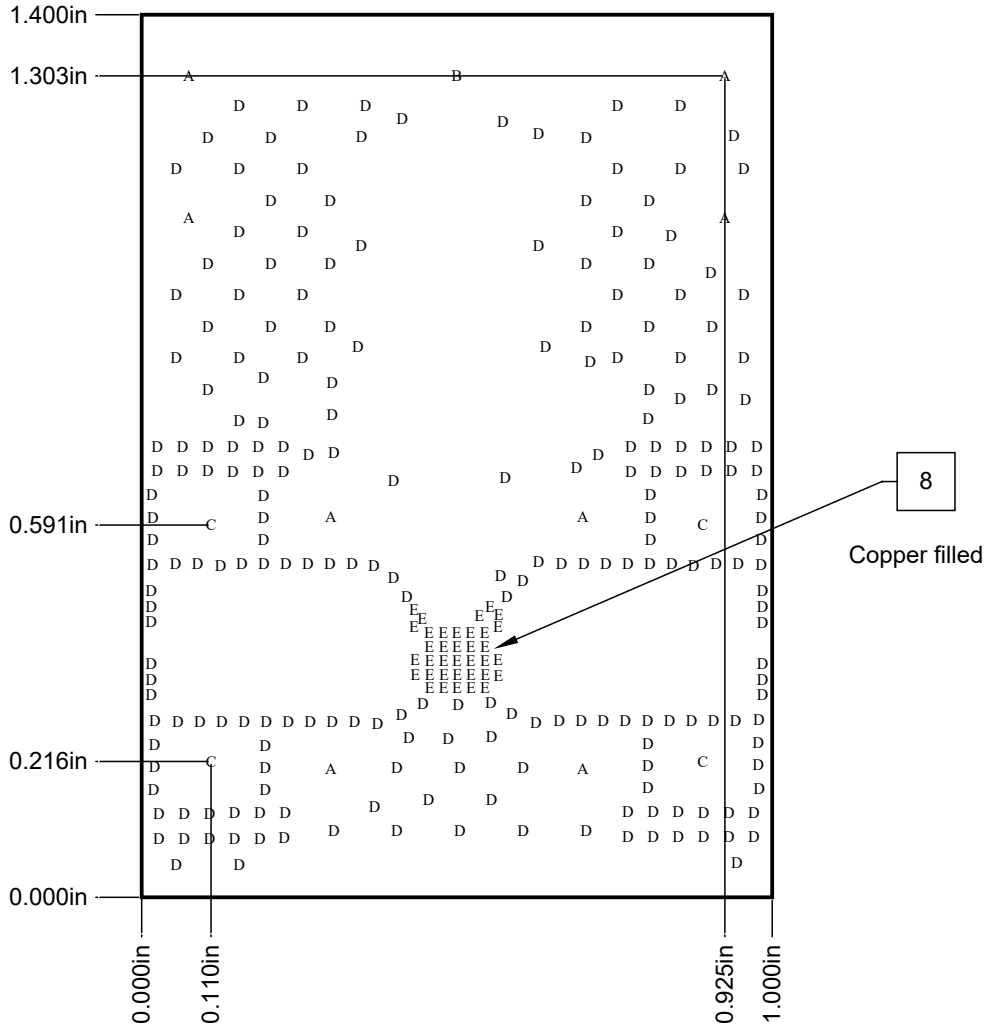
| Material | Layer | Thickness | Dielectric Material | Type | Note |
|---|---------------------------------|-----------|---------------------|-------------|---|
|  | SILKSCREEN_TOP | | | Legend | HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK. |
|  | Surface Material SOLDERMASK_TOP | 0.0000in | Solder Resist | Solder Mask | LPI (LIQUID PHOTO-IMAGEABLE), OR LDI (LASER DIRECT IMAGEABLE), GREEN. MAX FINISH THICKNESS TO BE 0.001in. |
|  | Copper METAL1_TOP | 0.0018in | | Signal | FINISH THICKNESS (STARTING BOARD MATERIAL : 0.5oz. COPPER) |
|  | Core | 0.0080in | R4003C | Dielectric | |
|  | Copper METAL2_BOTTOM | 0.0018in | | Signal | FINISH THICKNESS (STARTING BOARD MATERIAL : 0.5oz. COPPER) |
| Total thickness: 0.0116in | | | | | |

Drill Table


| Symbol | Count | Hole Size | Hole Tolerance | Plated | Drill Layer Pair |
|--------|-----------|-----------|---------------------|--------|----------------------------|
| E | 36 | 0.0079in | +0.0004in/-0.0080in | Plated | METAL1_TOP - METAL2_BOTTOM |
| D | 228 | 0.0149in | +0.0004in/-0.0150in | Plated | METAL1_TOP - METAL2_BOTTOM |
| C | 4 | 0.0950in | +/-0.0030in | Plated | METAL1_TOP - METAL2_BOTTOM |
| A | 8 | 0.1000in | +/-0.0030in | Plated | METAL1_TOP - METAL2_BOTTOM |
| B | 1 | 0.1200in | +/-0.0030in | Plated | METAL1_TOP - METAL2_BOTTOM |
| | 277 Total | | | | |

NOTES (UNLESS OTHERWISE SPECIFIED):

- BOARD FABRICATION METHODS MUST COMPLY WITH: FABRICATE BOARD PER PCI-6018 CLASS 2 IAW IPC-6011.
- ARTWORK FORMAT: GERBER 274X
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
- FINISH PLATING:
METAL 1(TOP) AND METAL 2(BOTTOM):
ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
ELECTROLESS NICKEL per IPC-4552, 118 - 236µin. (3 - 6µm)
IMMERSION GOLD per IPC-4552, 3 - 10 µin (0.08 - 0.25µm)
- FINISHED BOARD THICKNESS: (SEE LAYER STACKUP) ±10%
- GROUND PLANE COPPER FROM EDGE OF BOARD METAL 1 (TOP) AND METAL 2 (BOTTOM) IS PULLED BACK ACCORDING TO THE DATA. NO PULL BACK ON TAPER. THESE VALUES ARE CRITICAL AND MUST BE INSPECTED.
- TOLERANCE: PC BOARD OUTLINE: ±0.002in.
- BURRS SHALL NOT EXCEED 0.002in.
- VIA PLATING/FILLING:
A. ALL 7.9 MIL (E) VIAS UNDER THE DUT ARE TO BE COPPER-FILLED, OVER-PLATED AND PLANARIZED. FINISHED COPPER THICKNESS TO BE 0.0018 ±0.0004in.
B. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
- METAL 1(TOP) AND METAL2(BOTTOM) AFTER OVERPLATING AND PLANARIZATION SHALL HAVE A MAX ALLOWABLE NEGATIVE FEATURE OF 0.0008in. AND A MAX ALLOWABLE POSITIVE FEATURE OF 0.0003in.
- CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.003in. OF CAD DATABASE.
- SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
- ALL HOLES TO BE LOCATED WITHIN ±0.001 OF CAD DATABASE.
- NO VENDOR MARKING OR SERIALIZATION ALLOWED.
- DELIVER BOARDS BAGGED AS: SINGLES
- NO ELECTRICAL TEST NEEDED.



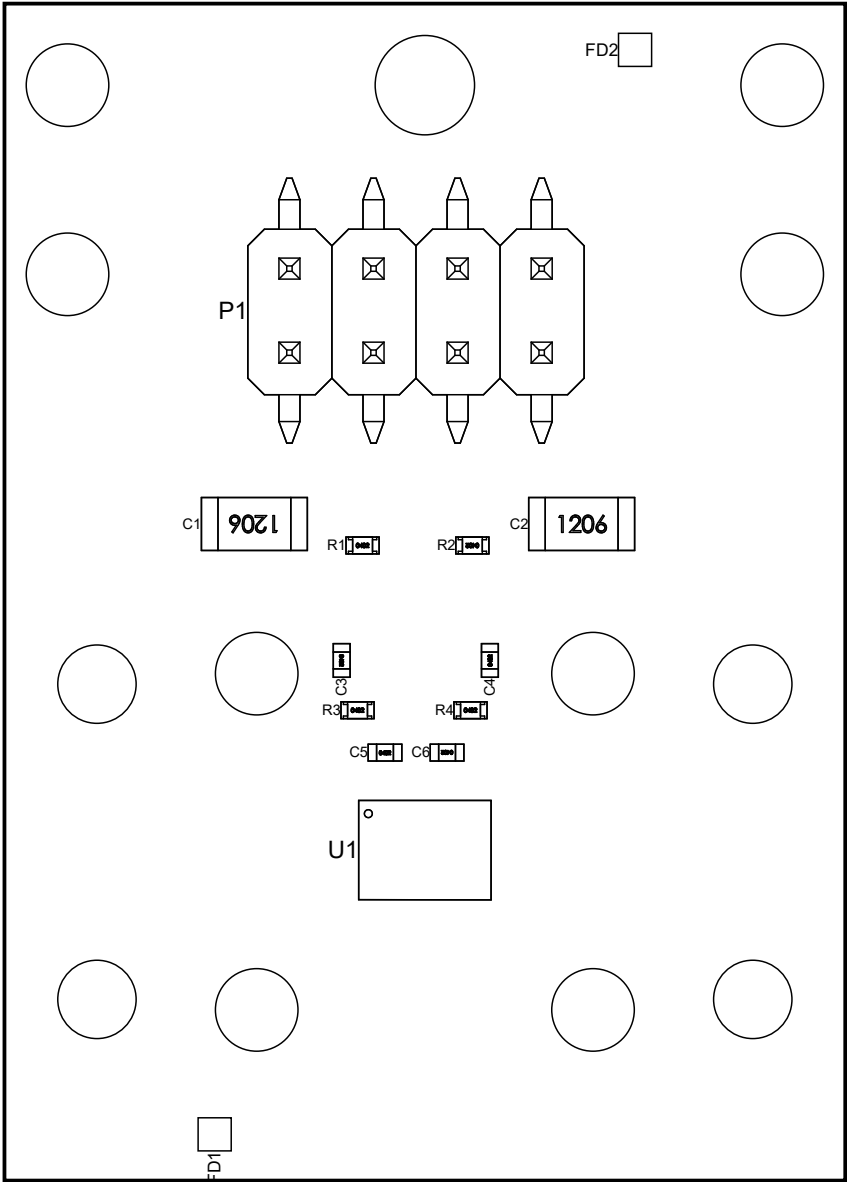
* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

| | | | | | | | | | | | |
|-----|--|---|--|----------------|-------|--------------|----------------------------------|----------------------------|-----------|------------|--|
| EAR | WARNING - THIS DOCUMENT CONTAINS TECHNICAL DATA WHOSE EXPORT IS UNDER CONTROL OF THE UNITED STATES DEPARTMENT OF COMMERCE UNDER THE EXPORT ADMINISTRATION REGULATIONS (15 CFR 730-774). DIVERSION CONTRARY TO U.S. LAW IS PROHIBITED. INFORMATION AND GUIDANCE ON EXPORT CONTROL REQUIREMENTS CAN BE FOUND AT www.BIS.doc.GOV |  | | PDE CONTROLLED | | SIZE B | DOCUMENT NUMBER: QPA0014-4000 | PROTOTYPE INSTANCE: [2] | REV. 1 | | |
| | | THIRD ANGLE PROJECTION | | CAGE CODE | 1CVM1 | SHEET 1 OF 5 | | CAD: ALTIUM DESIGNER | | SCALE: 2:1 | |
| | | DO NOT SCALE DRAWING | | | | | | | | | |
| | | | | | | | | | | | |
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ASSEMBLY NOTES:

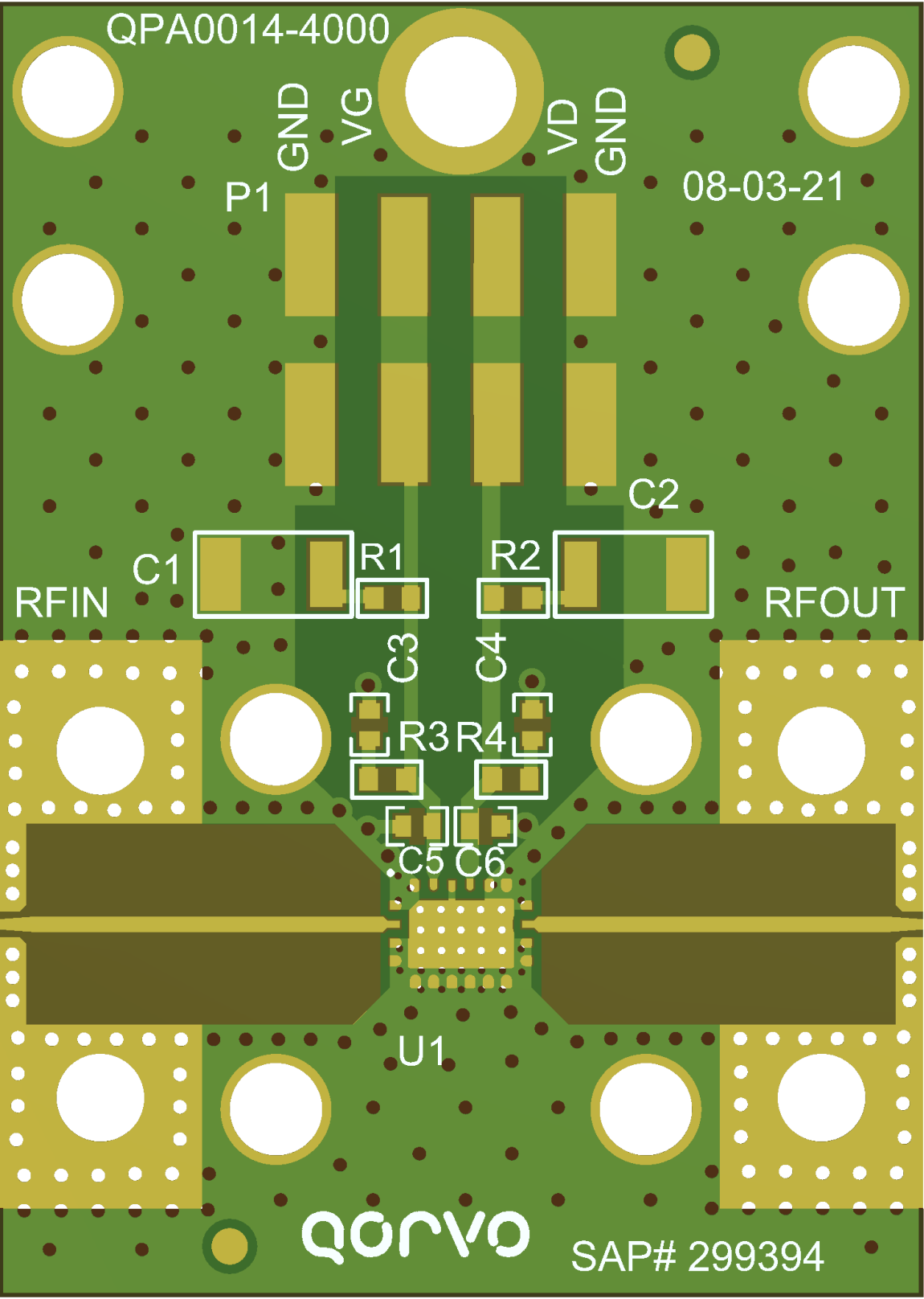
- 16. WORKMANSHIP & SOLDER PER IPC-A-610C, CLASS 2.
- 17. PARTS WITH * FOLLOWING THE REFERENCE DESIGNATOR IN THE BOM ARE NOT TO BE POPULATED ON PCBA.
- 18. QORVO DEVICES (DUT) MAY REQUIRE BAKING PER IPC/JEDEC J-STD-020 FOR A MINIMUM OF 24 HOURS AT 125 +5/-0 DEGREES C. ASSEMBLY MUST TAKE PLACE WITHIN 12 HOURS OF BAKE COMPLETION.
- 19. MANUFACTURERS' PART NUMBERS ARE SUBJECT TO CHANGE BY THE MANUFACTURERS FOLLOWING THE ISSUE OF THIS DOCUMENT, AND ARE THEREBY INCLUDED FOR REFERENCE ONLY. CONTACT QORVO CORORATE ENGINEERING MATERIALS WITH QUESTIONS REGARDING SPECIFIC MANUFACTURERS' PART NUMBERS.
- 20. SHADED LINES ON THE BOM INDICATE APPROVED ALTERNATE COMPONENTS.
- 21. SMA CONNECTORS ARE MOUNTED ON BOTTOM SIDE OF BOARD. SMB'S ARE MOUNTED ON TOP SIDE OF BOARD.
- 22. TAKE CARE NOT TO ADD TOO MUCH SOLDER WHEN ASSEMBLING J1 AND J2 (IF PRESENT).



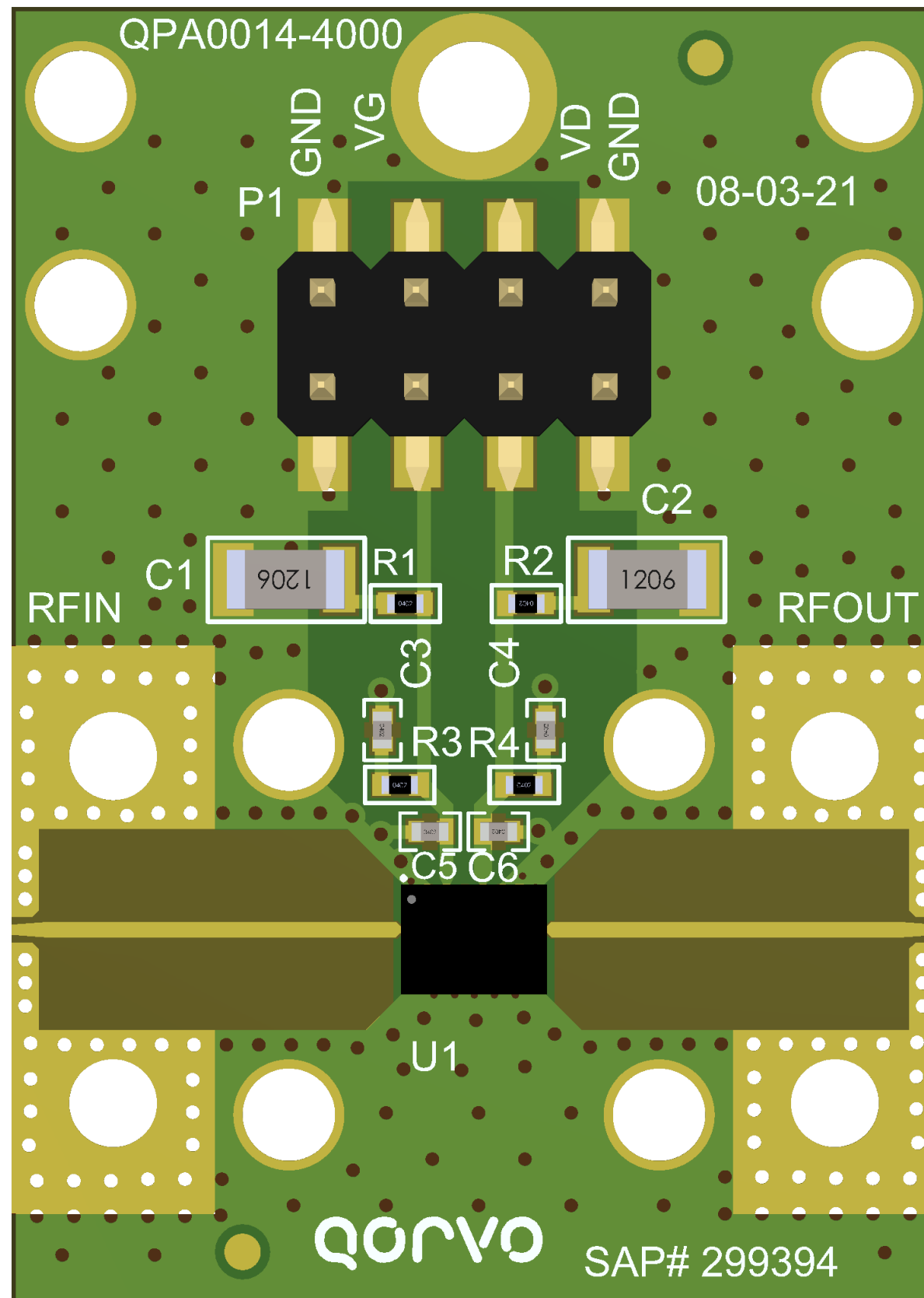
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| | | | | CAGE CODE | 1CVM1 | B | QPA0014-4000 | | [2] | 1 | |
| | | THIRD ANGLE PROJECTION | | | | | | | | | |
| | | DO NOT SCALE DRAWING | | | | SHEET 2 OF 5 | | | | | CAD: ALTIUM DESIGNER |

TOP VIEW



TOP VIEW (POPULATED)



B

B

A

A

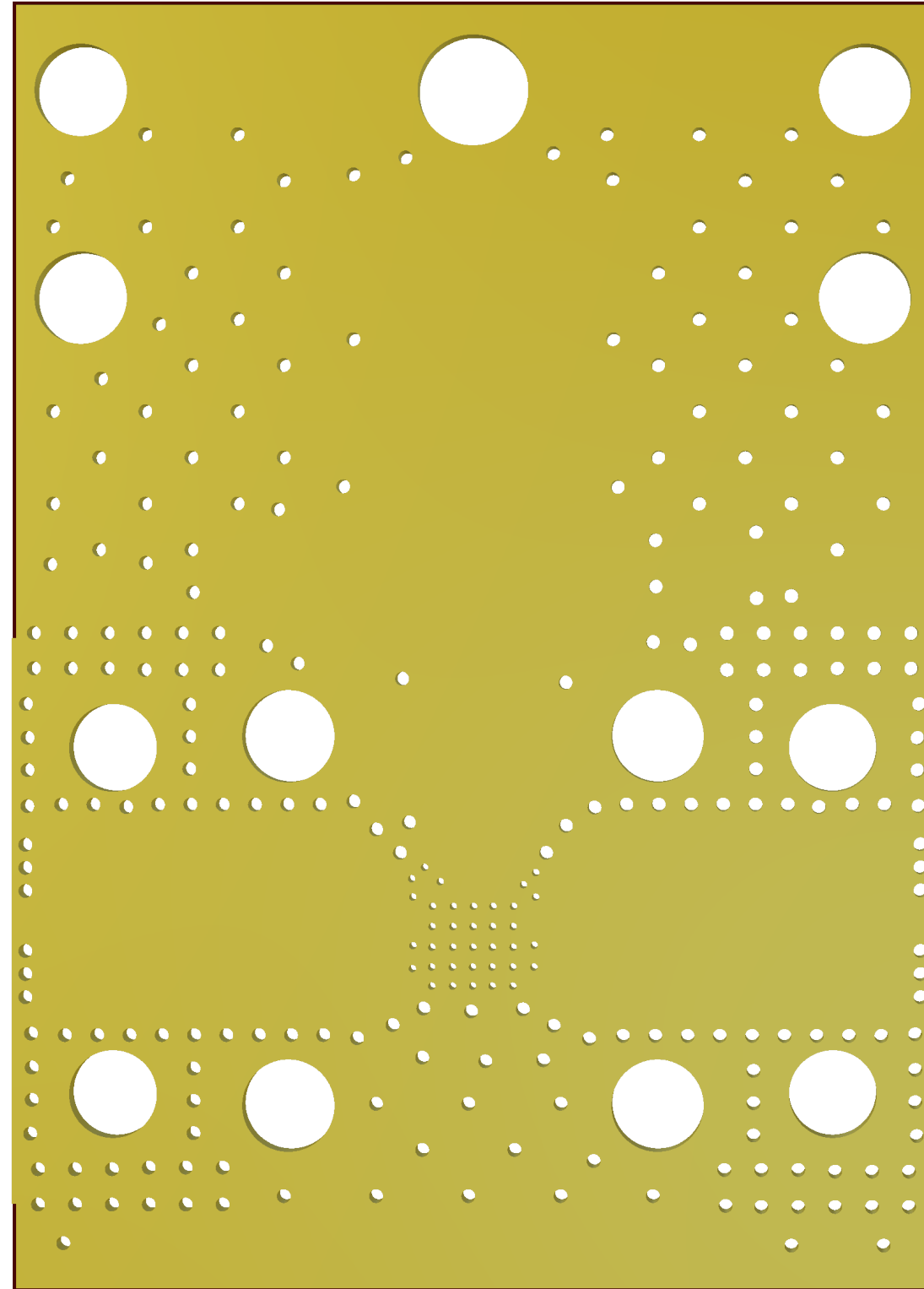
4

3

2

1

BOTTOM VIEW



B

B

A

A

4

3

2

1

