



*Power Application Controller Battery Management*  
*PRODUCT USER GUIDE*

# PAC2514x User Guide Preview

*PAC Battery Management System*

Multi-Mode Power Manager™  
Configurable Analog Front End™  
Application Specific Power Drivers™  
Arm® Cortex®-M4F Controller Core





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## PAC2514x Users Guide Preview

### 1 OVERVIEW

This document is the PAC2514x Device User Guide. It details the operation of the analog peripherals in the PAC25140, PAC25140N, PAC25141N.

For detailed information on the MCU and Digital Peripherals in the PAC2514x, see the [PAC55XX Family User Guide](#).

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## 2 STYLE AND FORMATTING CONVENTIONS

This chapter describes the formatting and styles used throughout this document.

### 2.1 Number Representation

Numbers other than decimal will have a postfix indicator. All numbers use little endian formatting, with the most significant bit/digit to the left. Digits for binary and hexadecimal representation are grouped with a single space every four digits to improve readability. Binary numbers use “b” as a postfix and hexadecimal numbers use “h” as a postfix.

For example, 1011b binary = Bh hexadecimal = 11 decimal.

### 2.2 Formatting Styles

TYPE	EXAMPLE	DESCRIPTION
Register Name	<b>RTCCTL</b>	Register names use a capital letter and <b>boldface</b> type.
Register Bit(s)	<b>RTCCTL.RTCCLKDIV</b>	Register bits are always represented with the register name separated with a period.
Function selected by register bit(s)	<b>[RTCCTL.RTCCLKDIV]</b>	Within text blocks, functions selected with a register bit setting are set in brackets. For example <b>[RTCCTL.RTCCLKDIV]</b> means divider settings /2 to /65536.
Pin Function	PA5	Pin functions use capital letters
Internal signals	<i>PWMA3</i>	Internal signals use <i>italicized</i> font.
Formulas	CLK = FCLK / DIV	Formulas use <code>monospaced text</code> .
Links	<a href="#">Link</a>	Hyperlinks are <u>underlined and blue</u> .
CPU Mnemonic	MRS	CPU Mnemonic uses <code>monospaced text</code> .
Operands	{ <i>Rd</i> , }, <i>Rn</i> , <i>Rm</i>	Operands use <i>monospaced italic text</i> .
Code examples	b loopA	Code examples use <code>monospaced text</code> .

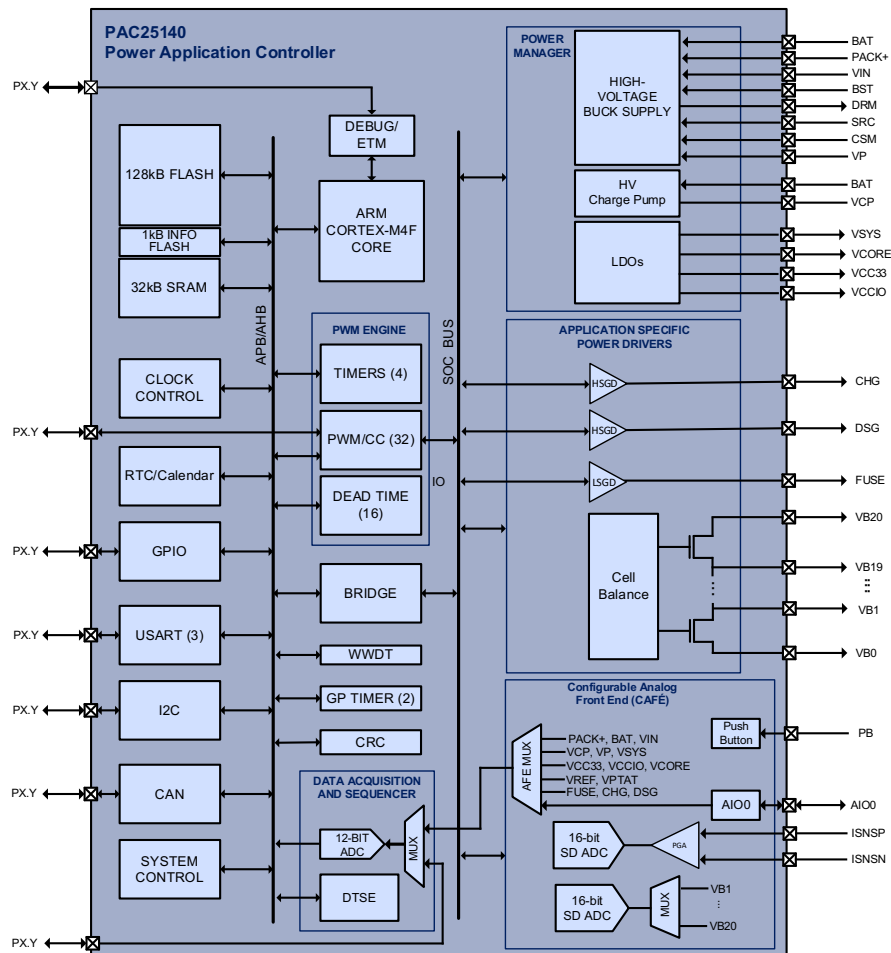
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### 3 ARCHITECTURAL BLOCK DIAGRAM

For Below is an architecture block diagram of the PAC2514X device.

Figure 3-1 PAC2514X Architectural Block Diagram



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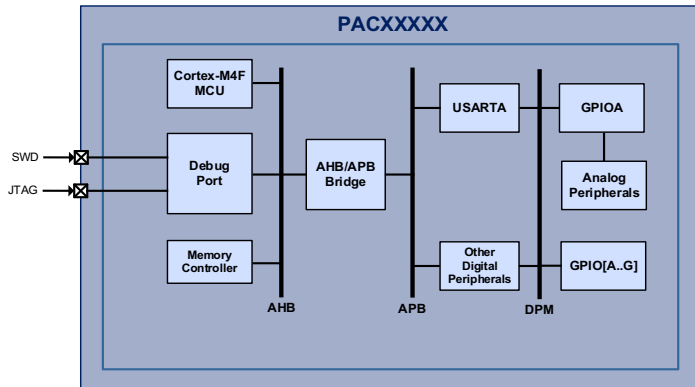
## 4 ANALOG REGISTER ACCESS

### 4.1 Overview

All analog registers in the PAC2514X are accessible through a SOC bus in the device. Unlike registers in the MCU (SRAM and digital peripheral registers), these analog registers are not memory mapped.

The block diagram below shows the different system busses that the MCU uses to access the different system registers.

Figure 4-1 PAC2514X Register Access



The PAC2514X contains two register buses: the AHB bus and the APB bus.

The AHB bus allows the MCU and Debug Port access to FLASH and SRAM via the Memory Controller. To access other digital peripheral connected to the APB bus, there is a bridge from the AHB to the APB bus so that the MCU or Debug Port can perform memory-mapped register access to all digital peripherals. Some digital peripherals such as timers are flexibly connected to IO using the DPM bus.

To access the Analog peripherals, the USARTA SPI peripheral is used to generate read and write transactions to the Analog registers using the DPM and GPIOA.

### 4.2 Functional Description

External programming interfaces such as JTAG and SWD or the Arm® Cortex®-M4F MCU may perform memory-mapped accesses to USART A through the AHB and APB busses on the device.

USART A is a serial communication peripheral that supports a SPI-like protocol that can be used to communicate to the Analog Peripherals for read and write transactions. The Digital

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Peripheral MUX (DPM) may be configured to connect the USART A SPI signals to GPIO A, where they are connected to the Analog peripherals.

### 4.3 USART Configuration

USART A acts as a SPI bus master to communicate with the Analog Peripherals. The USART A signals that are used for this communication are:

- *USASCLK* – USART A SPI Clock
- *USAMOSI* – USART A Master-Out/Slave-In
- *USAMISO* – USART A Master-In/Slave-Out
- *USASS* – USART A Slave Select

In order to communicate with the Analog Peripherals, the USART A should have the following configuration:

- 8-bit mode
- SCLK active high
- CPH is sample/setup
- SS active low

When communicating with the Analog Peripherals, the maximum SCLK frequency is 25MHz.

### 4.4 Protocol

The protocol for communicating with the Analog Peripherals is a simple two-byte protocol.

The first byte is always the address, which includes a 7-bit address [7:1] and a write bit [0]. For write operations, the write bit [0] is set to 1b. For read operations, the write bit [0] is set to 0b.

For write operations, the 2<sup>nd</sup> byte will be the 8-bit data to write to the given address.

For read operations, the 2<sup>nd</sup> byte is ignored and MISO will contain the 8-bit data read from the given address.

### 4.5 Write Register Example

To write the **HPDACH** register (address 11h) with the value 28h, issue the following transactions to USART A:

- Write **SSPADAT** with the value 23h (11h << 1 | 1b for write transaction)
- Write **SSPADAT** with the value 28h

The timing diagram from a write operation is shown below.

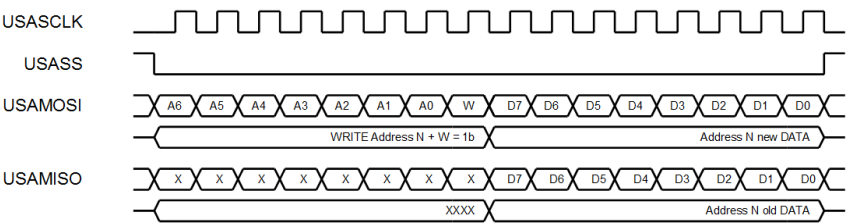
Figure 4-2 Analog Peripheral Register Write Timing

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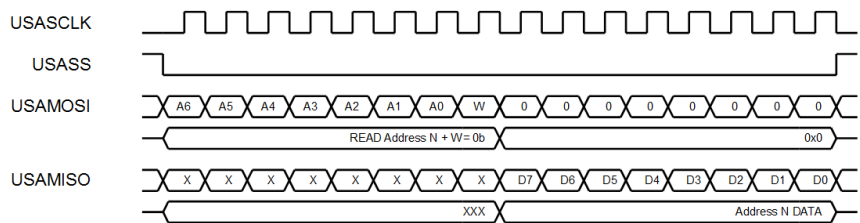
4.6 Read Register Example

To read the contents of the **HPDACH** register, issue the following transactions to USART A:

- Write **SSPADAT** with the value 22h (11h << 1 | 0b for read transaction)
- Write **SSPADAT** with a dummy character
- Read last data from MISO from **SSPADAT**, this is the register value

The timing diagram from a read operation is shown below.

Figure 4-3 Analog Peripheral Register Read Timing



For more information on how to configure the DPM to support the USART A peripheral for communicating with the Analog Registers, see the PAC55XX Family User Guide.

## 5 PAC2514X IO

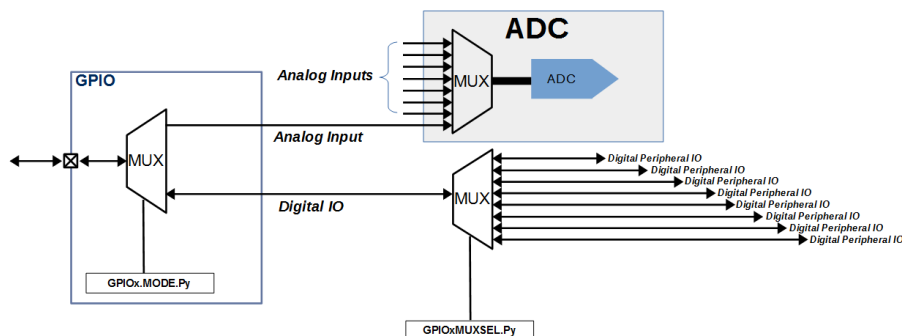
### 5.1 Overview

The Digital Peripheral MUX (DPM) on the PAC55XX family allows flexible assignment of peripheral functions to IO pins.

Each member of the family has a different set of IO pins that are available. It is important during application design that the designer consider the available IO pins to make sure the necessary peripherals will be available.

Below is a diagram of the GPIO and MUX structure.

Figure 5-1 GPIO and DPM Block Diagram



Each IO can be configured to select 1 of up to 8 digital peripheral signals. Some IOs also may be used as an ADC input. For information on how to configure the IO for each of these situations, see the PAC55XX Family User Guide.



## 5.2 ADC Channels

The ADC channels that are available on the PAC2514X are shown in the table below.

Table 5-1 PAC2514X ADC Input Pins

ADC Channel	MCU I/O PIN	Description
AD0	PG7	Internally Connected to AFE MUX
AD1	PD3,PG5	Package pin
AD2	PD2,PG6	Package pin
AD3	PD1	Package pin
AD4	PD0,PF4	Package pin
AD5	PF5	Package pin
AD6	PF6	Package pin
AD7	PF7	Package pin

Table 5-2 PAC2514X Internal Connections

AFE Function	MCU I/O PIN	Description
ICBCTL0	PB0	DSG Control Line
ICBCTL1	PB1	CHG Control Line
IADCBUSY	PB3	Current ADC Busy
VADCBUSY	PB4	Voltage ADC Busy
PBPT	PG6	Push Button
ADCIN	PG7	EMUX output Analog Signal input to MCU ADC
nIRQ1	PA7	Interrupt for Temperature Faults
nIRQ2	PA0	Interrupt for Current Faults and BATOV
MUXDATA	PA1	EMUX Setting
MUXCLK	PA2	EMUX Clock to load setting
SPICLK	PA3	SPI Clock
SPIMOSI	PA4	SPI MOSI
SPIMISO	PA5	SPI MISO
SPICS	PA6	SPI Chip Select

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### 5.3 Digital Peripheral Pins

The digital peripheral functions that are available in the PAC2514X are shown below.

Table 5-3 PAC2514X Digital Peripheral Pins

PORT	Pin	GPIOxMUXS.Py							
		000b	001b	010b	011b	100b	101b	110b	111b
GPIOA	P0	GPIOA0							
	P1	GPIOA1	EMUXD						
	P2	GPIOA2	EMUXC						
	P3	GPIOA3	USASCLK	USBCLK					
	P4	GPIOA4	USAMOSI	USBMOSI					
	P5	GPIOA5	USAMISO	USBMISO					
	P6	GPIOA6	USASS	USBSS					
	P7	GPIOA7							
GPIOB	P0	GPIOB0	TAPWM0	TBPWM0					
	P1	GPIOB1	TAPWM1	TBPWM1					
	P2	GPIOB2	TAPWM2	TBPWM2					
	P4	GPIOB4	TAPWM4	TBPWM4					
	P5	GPIOB5	TAPWM5	TBPWM5					
	P6	GPIOB6	TAPWM6	TBPWM6					
GPIOC	P4	GPIOC4	TBPWM4	TCPWM4	TCIDX	USBMOSI	USCSCLK	CANRXD	I2CSCL
	P5	GPIOC5	TBPWM5	TCPWM5	TCPHA	USBMISO	USCSS	CANTXD	I2CSDA
GIOD	P0	GIOD0	TBPWM0	TCPWM0	TDIDX		USCSCLK	CANTXD	EMUXD
	P1	GIOD1	TBPWM1	TCPWM1	TDPHA		USCSS	CANRXD	EMUXC
	P2	GIOD2	TBPWM2	TCPWM2	TDPHB		USCMOSI		
GPIOE	P0	GPIOE0	TCPWM4	TDPWM0	TAIDX	TBIDX	USCSCLK	I2CSCL	EMUXC
	P1	GPIOE1	TCPWM5	TDPWM1	TAPHA	TBPHA	USCSS	I2CSDA	EMUXD
	P2	GPIOE2	TCPWM6	TDPWM2	TAPHB	TBPHB	USCMOSI	CANRXD	EXTCLK
	P3	GPIOE3	TCPWM7	TDPWM3	FRCLK		USCMISO	CANTXD	
GPIOF	P0	GPIOF0	TCPWM0	TDPWM0	TMS/SWDCLK	TBIDX	USBCLK	TRACECLK	
	P1	GPIOF1	TCPWM1	TDPWM1	TMS/SWDIO	TBPHA	USBSS	TRACED0	
	P2	GPIOF2	TCPWM2	TDPWM2	TDI	TBPHB	USBMOSI	TRACED1	
	P3	GPIOF3	TCPWM3	TDPWM3	TDO	FRCLK	USBMISO	TRACED2	

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	P4	GPIOF4	TCPWM4	TDPWM4		TCIDX	USDCLK	TRACED3	EMUXC
	P5	GPIOF5	TCPWM5	TDPWM5		TCPHA	USDSS		EMUXD
	P6	GPIOF6	TCPWM6	TDPWM6		TCPHB	USDMOSI	CANRXD	I2CSCL

For more information on how to configure the DPM for the PAC2514X, see the PAC55XX Family User Guide.

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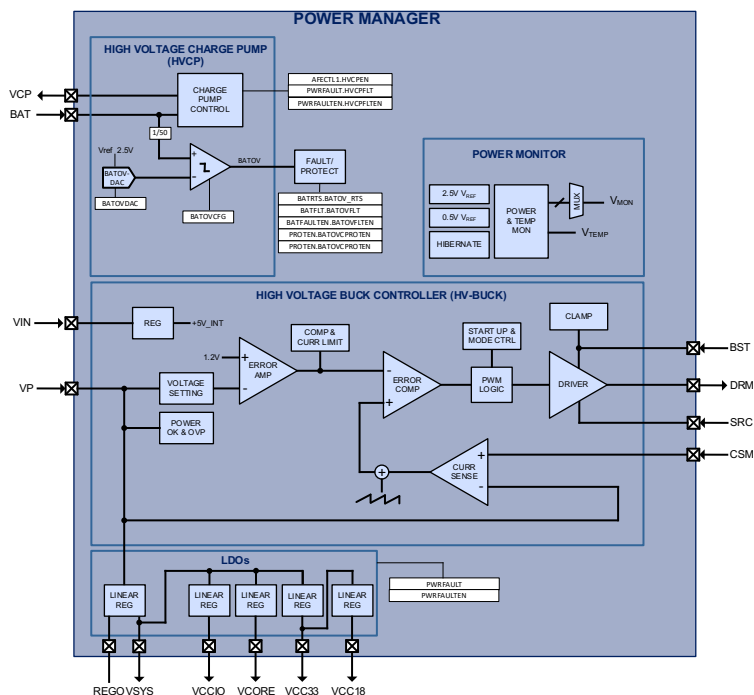
## 6 CONFIGURABLE POWER MANAGER

### 6.1 Features

- High Voltage BUCK
- High Voltage Charge Pump for CHG/DSG high-side gate driver supply
- 4 additional Linear regulators with power and hibernate management
- High-accuracy voltage reference for ADC and comparators
- Power and temperature monitor, warning, fault detection
- Extremely low hibernate mode IQ of 3 $\mu$ A at 80V

### 6.2 System Block Diagram

Figure 6-1 Power Manager System Block Diagram



### 6.3 Functional Description

The Configurable Power Manager (Figure 6-1) is optimized to efficiently provide “all-in-one” power management required by the PAC and associated application circuitry. It incorporates a

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high-voltage power supply controller that is used to convert power from a DC input source to generate a main supply output  $V_P$ . There are also linear regulators to provide  $V_{SYS}$ ,  $V_{CC33}$  and  $V_{CORE}$  supplies for 5V system, 3.3V mixed signal and micro-controller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

The three other linear regulators provide  $V_{CCIO}$ ,  $V_{CC33}$ ,  $V_{CC18}$  and  $V_{CORE}$  supplies for 3.3V I/O, 3.3V mixed signal, 1.8V analog and 1.9V microcontroller core circuitry. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

It incorporates a High-Voltage Charge Pump (HVCP) to efficiently convert power from the battery stack to generate a gate driver VCP.

### Hibernate Mode

Hibernate mode on the device allows a very low IQ mode when not in operation to minimize energy consumption when the motor is not running, and the battery pack need not provide power. See control registers in Register 8-6.

To enter hibernate mode, configure the SOC.HIBCTL register settings, and the set SOC.HIBENTER.HIB to 1b. This bit will be automatically cleared when exiting hibernate.

To wake-up from hibernate mode the user may either use the Hibernate Wake-up Timer, the Push-button function or PACK+ detection. Before entering hibernate mode, one of these methods should be configured.

### Push Button

Before entering hibernate mode by setting SOC.HIBENTER.HIB to 1b, the system could be configured to exit hibernate mode with a properly polarized push button assertion, by setting the SOC.HIBCTL.PBWAKEEN bit to 1d.

The Push Button wake up method is selected by configuring the SOC.HIBCTL.WAKESRC to 0d.

### Charger Pack+ Wake Up

Before entering hibernate mode by setting SOC.HIBENTER.HIB to 1b, the system could be configured to exit hibernation mode by detecting the moment in which the battery pack is connected to a charger, or a load, by setting the SOC.HIBCTL.HIB to 1b.

The Push Button wake up method is selected by configuring the SOC.HIBCTL.WAKESRC to 1d.

### Wake Up Timer

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Before entering hibernate mode by setting SOC.HIBENTER.HIB to 1b, the system could be configured to periodically exit hibernate mode by configuring the SOC. HIBCTL.WUTIMER from 0d to 7d. Refer to Section 34.1.6 for more information on available wake up timing periods. A configuration setting equal to 0d will in effect disable the Wake Up Timer. Settings from 1d to 7d will enable the Wake Up Timer with periods ranging from as low as 125 ms to as large as 8 seconds.

The Wake Up Timer method is selected by configuring the SOC. HIBCTL.WAKESRC to 2d.

### Power Manager Faults

The power manager monitors all of the power supplies and LDOs for faults during operation.

During a power management fault condition such as under-voltage or over-current each of the power supplies will set a fault bit and certain power supplies can be disabled as a result of the fault. The device may be reset and power rails restarted. To determine the fault condition, fault registers can be read. The corresponding fault bit(s) should be written to a 1b to clear the fault flag.

### Temperature Warnings and Faults

The PAC2514X has an integrated temperature sensor that is used for temperature warnings and faults and can also be sampled by the MCU ADC through the AFE MUX using the VPTAT MUX channel.

This value has a compensation coefficient available in INFO FLASH that can be used to obtain an accurate temperature. The parameter VT300K will be stored in INFO FLASH and will indicate the compensation factor.

The die temperature in degrees Kelvin can then be calculated by the following formula:

$$TKELVIN = 300 * (VPTAT + 0.075) / (VT300K + 0.075)$$

The PAC2514X contains two warning thresholds and one fault threshold:

- Warn 1: 120°C
- Warn 2: 140°C
- Fault: 155°C

If the internal temperature (VPTAT) rises above the Warn 1 threshold, the device will indicate this through a latched register bit. The user may enable a mask-able interrupt to the MCU to announce this condition.

If the internal temperature (VPTAT) rises above the Warn 2 threshold, the device will indicate this through a separate latched register bit. The user may enable an interrupt to the MCU to announce this condition. This will be the same interrupt as the Warn 1 threshold.

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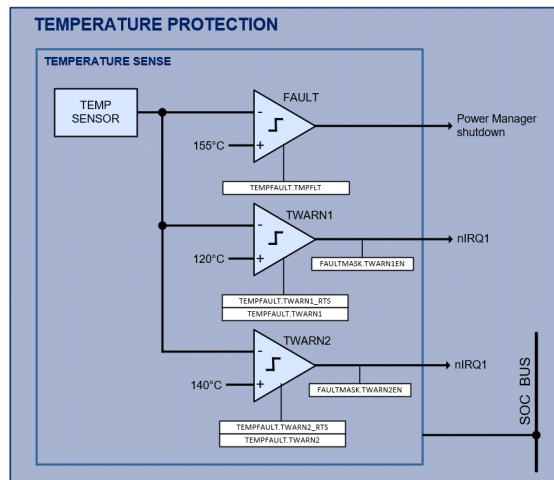


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If the internal temperature (VPTAT) rises above the Fault threshold, the Charge pump, DC/DC and gate drivers will be disabled. The device will indicate this through a latched register bit. There is not interrupt for this condition. When the device falls below the hysteresis value, then the DC/DC will be re-enabled.

The temperature hysteresis level for all three thresholds is 10°C.

Figure 6-2 Temperature Protection Block Diagram



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## 6.4 Register Summary

Table 6-1 CPM Register Summary

ADDRESS	REGISTER	DESCRIPTION	RESET
00h	<b>SOC.FAULT</b>	Fault condition indication register	00h
01h	<b>SOC.STATUS</b>	Hardware status condition register	00h
02h	<b>SOC.MISC</b>	Miscellaneous features register	00h
03h	<b>SOC.PWRCTL</b>	Power Manager control register	00h
04h	<b>SOC.FAULTENABLE</b>	Power Manager fault mask register	00h
05h	<b>SOC.WATCHDOG</b>	SOC Watchdog configuration register	00h
2Bh	<b>SOC.SYSCONF</b>	Power Manager system configuration register	0Ch

## 6.5 Register Details

### 6.5.1 SOC.FAULT

Register 6-1 SOC.FAULT (Fault Condition, 00h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	<b>TMPWARN</b>	R	0x0	Real-time temperature warning status. When the temperature is greater than the warning threshold, this bit is set to 1b. When the temperature less than the warning threshold, this bit is set to 0b.  0b: No temperature warning 1b: Temperature warning
6	<b>TMPWARN_LATCH</b>	R	0x0	Latched temperature warning status. If the temperature reaches the warning threshold and the <b>SOC.FAULTENABLE.nTMPWARN</b> is not masked, this bit is set and nIRQ1 is asserted.  Write 1b to clear when not masked.  0b: No temperature warning 1b: Temperature warning
5	<b>TMPFLT</b>	R	0x0	Temperature fault status. If the temperature reaches the fault threshold, this bit is set to 1b. Write 1b to clear.  0b: No temperature fault 1b: Temperature fault
4	<b>VPFLT</b>	R	0x0	DC/DC fault when VP is below UVLO or over-voltage. Set on fault, and cleared when written to 1b.  0b: No VP fault 1b: VP fault
3	<b>VSYSFLT</b>	R	0x0	VSYS fault when VSYS is below UVLO or over-voltage. Set on fault, and cleared when written to 1b.  0b: No VSYS fault

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				1b: VSYS fault
2	VCCIOFLT	R	0x0	VCCIO fault. Set on fault, and cleared when written to 1b. 0b: No VCCIO fault 1b: VCCIO fault
1	VCC33FLT	R	0x0	VCC33 fault. Set on fault, and cleared when written to 1b. 0b: No VCC33 fault 1b: VCC33 fault
0	VCOREFLT	R	0x0	VCORE fault. Set on fault, and cleared when written to 1b. 0b: No VCORE fault 1b: VCORE fault

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### 6.5.2 SOC.STATUS

#### Register 6-2 SOC.STATUS (System Status, 01h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	HWRSTAT	R	0x0	Hardware Reset Status. Bit is set on hardware reset and is cleared when written to 1b.  0b: No hardware reset 1b: Hardware reset
6	SRST	R	0x0	Soft Reset Event. Bit is set on software reset event and is cleared when written to 1b.  0b: No software reset 1b: Software reset
5	WDTRSTAT	R	0x0	Watchdog Timer Reset Status. When enabled, this bit is set on Watchdog Timer Reset and cleared when written to 1b.  0b: No WDT reset 1b: WDT Reset
4	RFU	R	0x0	Reserved
3	VPLOW	R	0x0	Real-time VP Low Status.  0b: No VP low 1b: VP low
2	VPLOW_LATCH	R	0x0	Latched VP Low Status. During VP low condition, this bit is set and the nIRQ signal is asserted. To clear this bit, write to 1b.  0b: No latched VP low 1b: Latched VP low
1	PBSTAT	R	0x0	Real-time Push-button Status.  0b: Push-button not active 1b: push-button active
0	PBSTAT_LATCH	R	0x0	Latched Push-button Status. This bit is set in normal operation as long as the push button is enabled and on for more than the deglitch time, if not masked. When this bit is set, it will assert the nIRQ signal.  0b: Latched push-button not active 1b: Latched push-button active

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### 6.5.3 SOC.MISC

#### Register 6-3 SOC.MISC (SOC Miscellaneous Configuration, 02h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	HIB	R/W	0x0	Hibernate Mode. This bit is automatically cleared when the power up sequence is initiated, after wake-up timer delay or external event.  0b: Normal 1b: Shutdown mode
6	PBEN	R/W	0x0	AIO6 Push-button Enable.  0b: Push-button not enabled 1b: Push-button enabled
5	VREFSET	R/W	0x0	ADC Reference Voltage Setting.  0b: 2.5V 1b: 3.0V
4	CLKOUTEN	R/W	0x0	Low-speed clock output (CLKOUT) enable.  0b: Not enabled 1b: Enabled
3	MCUALIVE	R/W	0x0	MCU Alive. Set by the MCU to indicate that it is alive. Before this bit is set, ignore all MCU commands (EMUX, gate driver) except SPI register commands. This bit will automatically be cleared when the reset signal to the MCU is asserted.  0b: MCU not alive 1b: MCU alive
2	TPBD	R/W	0x0	Push-button deglitch time:  0b: 32ms 1b: 1ms
1	RFU	R	0x0	Reserved
0	SMEN	R/W	0x0	Signal Manager Enable. This bit is automatically cleared when the reset signal to the MCU is asserted.  0b: Not enabled 1b: Enabled

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6.5.4 SOC.PWRCTL

Register 6-4 SOC.PWRCTL (Power Control, 03h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	CLKOUTFREQ	R/W	0x0	Low-Speed Clock Output Frequency Setting (CLKOUT).  00b: 250Hz 01b: 500Hz 10b: 1kHz 11b: 2kHz
5:3	PWRMON	R/W	0x0	Power Monitor Signal. This field selects the signal to use for AB11 for ADC monitoring (buffered).  000b: VCORE 001b: VCORE x 4/10 010b: VCC33 x 4/10 011b: VCCIO x 4/10 100b: VSYS x 4/10 101b: ISENSE 110b: VPTAT 111b: VP x 1/10
2:0	WUTIMER	R/W	0x0	Wake-up Timer:  000b: infinite 001b: 125ms 010b: 250ms 011b: 500ms 100b: 1s 101b: 2s 110b: 4s 111b: 8s

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6.5.5 SOC.FAULTENABLE

Register 6-5 SOC.FAULTENABLE (Fault enable, 04h)

BIT	NAME	ACCESS <sup>1</sup>	RESET	DESCRIPTION
7	RFU	R/W	0x0	Reserved
6	nTMPWARN	R/W	0x0	Temperature Warning Mask. 0b: Masked 1b: Not masked (asserts nIRQ1)
5	nVPFLT	R/W	0x0	VP Fault Mask. 0b: Masked 1b: Not masked
4	nVSYSFLT	R/W	0x0	VSYS Fault Mask. 0b: Masked 1b: Not masked
3	RFU	R	0x0	Reserved
2	nLDOFLT	R/W	0x0	LDO Fault Mask. 0b: Masked 1b: Not masked
1	nPBINT	R/W	0x0	Push-button Interrupt Mask. 0b: Masked 1b: Not masked
0	nVPINT	R/W	0x0	VP Low Interrupt Mask. 0b: Masked 1b: Not masked

<sup>1</sup> This byte is unlocked for writing when **UNLOCK** = 1b.

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6.5.6 SOC.WATCHDOG

Register 6-6 SOC.WATCHDOG (SOC Watchdog Configuration, 05h)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	SRST	R/W	0x0	Soft Reset. This bit can be set to issue a system soft reset. This bit is always read as 0b. When set, the STATUS.SRST bit will be latched to a 1b so the MCU knows the system is being started after a soft reset.  0b: Do not issue soft reset 1b: Issue soft reset
6:4	RFU	R	0x0	Reserved
3	WDTEN	R/W	0x0	Watchdog Timer Enable. Cleared during hard reset.  0b: disabled 1b: enabled
2:0	TWD	R/W	0x0	Watch-dog Timer.  000b: 62.5ms 001b: 125ms 010b: 250ms 011b: 500ms 100b: 1s 101b: 2s 110b: 4s 111b: 8s

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### 6.5.7 SOC.SYSCONF

#### Register 6-7 SOC.SYSCONF (System Configuration, 2Bh)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	RFU	R	0x0	Reserved
3	VPSET	R/W	0x1	VP Setting. 0b: 12V 1b: 15V
2:1	HVBK_FREQ	R/W	0x1	High-Voltage Buck Switching Frequency Setting. 00b: 50kHz 01b: 100kHz 10b: 200kHz 11b: 400kHz
0	RFU	R	0x0	Reserved

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## 7 CONFIGURABLE ANALOG FRONT-END

### 7.1 Overview

The device includes a Configurable Analog Front End (CAFE, Figure 7-1). The CAFE can be used to sense battery pack current using an integrated Differential Amplifier and 16-bit Sigma-Delta ADC. The CAFE can configure three independent DACs to set three comparator thresholds for over-current detection for the battery pack.

The CAFE can also sense cell voltages via a 16-bit Sigma Delta ADC and MUX which contains inputs for each of the cell balance channels. Internal power supply rails, temperature, and other signals can be selected using the AFE Mux and sampled using the MCU 12-bit SAR ADC.

### 7.2 Features

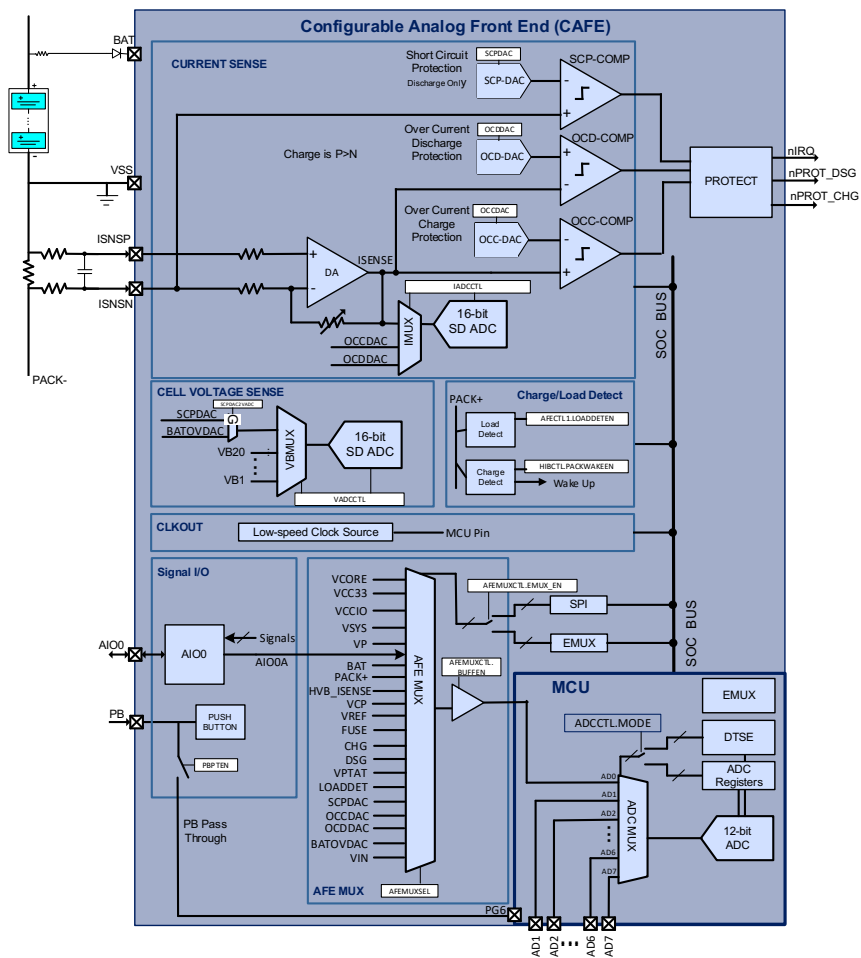
- 16-bit Sigma-Delta ADC for current sense
- Current Sense Differential Programmable-Gain Amplifier
- Analog input/output gain amplifier with ADC Input or signal output selection
- Three comparators with DACs for programmable references for configurable OC warning or fault handling
- 16-bit Sigma-Delta ADC for Voltage Sampling of up to 20 cell voltages
- 12-bit Successive Approximation Register for Temperature sense and Pin ADC input and internal power supplies
- Internal Temperature warning and fault protection
- Push-Button (PB) input for exiting hibernate mode
- PACK+ Charge detection and Load detection
- 2kHz independent clock source

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### 7.3 System Block Diagram

Figure 7-1 Configurable Analog Front End System Block Diagram



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## 7.4 Functional Description

### 7.4.1 Register Protection

Select registers require the protection address SOC.PROT\_KEY be written before the select registers can be written. Registers that require this will contain a note about writing PROT\_KEY. To enable writing of the protected registers, write SOC.PROT\_KEY.KEY with 0xA5, and then write the protected register.

### 7.4.2 Current Sensing

The PAC2514X contains circuitry for battery pack current sense. The positive terminal, I sense positive (ISNSP) and negative terminal, I sense negative (ISNSN) are connected to each side of an external sense resistor. The ISNSP pin is connected to the positive terminal of a differential amplifier (DA) and the ISNSN pin is connected to the negative terminal of the amplifier. The differential amplifier has a programmable gain up to x128. This amplifier has a common-mode range of -0.3V to 0.5V.

The output of the differential amplifier is connected to the 16-bit Sigma-Delta ADC for current sensing and also to over current protection comparators.

### 7.4.3 IADC 16-bit Sigma-Delta ADC

The IADC is a 16-bit Sigma-Delta ADC and has an input range of -500mV to +500mV. The IADC is controlled using SOC.IADCCTL register. Write the SOC.IADCCTL register to set the Diff Amp gain, select the IMUX setting, and start the IADC conversion. To know if the conversion is complete, the SOC.IADCCTL.IADCBUSY bit can be polled. The IADCBUSY bit signal is also routed to the MCU PB3 GPIO, which can be configured to generate an interrupt based on the IADCBUSY signal.

#### Differential Amplifier Gain

Use SOC.IADCCTL.DAGAIN to set to gain between 1x to 128x.

#### Differential Amplifier Reference

The Differential Amplifier reference is 0.5V.

#### Measuring Current SENSE voltages

The Current SENSE ADC (IADC) is enabled by setting the SOC.SIGMGRCTL2.IADCEN bit.

In order to measure the battery pack current through the SENSE resistor, the IADC multiplexer must be configured to select the differential output by writing a 0d to the SOC.IADCTL.IMUXSEL register. Alternatively, the same multiplexer allows the voltage conversion of the SCP DAC, OCC DAC and OCD DAC. However, when OCCDAC, OCDDAC are selected to IMUX mux, the DA is disconnected from current sensing and operate as buffer mode.

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To start a IADC Conversion, the SOC.IADCCTL.ADCSTART bit must be set to 1d. The read only bit SOC.VADCCTL.IADCBUSY bit will set to 1d during the conversion and set to 0d when completed. The 16 bit conversion can be obtained by reading the SOC.IADCRESHI and SOC.IADCRESLO registers.

Reading the current SENSE value can be achieved concurrently while the cell voltage ADC (VADC) operates and convert independent cell voltage values.

### 7.4.4 Over-Current Protection

There are three protection comparators that may be used for over-current protection: one for short circuit protection (SCP-COMP), one for over-current discharge protection (OCD-COMP) and one for over-current charge protection (OCC-COMP). Each of the comparators has a DAC that may be used to set the comparator reference.

When one of the comparators trips, the device will send a signal to the driver manager and can be programmed in various ways to disable the CHG/DSG FETs, as well as interrupt the MCU via an IRQ signal. Determining which source asserted the IRQ signal can be achieved by reading the SOC.SIGFAULT register.

### 7.4.5 Short- Circuit Protection

Short-Circuit protection (SCP) is designed to disable gate drivers if the battery pack suddenly is discharging a large amount of current. The SCP is implemented with the SCP DAC (0.5V Vref) and SCP comparator (0.5V Vref) to compare the DAC setting to the ISNSN signal. If the comparator threshold is met, the comparator will set the SOC.SIGFAULT.SCPFLT bit. An active SCP Fault can be configured to perform the following:

- disable the CHG gate driver via the SOC.PROTEN.SCPCPROTEN bit,
- disable the DSG gate driver via the SOC.PROTEN.SCPDPROTEN bit.
- Interrupt the MCU via the nIRQ2 signal connected to the PA0 GPIO signal if the SOC.SIGFAULTEN.SCPFAULTEN bit is set.

The SCP DAC value can be set by writing the SOC.SCPDDAC register. The SCP comparator is enabled by setting the SOC.SIGMGRCTL1.SCPEN bit. The SCP comparator blanking time can be configured by writing the SOC.SCPCFG register. The hysteresis is not configurable and is fixed. Once the SCP DAC value is exceeded at the SCP Comparator input, a short circuit event will be registered and the SOC.SIGFAULT.SCPFAULT flag will be set. The SOC.SIGFAULT.SCPFAULT flag is cleared by writing a 1d.

Short circuit protection comparator output can be polled in real time by reading the SOC.BATRTS.SCP\_RTS bit.

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### 7.4.6 Over-Current Charge Protection

Over-Current Charge protection (OCC) is designed to be implemented with the OCC DAC (0.5V Vref) and OCC comparator (0.5V Vref) to compare the DAC setting to the differential amplifier output signal. If the comparator threshold is met, the comparator will set the SOC.SIGFAULT.OCCFLT bit. An active OCC Fault can be configured to perform the following:

- disable the CHG gate driver via the SOC.PROTEN.OCCPPROTEN bit,
- Interrupt the MCU via the nIRQ2 signal connected to the PA0 GPIO signal if the SOC.SIGFAULTEN.OCCFAULTEN bit is set.

The OCC DAC value can be set by writing the SOC.OCCDAC register. The OCC comparator is enabled by setting the SOC.SIGMGRCTL1.OCCEN bit. The OCC comparator blanking time can be configured by writing the SOC.OCCCFG register. The hysteresis is not configurable and is fixed. Once the OCC DAC value is exceeded at the OCC Comparator input, an Over Current Charge event will be registered and the SOC.SIGFAULT.OCCFAULT flag will be set. The SOC.SIGFAULT.OCCFAULT flag is cleared by writing a 1d.

Over current charge protection comparator output can be polled in real time by reading the SOC.BATRTS.OCC\_RTS bit.

When OCCDAC, OCDDAC are selected to IADC IMUX, the DA is disconnected from current sensing and operate as buffer mode.

### 7.4.7 Over-Current Discharge Protection

Over-Current Discharge protection (OCD) is designed to be implemented with the OCD DAC (0.5V Vref) and OCD comparator (0.5V Vref) to compare the DAC setting to the differential amplifier output signal. If the comparator threshold is met, the comparator will set the SOC.SIGFAULT.OCDFLT bit. An active OCD Fault can be configured to perform the following:

- disable the CHG gate driver via the SOC.PROTEN.OCDPPROTEN bit,
- Interrupt the MCU via the nIRQ2 signal connected to the PA0 GPIO signal if the SOC.SIGFAULTEN.OCDFAULTEN bit is set.

The OCD DAC value can be set by writing the SOC.OCDDAC register. The OCD comparator is enabled by setting the SOC.SIGMGRCTL1.OCDEN bit. The OCD comparator blanking time and hysteresis can be configured by writing the SOC.OCDCFG register. Once the OCD DAC value is exceeded at the OCD Comparator input, an Over Current Discharge event will be registered and the SOC.SIGFAULT.OCDFAULT flag will be set. The SOC.SIGFAULT.OCDFAULT flag is cleared by writing a 1d. Over current discharge protection comparator output can be polled in real time by reading the SOC.BATRTS.OCD\_RTS bit.

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### 7.4.8 Battery Over-Voltage Protection

Battery Over Voltage protection (BATOV) is designed to be implemented with the BATOV DAC (2.5V Vref) and BATOV comparator (2.5V Vref) to compare the DAC setting to the scaled down version (1/50) version of the battery pack's PACK+ terminal. If the comparator threshold is met, the comparator will set the SOC.SIGFAULT.BATOVFLT bit. An active BATOV Fault can be configured to perform the following:

- disable the CHG gate driver via the SOC.PROTEN.BATOVCPPROTEN bit,
- disable the DSG gate driver via the SOC.PROTEN.BATOVDCPPROTEN bit.
- Interrupt the MCU via the nIRQ2 signal connected to the PA0 GPIO signal if the SOC.SIGFAULTEN.BATOVCPROTEN bit is set.
- Interrupt the MCU via the nIRQ2 signal connected to the PA0 GPIO signal if the SOC.SIGFAULTEN.BATOVDPROTEN bit is set.

The BATOV DAC value can be set by writing the SOC.BATOVDAC register. The BATOV comparator is enabled by setting the SOC.SIGMGRCTL1.BATOVEN bit. The BATOV comparator blanking time can be configured by writing the SOC.BATOVCFG register. The hysteresis is not configurable and is fixed. Once the BATOV DAC value is exceeded at the BATOV Comparator input, an Over Voltage event will be registered and the SOC.SIGFAULT.BATOVFAULT flag will be set. The SOC.SIGFAULT.BATOVFAULT flag is cleared by writing a 1d.

Battery over voltage protection comparator output can be polled in real time by reading the SOC.BATRTS.BATOV\_RTS bit.

### 7.4.9 Voltage Sensing

The PAC2514X also contains a 16-bit Sigma-Delta ADC that may be used for voltage sensing for the individual cells. There is a MUX that selects each of the individual cell balance nodes (VB1 to VB20) so that they may be sampled by the 16-bit ADC.

The SOC bus is used for the MUX select as well as the ADC operation and fetching of the 16-bit result from the MCU.

### 7.4.10 Measuring Independent Cell Voltages

The cell voltage ADC (VADC) is enabled by setting the SOC.SIGMGRCTL2.VADCEN bit. Cells for which voltage ADC capturing will be performed, must also be enabled by setting their respective enable bit. This can be accomplished by writing to the SOC.CELLEN1.CENx, SOC.CELLEN2.CENx and SOC.CELLEN3.CENx registers. Cells which are not enabled will be removed from the ADC path and can't be digitized.

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In order to measure each independent voltage, the VADC multiplexer must be configured to select the cell which will be connected into the VADC converter. The VBMUXSEL value can be configured by writing a number from 0d to 19d to the SOC.VADCTL.VBMUX register. Alternatively, the same multiplexer allows the voltage conversion of the Battery Over Voltage DAC by selecting multiplexer entry 20d.

To start a VADC Conversion, the SOC.VADCCTL.ADCSTART bit must be set to 1d. The read only bit SOC.VADCCTL.VADCBUSY bit will set to 1d during the conversion and set to 0d when completed. The VADCBUSY bit signal is also routed to the MCU PB4 GPIO, which can be configured to generate an interrupt based on the VADCBUSY signal. The 16-bit Cell Voltage conversion can be obtained by reading the SOC.VADCRESHI and SOC.VADCRESLO registers.

Reading cell voltages can be achieved concurrently while the current ADC operates and convert current values.

### 7.4.11 AFE MUX

The CAFE also contains the AFE MUX that can be used to sample the internal power supply rails on the device, internal die temperature, and other signals.

The AFE MUX select can be controlled from the SOC bus or via the EMUX. The output of the AFE MUX is connected to the 12-bit ADC on the MCU so it may be sampled by the auto-sequencer.

The MUX channels that are available are:

- VCORE – 1.9V Core Logic LDO
- VCC33 – 3.3V Analog LDO
- VCCIO – 3.3V Digital I/O LDO
- VSYS – 5V System Supply
- VP – DC/DC Output
- AIO0A – AIO0 Analog Output
- BAT – Battery Stack Input
- PACK+ - Charger Supply Input
- VCP – Charge Pump Output
- VREF – 2.5V Voltage reference
- FUSE – FUSE output
- CHG – CHG FET gate driver signal
- DSG – DSG FET gate driver signal
- VPTAT – Internal Temperature Sensor
- LOADDET – Load monitoring signal
- SCPDAC – Short Circuit Protection DAC output
- OCCDAC – Over Current Charge DAC output
- OCDDAC – Over Current Discharge DAC output
- VIN – Main Input Supply Voltage

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#### 7.4.12 Enabling the CAFE

The CAFE will not respond to signals from the MCU other than the SOC Bridge until the MCU sets SOC.AFECTL1.MCUALIVE to 1b. Also, before the CAFE sub-system can begin any signal conditioning, it must be enabled. To enable the CAFE set SOC.AFECTL1.SIGEN to 1b.

#### 7.4.13 Push-Button (PB) Input

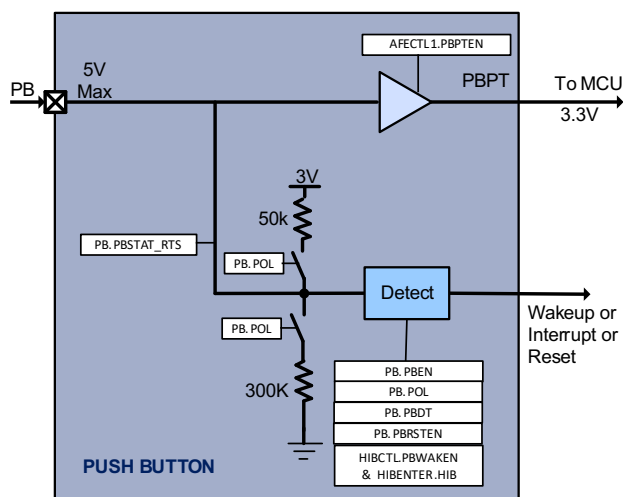
The PAC2514X contains a push-button input pin (PB) and a push-button module (see Figure 7 below). A push-button pass through to the MCU can be enabled so that the MCU can read the state of the digital PB pin directly on the PG6 GPIO.

The push-button module can be used to wake-up the device from hibernate, interrupt the MCU, or reset the device. The push-button polarity can be set to active high or active low using the polarity setting.

The push-button module can be configured so that an active PB will wake up the PAC2514X from hibernate mode.

When enabled, the push-button may also be used as a hardware reset when held active for longer than 8s during normal operation. Once the push-button is enabled, the polarity setting will determine whether the PB input will be pulled up to 3V with a 50kΩ resistor or pulled down to GND with a 300kΩ resistor. There is also a programmable de-glitch time that may be configured to 1, 4, 8, or 32ms. The PAC2514X contains an integrated temperature sensor that can be sampled on the analog bus on channel AB11 (VPTAT). To read the temperature, sample this ADC channel and convert the ADC counts to °C using the following formula:

Figure 7-2 Push Button Block Diagram



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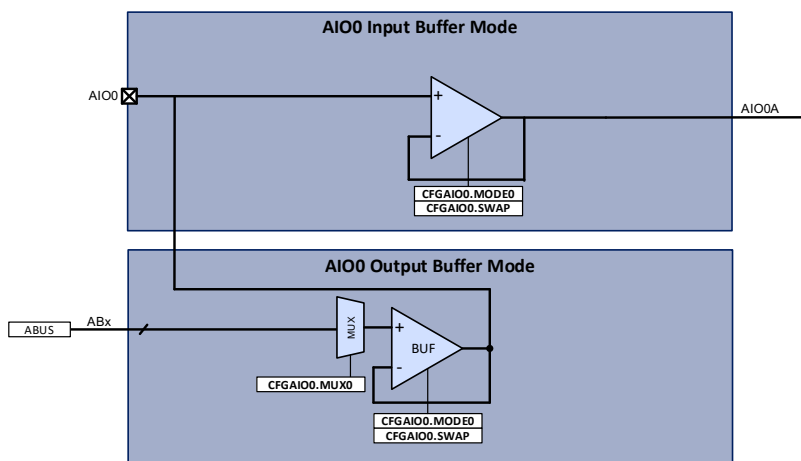
### 7.5 Analog I/O 0 (AIO0)

The PAC2514X has an AIO0 module and pin that includes a gain amplifier for analog I/O. The AIO0 pin can be configured as an input to the amplifier with the output of the gain amplifier, AIO0A, routed to the AFE Mux for input to the MCU ADC. Or the AIO0 pin can be configured to output internal signals of the AFE. The following signals are available for output on the AIO0 pin:

- ADCVREF – 2.5V Voltage Reference
- AFEMUXOUT – AFE Mux Output to the MCU ADC
- IMUXOUT – Current Mux Output to the Current ADC
- VBMUXOUT – Battery Cell Voltage Mux Output to the Voltage ADC

#### 7.5.1 AIO0 Block Diagram

Figure 7-3 AIO0 Block Diagram



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## 8 Miscellaneous AFE Registers and Controls

### 8.1 General-Purpose Register

The device contains an 8-bit general-purpose register in the analog sub-system that is available for user applications. This register may be used to synchronize information between the MCU and analog sub-system for the application.

The user may read or write this register at **SOC.GP**. This register is only reset on a power-on-reset (POR) or a Push Button (PB) reset.

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## 8.2 AFE Registers

### Analog Front End Register Map

Table 8-1 Analog Front End Register Map

SOC ADDRESS	NAME	DESCRIPTION	RESET VALUE
<b>Configurable Analog Front End</b>			
0x00	<b>AFECTL1</b>	AFE Control 1	
0x01	<b>AFECTL2</b>	AFE Control 2	
0x02	<b>DVRCTL</b>	Driver Control	
0x03	<b>AFEMUXCTL</b>	AFE Mux Control	
0x04	<b>AFEMUXSEL</b>	AFE Mux Select	
0x05	<b>HIBCTL</b>	Hibernate Control	
0x06	<b>HIBENTER</b>	Hibernate Enter	
0x07	<b>RSTSTAT</b>	Reset Status	
0x08	<b>PB</b>	Push Button	
0x09	<b>AIO0CFG</b>	AIO 0 Configuration	
0x10	<b>PROTKEY</b>	Protection Key	
0x11	<b>SIGMGRCTL1</b>	Signal Manager Control 1	
0x12	<b>SIGMGRCTL2</b>	Signal Manager Control 2	
0x13	<b>PROTEN</b>	Protection Enable	
0x14	<b>FUSE</b>	Fuse Driver Control	
0x15	<b>PWRFAULTEN</b>	Power Fault Enable	
0x16	<b>PWRFAULT</b>	Power Fault	
0x17	<b>TEMPFAULTEN</b>	Temperature Fault Enable	
0x18	<b>TEMPFAULT</b>	Temperature Fault	
0x19	<b>SIGFAULTEN</b>	Signal Manager Fault Enable	
0x1A	<b>SIGFAULT</b>	Signal Manager Fault	
0x1B	<b>BATRTS</b>	Battery Real-Time Status	
0x20	<b>BATOVCFG</b>	Battery Over-Voltage Configuration	
0x21	<b>BATOVDAC</b>	Battery Over Voltage DAC Setting	
0x22	<b>VADCCTL</b>	Voltage ADC Control	
0x23	<b>VADCRESHI</b>	Voltage ADC Result Hi Byte	
0x24	<b>VADCRESLO</b>	Voltage ADC Result Low Byte	
0x25	<b>IADCCTL</b>	Current ADC Control	
0x26	<b>IADCRESHI</b>	Current ADC Result Hi Byte	
0x27	<b>IADCRESLO</b>	Current ADC Result Low Byte	

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### Configurable Analog Front End Register Map Continued

SOC ADDRESS	NAME	DESCRIPTION	RESET VALUE
<b>Configurable Analog Front End</b>			
0x28	<b>SCPDAC</b>	Short-Circuit Protection DAC	
0x29	<b>SCPCFG</b>	Short-Circuit Protection Configuraiton	
0x2A	<b>OCDDAC</b>	Over-Current Discharge Protection DAC	
0x2B	<b>OCCCFG</b>	Over Current Charge Protection Configuration	
0x2C	<b>OCCDAC</b>	Over Current Charge Protection DAC	
0x2D	<b>OCDCFG</b>	Over Current Discharge Protection Configuraiton	
0x30	<b>CELLEN1</b>	Cell Enable 1	
0x31	<b>CELLEN2</b>	Cell Enable 2	
0x32	<b>CELLEN3</b>	Cell Enable 3	
0x33	<b>CFGCB1</b>	Configure Cell Balance 1	
0x34	<b>CFGCB2</b>	Configure Cell Balance 2	
0x35	<b>CFGCB3</b>	Configure Cell Balance 3	
0x40	<b>GP</b>	General Purpose	
0x41	<b>CLKOUTCFG</b>	Clock Out Configuration	
0x42	<b>WWDTCTL</b>	Windowed Watchdog Timer Control	
0x43	<b>WWDTCTR</b>	Windowed Watchdog Timer Counter	
0x44	<b>WWDTCDV</b>	Windowed Watchdog Timer Count Down Value	
0x45	<b>WWDTWIN</b>	Windowed Watchdog Timer Window	
0x46	<b>WWDTRST</b>	Windowed Watchdog Timer Reset	

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### SOC.AFECTL1

Register 8-1. SOC.AFECTL1 (AFE Control 1, SOC 0x00)

BITS	NAME	ACCESS	RESET	DIFFAMP MODE
7	SRST	RW	0	Soft Reset Write to 1 to reset the device. The majority of AFE registers will be reset also unless noted. This bit is self clearing and will always be read as 0.
6	MCUALIVE	RW	0	MCU Alive This bit should be written to 1 by the MCU after it comes out of reset. Prior to setting this bit, the AFE will only respond to SPI transactions.
5	RFU	RW	0	Reserved, write as 0.
4	DIS_CPOK	RW	0	Charge Pump OK Overwrite 0: Normal Operation 1: Overwrite to OK
3	SCPDAC2VADC	RW	0	Mux Selection for Voltage SD ADC Ch20 0: Select BATOV DAC 1: Select SCPDAC
2	LOADDETEN	RW	0	Load Detect Enable 0: Disabled 1: Enabled When enabled, measure PACK+ to determine if a load is present.
1	HVCPEN	RW	0	High Voltage Charge Pump Enable 0: Disabled 1: Enabled
0	SIGEN	RW	0	Signal Manager Tile Enable 0: disabled 1: enabled

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**SOC.DRVCTL**

Register 8-2. SOC.DRVCTL (Driver Control, SOC 0x02)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	RFU	R	0	Reserved
1:0	DRVMODE	RW	0x0	Driver Mode  0: Drivers Disabled 1: Drivers Enabled - MCU signals control CHG/DSG on off. 2: Source Follower Mode 3: Reserved  Driver Mode is set to 0 if SEGEN = 0 or if nRST is active

**SOC.AFEMUXCTL**

Register 8-3. SOC.AFEMUXCTL (AFE Mux Control, SOC 0x03)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:2	RFU	R	0	Reserved
1	BUFFEN	RW	0x0	ADC Buffer Enable  0: Disabled 1: Enabled  Enables the buffer after the AFE Mux that drives the signal feeding channel 0 of the ADC Mux.
0	EMUX_EN	RW	0x0	EMUX Enable – Enables the AFE EMUX Module  0: Disabled 1: Enabled  When the EMUX is enabled, writes to the AFEMUXSEL will be performed by the EMUX logic. The AFEMUXSEL cannot be written by the SOC Bridge SPI I/F, but can be read over the SOC Bridge SPI I/F.  Setting EMUX_EN = 0 will reset the AFE EMUX module.

**SOC.AFEMUXSEL**

Register 8-4. SOC.AFEMUXSEL (AFE Mux Select, SOC 0x04)

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BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	RFU	R	0	Reserved
4:0	AFEMUXSEL	R/W	0x0	<p>AFE MUX Channel Selector:</p> <p>0 = VCORE 1 = VCORE / 2.5 2 = VDDA / 2.5 3 = VCCIO / 2.5 4 = VSYS / 2.5 5 = ISENSE 6 = VPTAT 7 = VP / 10 8 = VREF / 2 9 = FUSE / 10 10 = CHG / 50 11 = DSG / 50 12 = BAT / 50 13 = AIO0A 14 = LOADDET 15 = SCPDAC 16 = OCCDAC 17 = OCDDAC 18 = BATOVDAC 19 = VIN / 50 20 = PACK+ / 50 21 = VCP / 50</p> <p>This register is only writeable by the SOC Bridge SPI I/F when EMUX_EN=0, but is readable by the SOC Bridge SPI I/F at anytime.</p>

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SOC.HIBCTL

Register 8-5. SOC.HIBCTL (Hibernate Control, SOC 0x05)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	WUTIMER	R/W	0x0	Wake Up Timer Duration  0: Disabled 1: 125ms 2: 250ms 3: 500ms 4: 1s 5: 2s 6: 4s 7: 8s
4:3	WAKESRC	R/W	0x0	Wake Up Source  0: PB 1: PACK+ 2: WUTIMER 3: RFU
2	PACKWAKEVREF	R/W	0x0	PACK+ Wake Up Voltage Reference Threshold  0: 5V 1: 20V
1	PACKWAKEEN	R/W	0x0	PACK+ Wake Up Enable  0: Disabled 1: Enabled
0	PBWAKEEN	R/W	0x0	Push Button Wake Up Enable  0: Disabled 1: Enabled

Note: If all wake-up enables are set to Disabled when HIBENTER.HIB is written, then PBWAKEN and PACKWAKEN will be set to 1 as a fail safe to allow the device to be brought out of hibernate.

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### SOC.HIBENTER

Register 8-6. SOC.HIBENTER (Hibernate Enter, SOC 0x06)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	RFU	R	0	Reserved, write as 0.
0	HIB	R/W	0x0	Hibernate  Write to 1 to enter Hibernate. This bit is automatically cleared upon wakeup.

### SOC.RSTSTAT

Register 8-7. SOC.RSTSTAT (Reset Status, SOC 0x07)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	RFU	R	0x0	Reserved
4	PBRST	W1C	0x0	Push Button Reset Flag  This flag will be set when the Push Button is enabled and has been active for 8 seconds.
3	HIBRST	W1C	0x0	Hibernate Reset Flag  This flag will be set when the device has been reset following a hibernate wake-up. Read the HIBCTL.WAKESRC bits to determine the source of the hibernate wake-up.
2	WDTRST	W1C	0x0	AFE Watchdog Timer Reset Flag  This flag will be set when the device has been reset by the AFE Watchdog Timer
1	SOFTRST	W1C	0x0	Soft Reset Flag  This flag will be set when an AFE Soft Reset has been performed by writing a 1 to SOC.AFECTL1.SRST.
0	FLTRST	W1C	0x0	Fault Reset Flag  This flag will be set when a power or temperature fault occurs that causes a device reset. The following faults may cause a Fault Reset. Power Faults: VPFLT, VSYSFLT, VDDIOFLT, VDDAFLT, VCCOREFLT Temp Faults: TMPFLT Following a Fault Reset, read the PWRFAULT and TEMPFAULT registers to determine which faults caused the reset.

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SOC.PB

Register 8-8. SOC.PB (Push Button, SOC 0x08)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	PBSTAT_RTS	R	0x0	
6	PBINTF	W1C	0x0	Push Button Interrupt Flag
5	PBINTEN	R/W	0x0	Push Button Interrupt Enable  The interrupt is level sensitive.
4	PBPOL	R/W	0x0	Push Button Polarity  0: Active Low 1: Active High  Depending on other bit settings, an active signal will generate an interrupt, hibernate wake-up, or reset.
3:2	PBDT	R/W	0x0	Push Button Deglitch Time  0: 1ms 1: 4ms 2: 8ms 3: 32ms
1	PBRSTEN	R/W	0x0	Push Button Reset Enable  0: Disabled 1: Enabled  If enabled, when the Push Button has been active for 8 seconds, the device shall be reset.
0	PBEN	R/W	0x0	Push Button Enabled  0: Disabled 1: Enabled

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### SOC.AIO0CFG

Register 8-9. SOC.AIO0CFG (Analog I/O 0 Configuration, SOC 0x09)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	MUXSEL	R/W	0x0	AIO0 Mux Select - during I/O output mode 0: ADC VREF = 2.5V 1: AFEMUXOUT 2: IMUXOUT 3: VBMUXOUT 15:4: RFU
4	RFU	R/W	0x0	Reserved
3:2	SWAP	R/W	0x0	Swaps the offset of the buffer. 0: No swap 1: Swap
1	MODE	R/W	0x0	AIO0 Buffer Mode 0: Input Buffer Mode 1: Output Buffer mode (2mA drive strength)
0	AIO0EN	R/W	0x0	AIO0 Buffer Enable 0: Disabled 1: Enabled

### SOC.PROT\_KEY

Register 8-10. SOC.PROT\_KEY (Protection Key, SOC 0x10)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	KEY	RW	0	Protection Key  Select SOC registers require that PROT_KEY.KEY be written with 0xA5 before those registers can be written. The KEY field is self clearing to 0x0 after any write to one of the select registers.

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**SOC.SIGMGRCTL1**

Register 8-11. SOC.SIGMGRCTL1 (Signal Manager Control 1, SOC 0x11)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:5	RFU	R	0x0	Reserved
4	DAEN	R/W	0x0	Current Sense Differential Amp Enable
3	SCPEN	R/W	0x0	Short Circuit Protection DAC and Comparator Enable
2	OCCEN	R/W	0x0	Over Current Charge Protection DAC and Comparator Enable
1	OCDEN	R/W	0x0	Over Current Discharge Protection DAC and Comparator Enable
0	BATOVEN	R/W	0x0	Battery Over Voltage DAC and Comparator Enable

Note: This register requires a write of PROT\_KEY before register can be written.

**SOC.SIGMGRCTL2**

Register 8-12. SOC.SIGMGRCTL2 (Signal Manager Control 2, SOC 0x12)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	RFU	R	0x0	Reserved
2	PBPTEN	R/W	0x0	Push Button Pass Through Enable
1	IADCEN	R/W	0x0	Current ADC Enable
0	VADCEN	R/W	0x0	Voltage ADC Enable

**SOC.PROTEN**

Register 8-13. SOC.PROTEN (Reset Status, SOC 0x13)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	RFU	R	0x0	Reserved
5	SCPCPROTEN	R/W	0x0	Short Circuit Protection CHG Protection Enable – If enabled, then when protection is activated the CHG FET will be disabled
4	SCPDPROTEN	R/W	0x0	Short Circuit Protection DSG Protection Enable – If enabled, then when protection is activated the DSG FET will be disabled
3	OCCPROTEN	R/W	0x0	Over Current CHG Protection Enable – If enabled, then when protection is activated the CHG FET will be disabled
2	OCDPROTEN	R/W	0x0	Over Current DSG Protection Enable – If enabled, then when protection is

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				activated the DSG FET will be disabled
1	BATOVCPROTEN	R/W	0x0	Battery Over Voltage CHG Protection Enable – If enabled, then when protection is activated the CHG FET will be disabled
0	BATOVDPROTEN	R/W	0x0	Battery Over Voltage DSG Protection Enable – If enabled, then when protection is activated the DSG FET will be disabled

Note: This register requires a write of PROT\_KEY before register can be written.

SOC.FUSE

Register 8-14. SOC.FUSE (Fuse Driver Control, SOC 0x14)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:1	FUSEKEY	R/W	0	Must write FUSEKEY = 0x66 and PROT_KEY must already be written with 0xA5 for a write to FUSE.FUSEEN to succeed. FUSEKEY is automatically cleared to 0x00 following the write to the FUSE register.
0	FUSEEN	R/W	0	Enable FUSE FET gate drive output

Note: This register requires a write of PROT\_KEY before register can be written.



#### SOC.PWRFAULTEN

Register 8-15. SOC.PWRFAULTEN (Power Fault Interrupt Enable, SOC 0x15)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	RFU	R	0x0	Reserved
6	DRVFLTEN	R/W	0x0	Driver Fault Interrupt Enable
5	VCCIOFLTEN	R/W	0x0	VCCIO Fault Interrupt Enable
4	VDDAFLTEN	R/W	0x0	VDDA Fault Interrupt Enable
3	VCOREFLTEN	R/W	0x0	VCORE Fault Interrupt Enable
2	VSYSFLTEN	R/W	0x0	VSYS Fault Interrupt Enable
1	VPFLTEN	R/W	0x0	VP Fault Interrupt Enable
0	HVCPFLTEN	R/W	0x0	HVCP Fault Interrupt Enable

Note: This register requires a write of PROT\_KEY before register can be written.



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### SOC.PWRFAULT

Register 8-16. SOC.PWRFAULT (Power Fault, SOC 0x16)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	RFU	R	0x0	Reserved
6	DRVFLT	W1C	0x0	Driver Fault Flag
5	VCCIOFLT	W1C	0x0	VCCIO Fault Flag
4	VDDAFLT	W1C	0x0	VDDA Fault Flag
3	VCOREFLT	W1C	0x0	VCORE Fault Flag
2	VSYSFLT	W1C	0x0	VSYS Fault Flag
1	VPFLT	W1C	0x0	VP Fault Flag
0	HVCPFLT	W1C	0x0	HVCP Fault Flag

### SOC.TEMPFAULTEN

Register 8-17. SOC.TEMPFAULTEN (Temperature Fault Interrupt Enable, SOC 0x17)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	RFU	R	0x0	Reserved
5	TWARN2CBDEN	R/W	0x0	TWARN2 Cell Balance Disable – If set to 1, then when TWARN2 occurs, Cell Balancing will be disabled
4	TWARN1CBDEN	R/W	0x0	TWARN1 Cell Balance Disable – If set to 1, then when TWARN1 occurs, Cell Balancing will be disabled
3	RFU	R	0x0	Reserved
2	TMPFLTEN	R/W	0x0	Temperature Fault Interrupt Enable
1	TWARN2EN	R/W	0x0	TWARN2 Fault Interrupt Enable
0	TWARN1EN	R/W	0x0	TWARN1 Fault Interrupt Enable

Note: This register requires a write of PROT\_KEY before register can be written.

### SOC.TEMPFAULT

Register 8-18. SOC.TEMPFAULT (Temperature Fault Flag, SOC 0x18)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	TWARN2C_RTS	R/W	0x0	TWARN2 Real-Time Status
6	TWARN1_RTS	R/W	0x0	TWARN1 Real-Time Status
5:3	RFU	R	0x0	Reserved
2	TMPFLT	W1C	0x0	Temperature Fault Flag
1	TWARN2	W1C	0x0	TWARN2 Fault Flag
0	TWARN1	W1C	0x0	TWARN1 Fault Flag

### SOC.SIGFAULTEN

Register 8-19. SOC.SIGFAULTEN (Signal Manager Fault Interrupt Enable, SOC 0x19)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:6	RFU	R	0x0	Reserved

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4	EMUXFLTEN	R/W	0x0	EMUX Fault Interrupt Enable
3	SCPFLTEN	R/W	0x0	Short Circuit Protection Fault Interrupt Enable
2	OCCFLTEN	R/W	0x0	Over Current Charge Fault Interrupt Enable
1	OCDFLTEN	R/W	0x0	Over Current Discharge Fault Interrupt Enable
0	BATOVFLTEN	R/W	0x0	Battery Over Voltage Fault Interrupt Enable

Note: This register requires a write of PROT\_KEY before register can be written.

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**SOC.SIGFAULT**

Register 8-20. SOC.SIGFAULT (Signal Manager Fault Flag, SOC 0x1A)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	RFU	R	0x0	Reserved
6	CHGFLT	W1C	0x0	CHG Fault Flag • This flag will be set if a CHG Protection is enabled in the PROTEN register and one of the protections trips and disables the CHG FET. • This bit must be written with a 1 to clear it before the CHG FET can be enabled again.
5	DSGFLT	W1C	0x0	DSG Fault Flag • This flag will be set if a DSG Protection is enabled in the PROTEN register and one of the protections trips and disables the DSG FET. • This bit must be written with a 1 to clear it before the DSG FET can be enabled again.
4	EMUXFLT	W1C	0x0	EMUX Fault Flag – flag is set if EMUX bits [7:5] != 010b
3	SCPFLT	W1C	0x0	Short Circuit Protection Fault Flag
2	OCCFLT	W1C	0x0	Over Current Charge Fault Flag
1	OCDFLT	W1C	0x0	Over Current Discharge Fault Flag
0	BATOVFLT	W1C	0x0	Battery Over Voltage Fault Flag

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**SOC.BATRTS**

Register 8-21. SOC.BATRTS (Battery Protection Comparator Real-Time Status, SOC 0x1B)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	RFU	R	0x0	Reserved
3	SCP_RTS	R/W	0x0	Short Circuit Protection Real-Time Status
2	OCC_RTS	R/W	0x0	Over Current Charge Real-Time Status
1	OCD_RTS	R/W	0x0	Over Current Discharge Real-Time Status
0	BATOV_RTS	R/W	0x0	Battery Over Voltage Real-Time Status

**SOC.BATOVCFG**

Register 8-22. SOC.BATOVCFG (Battery Over Voltage Comparator Config., SOC 0x20)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	BLANKSF	R/W	0x0	Blanking Scale Factor 0 = 1, 1 = 2, 2 = 3.....14 = 15, 15 = 16
3:0	TIMEBASE	R/W	0x0	Time Base: 0 = 32uS, 1 = 64uS, 2 = 128uS, 3 = 256uS .....15 = 1,048,576 uS

Notes:

This register requires a write of PROT\_KEY before register can be written.

Blanking Time = TIMEBASE \* BLANKSF

Example: TIMEBASE = 1, BLANKSF = 2; So, Blanking Time = 64uS \* 3 = 192uS

BATOV Comparator Hysteresis is fixed at 100mV

**SOC.BATOVDAC**

Register 8-23. SOC.BATOVDAC (Battery Over Voltage DAC, SOC 0x21)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	BATOVDAC	RW	0	BATOV DAC Setting – This is the comparator threshold for the BATOV comparator.

Note: This register requires a write of PROT\_KEY before register can be written.





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### SOC.VADCCTL

Register 8-24. SOC.VADCCTL (Voltage ADC Control, SOC 0x22)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	VADCSTART	R/W	0x0	Cell Voltage ADC Start Conversion
6	VADCBUSY	R	0x0	Cell Voltage ADC Busy - This bit is set to 1 during conversion and set to 0 when complete.
5	RFU	R	0	Reserved
4:0	VBMUXSEL	R/W	0x0	Voltage ADC MUX Select:  0: VB1 1: VB2 2: VB3 3: VB4 4: VB5 5: VB6 6: VB7 7: VB8 8: VB9 9: VB10 10: VB11 11: VB12 12: VB13 13: VB14 14: VB15 15: VB16 16: VB17 17: VB18 18: VB19 19: VB20 20: BATOVDAC or SCPDAC (see AFECTL1) 21 - 31: RFU

### SOC.VADCRESHI

Register 8-25. SOC.VADCRESHI (Voltage ADC Result High, SOC 0x23)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	VADCRES[15:8]	RW	0	Voltage ADC Result MSByte

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### SOC.VADCRESLO

Register 8-26. SOC.VADCRESLO (Voltage ADC Result Low, SOC 0x24)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	VADCRES[7:0]	RW	0	Voltage ADC Result LSByte

### SOC.IADCCTL

Register 8-27. SOC.IADCCTL (Current ADC Control, SOC 0x25)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	IADCSTART	R/W	0x0	Current ADC Start Conversion
6	IADCBUSY	R	0x0	Current ADC Busy - This bit is set to 1 during conversion and set to 0 when complete.
5	RFU	R	0	Reserved
4:3	IMUXSEL[1:0]	R/W	0x0	0: Isense Diff Amp Output 1: SCP DAC 2: OCC DAC 3: OCD DAC
2:0	DAGAIN[2:0]	R/W	0x0	Differential Amplifier Gain:  0: 1X 1: 2X 2: 4X 3: 8X 4: 16X 5: 32X 6: 64X 7: 128X

### SOC.IADCRESHI

Register 8-28. SOC.IADCRESHI (Current ADC Result High, SOC 0x26)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	IADCRES[15:8]	RW	0	Current ADC Result MSByte

### SOC.IADCRESLO

Register 8-29. SOC.IADCRESLO (Current ADC Result Low, SOC 0x27)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	IADCRES[7:0]	RW	0	Current ADC Result LSByte

### SOC.SCPDAC

Register 8-30. SOC.SCPDAC (SCP DAC, SOC 0x28)

BIT	NAME	ACCESS	RESET	DESCRIPTION
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7:0	SCP DAC	RW	0	SCP DAC Setting – This is the comparator threshold for the SCP comparator.
-----	---------	----	---	--

Note: This register requires a write of PROT\_KEY before register can be written.

### SOC.SCPCFG

Register 8-31. SOC.SCPCFG (SCP Comparator Configuration, SOC 0x29)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	BLANKSF	R/W	0x0	Blanking Scale Factor 0 = 1, 1 = 2, 2 = 3.....14 = 15, 15 = 16
3:0	TIMEBASE	R/W	0x0	Time Base: 0 = 1uS, 1 = 2uS, 2 = 4uS, 3 = 256uS .....15 = 32768 uS

Notes:

This register requires a write of PROT\_KEY before register can be written.

Blanking Time = TIMEBASE \* BLANKSF

Example: TIMEBASE = 1, BLANKSF = 2; So, Blanking Time = 2uS \* 3 = 6uS

SCP Comparator Hysteresis is fixed at 25mV

### SOC.OCDDAC

Register 8-32. SOC.OCDDAC (OCD DAC, SOC 0x2A)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	OCDDAC	RW	0	OCD DAC Setting – This is the comparator threshold for the OCD comparator.

Note: This register requires a write of PROT\_KEY before register can be written.

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### SOC.OCDCFG

Register 8-33. SOC.OCDCFG (OCD Comparator Configuration, SOC 0x2D)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	BLANKSF	R/W	0x0	Blanking Scale Factor 0 = 1, 1 = 2, 2 = 3.....14 = 15, 15 = 16
3:0	TIMEBASE	R/W	0x0	Time Base: 0 = 1uS, 1 = 2uS, 2 = 4uS, 3 = 256uS .....15 = 32768 uS

Notes:

This register requires a write of PROT\_KEY before register can be written.

Blanking Time = TIMEBASE \* BLANKSF

Example: TIMEBASE = 1, BLANKSF = 2; So, Blanking Time = 2uS \* 3 = 6uS

OCD Comparator Hysteresis is fixed at 25mV

### SOC.OCCDAC

Register 8-34. SOC.OCCDAC (OCC DAC, SOC 0x2C)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	OCCDAC	RW	0	OCC DAC Setting – This is the comparator threshold for the OCC comparator.

Note: This register requires a write of PROT\_KEY before register can be written.

### SOC.OCCCFG

Register 8-35. SOC.OCCCFG (OCC Comparator Configuration, SOC 0x2B)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	BLANKSF	R/W	0x0	Blanking Scale Factor 0 = 1, 1 = 2, 2 = 3.....14 = 15, 15 = 16
3:0	TIMEBASE	R/W	0x0	Time Base: 0 = 1uS, 1 = 2uS, 2 = 4uS, 3 = 256uS .....15 = 32768 uS

Notes:

This register requires a write of PROT\_KEY before register can be written.

Blanking Time = TIMEBASE \* BLANKSF

Example: TIMEBASE = 1, BLANKSF = 2; So, Blanking Time = 2uS \* 3 = 6uS

OCC Comparator Hysteresis is fixed at 25mV

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### SOC.CELLEN1

Register 8-36. SOC.CELLEN1 (Cell Enable 1, SOC 0x30)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	CEN8	R/W	0x0	Cell 8 Enable
6	CEN7	R/W	0x0	Cell 7 Enable
5	CEN6	R/W	0x0	Cell 6 Enable
4	CEN5	R/W	0x0	Cell 5 Enable
3	CEN4	R/W	0x0	Cell 4 Enable
2	CEN3	R/W	0x0	Cell 3 Enable
1	CEN2	R/W	0x0	Cell 2 Enable
0	CEN1	R/W	0x0	Cell 1 Enable

### SOC.CELLEN2

Register 8-37. SOC.CELLEN2 (Cell Enable 2, SOC 0x31)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	CEN16	R/W	0x0	Cell 16 Enable
6	CEN15	R/W	0x0	Cell 15 Enable
5	CEN14	R/W	0x0	Cell 14 Enable
4	CEN13	R/W	0x0	Cell 13 Enable
3	CEN12	R/W	0x0	Cell 12 Enable
2	CEN11	R/W	0x0	Cell 11 Enable
1	CEN10	R/W	0x0	Cell 10 Enable
0	CEN9	R/W	0x0	Cell 9 Enable

### SOC.CELLEN3

Register 8-38. SOC.CELLEN3 (Cell Enable 3, SOC 0x32)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	RFU	R	0x0	Reserved
3	CEN20	R/W	0x0	Cell 20 Enable
2	CEN19	R/W	0x0	Cell 19 Enable
1	CEN18	R/W	0x0	Cell 18 Enable
0	CEN17	R/W	0x0	Cell 17 Enable

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### SOC.CFGCB1

Register 8-39. SOC.CFGCB1 (Configure Cell Balance 1, SOC 0x33)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	VB8	R/W	0x0	Cell 8 Cell Balance Enable
6	VB7	R/W	0x0	Cell 7 Cell Balance Enable
5	VB6	R/W	0x0	Cell 6 Cell Balance Enable
4	VB5	R/W	0x0	Cell 5 Cell Balance Enable
3	VB4	R/W	0x0	Cell 4 Cell Balance Enable
2	VB3	R/W	0x0	Cell 3 Cell Balance Enable
1	VB2	R/W	0x0	Cell 2 Cell Balance Enable
0	VB1	R/W	0x0	Cell 1 Cell Balance Enable

### SOC.CFGCB2

Register 8-40. SOC.CFGCB2 (Configure Cell Balance 2, SOC 0x34)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7	VB16	R/W	0x0	Cell 16 Cell Balance Enable
6	VB15	R/W	0x0	Cell 15 Cell Balance Enable
5	VB14	R/W	0x0	Cell 14 Cell Balance Enable
4	VB13	R/W	0x0	Cell 13 Cell Balance Enable
3	VB12	R/W	0x0	Cell 12 Cell Balance Enable
2	VB11	R/W	0x0	Cell 11 Cell Balance Enable
1	VB10	R/W	0x0	Cell 10 Cell Balance Enable
0	VB9	R/W	0x0	Cell 9 Cell Balance Enable

### SOC.CFGCB3

Register 8-41. SOC.CFGCB3 (Configure Cell Balance 3, SOC 0x35)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:4	RFU	R	0x0	Reserved
3	VB20	R/W	0x0	Cell 20 Cell Balance Enable
2	VB19	R/W	0x0	Cell 19 Cell Balance Enable
1	VB18	R/W	0x0	Cell 18 Cell Balance Enable
0	VB17	R/W	0x0	Cell 17 Cell Balance Enable

### SOC.GP

Register 8-42. SOC.GP (General-Purpose Register, SOC 0x40)

BIT	NAME	ACCESS	RESET	DESCRIPTION
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7:0	GP	RW	0x0	General-purpose read-write register.
-----	----	----	-----	--------------------------------------

SOC.CLKOUTCFG

Register 8-43. SOC.CLKOUTCFG (Clock Out Configuration, SOC 0x41)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	RFU	R	0	Reserved
2:1	CLKOUTFREQ[1:0]	RW	0x0	Low-Speed Clock Output Frequency Setting 0: 250Hz 1: 500Hz 2: 1kHz 3: 2kHz
0	CLKOUTEN	RW	0x0	Low Speed Clock Output Enable

Note: Used during clock test that can help meet Class B Safety

SOC.WWDCTL

Register 8-44. SOC.WWDCTL (Windowed Watchdog Timer Control, SOC 0x42)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:3	KEY	R	0	Write KEY = 0x14 to modify WWDT registers. All other values disallow writes to WWDT registers except WWDTRST register which can be written at anytime.
2:1	CLKDIV[1:0]	RW	0x0	WWDT Clock Divider – The WWDT Clock = 32kHz / CLKDIV 0: /2 1: /16 2: /128 3: /1024
0	EN	RW	0x0	WWDT Enable

Note: The WWDT runs off of a 32kHz clock that is independent of the 4MHz CLKREF that the MCU runs off. When the WWDT is used, it can help meet Class B Safety requirements.



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### SOC.WWDTCR

Register 8-45. SOC.WWDTCR (Windowed Watchdog Timer Counter, SOC 0x43)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	CTR[7:0]	RW	0x0	WWDTCR Counter Value

### SOC.WWDTCDV

Register 8-46. SOC.WWDTCDV (Windowed Watchdog Timer Count Down Value, SOC 0x44)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	CDV[7:0]	RW	0x0	WWDTCDV Count Down Value

### SOC.WWDTCWIN

Register 8-47. SOC.WWDTCWIN (Windowed Watchdog Timer Window, SOC 0x45)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	WINDOW[7:0]	RW	0x0	WWDTCWIN Window Value - If WWDTCRST is written when CTR >= WINDOW, then the WWDTCR will issue a device reset.

### SOC.WWDTCRST

Register 8-48. SOC.WWDTCRST (Windowed Watchdog Timer Reset, SOC 0x46)

BIT	NAME	ACCESS	RESET	DESCRIPTION
7:0	RESET[7:0]	RW	0x0	WWDTCRST Reset (Pet the Dog / Feed the Dog) - Write this register with 0xAC to keep it from resetting the device. - A Write of 0xAC will reset the WWDTCR by reloading the CDV value into the CTR. - If CTR >= WINDOW when 0xAC is written, then the WWDTCR shall issue a device reset. - If CTR counts down to 0 before RESET is written with 0xAC the WWDTCR will issue a device reset. - This register shall automatically be cleared to 0x00, and shall always read 0x00.

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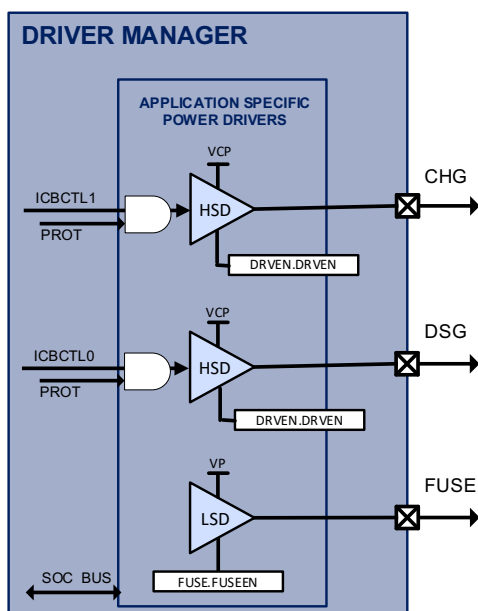


## 8.3 Driver Manager

### Features

- High-Side gate drivers for CHG and DSG FET
- Low-side gate driver for external FUSE

#### 8.3.1 Block Diagram



### Functional Description

The Application Specific Power Drivers™ (ASPD) module drives the gate of the external CHG and DSG FETs and external protection fuse FET for the battery pack.

The CHG and DSG FET gates are driven from the CHG and DSG pins. The gate drive voltage for the CHG and DSG FETs is VCP (BAT + 9V). The FUSE output is a low-side switch supplied by VP which is intended for driving the gate on an external FET, which is used to blow an external fuse in series with PACK+ and the battery stack. Source Follower Mode can be selected for lower current operations and not require enabling the charge pump. In this mode, CHG drive is off and DSG is on with a pull up to BAT. These modes are control by the DRVMODE control bits (see [SOC.DRVCTL \(Driver Control, SOC 0x02\)](#))

The FUSE output is a low-side switch supplied by VP which is intended for driving the gate on an external FET which is typically used to below an external fuse in series with PACK+ and the battery stack. The FUSE could support another low-side driver need such as driving an LED.

The ASPD also integrates gate driver over-current, under-voltage and over-voltage protection. Over current and battery over voltage protections can be enabled using the SIGMGRCTL1 register and the PROTEN

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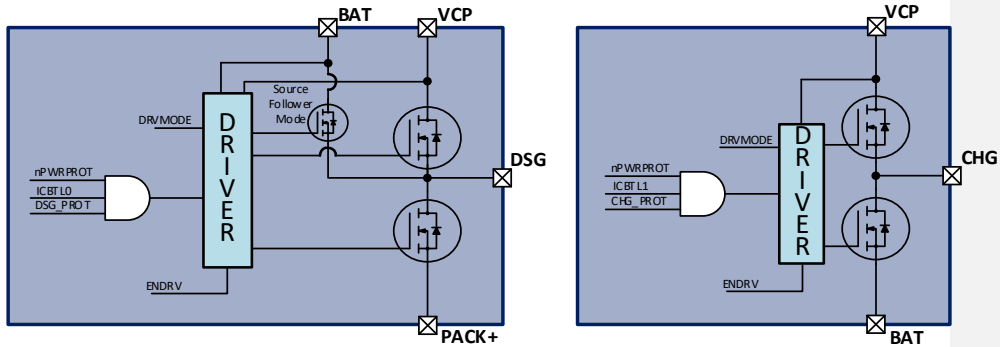
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register. These protections control the nPROT\_CHG and nPROT\_DSG signals that disable the gate drivers when active.

### 8.3.2 Detail Block Diagram



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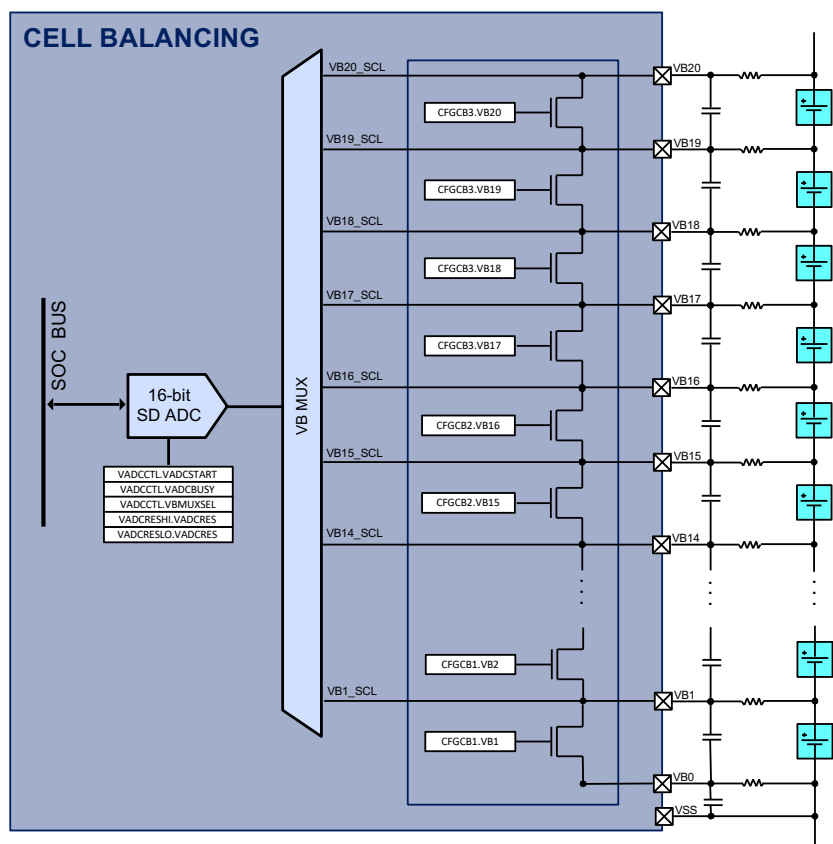
### 8.4 Cell Balancing

The PAC2514X contains integrated cell balancing FETs for up to 20 cells.

#### Features

- Cell Balancing FETs for up to 20 cells
- Allows for discharge of individual cells
- Voltage ADC for sensing the voltage of each cell

#### 8.4.1 Block Diagram



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### Functional Description

The integrated cell balancing contains FETs for up to 20 battery cells. Cell balancing can be performed through firmware programming. Each of the battery cell voltages from the VB[1..20] pins are available for sampling from the 16-bit ADC.

Adjacent cells should not be balanced at the same time. In the event that too many cells are being balanced at the same time and Thermal protection occurs, then the cell balancing will be shut down first.

Only enabled cells can be balanced. Each independent cell can be enabled by setting their respective CENx enable bit. This can be accomplished by writing to the SOC.CELLEN1.CENx, SOC.CELLEN2.CENx and SOC.CELLEN3.CENx registers.

To start the cell balancing process, simply set the respective VBx cell balancing enable bit. This can be accomplished by writing to the SOC.CFGCB1, SOC.CFGCB2 and SOC.CFGCB3 registers.

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## 8.5 AFE MUX and EMUX

. The ADC MUX is an 8-channel MUX local to the ADC on the MCU that is directly controlled either by registers in the MCU, or automatically by the ADC sequencer.

To configure the ADC for manual mode, set **ADCCTL.MODE** to 000b. When the ADC is in manual mode, **ADCCTL** may be used to enable and configure the ADC, including selecting the MUX channel that is used for sampling.

To configure the ADC for sequencer mode, set one of the sequencer modes by setting **ADCCTL.MODE** to 001b to 111b. In one of the sequencer modes, the operation of the ADC and ADC MUX are done automatically in hardware according the sequencer and ADC configuration.

There are 5 external pins and one internal ADC channel that may be configured for ADC analog input that are shown in the table below.

Table 8-2 ADC MUX channels

ADC Channel	MCU I/O PIN	Description
AD0	PG7	Internally Connected to AFE MUX
AD2	PC2	Package pin
AD3	PC3	Package pin
AD4	PC4	Package pin
AD5	PC5	Package pin
AD6	PC6	Package pin

The AD0 channel is always used for analog input from the AFE and is connected to the AFE MUX on MCU internal pin PG7. ADC channels AD<6:2> are directly connected to package pins on the device as shown in the table above.

To use any of these channels as analog inputs to the ADC the IO controller configuration for these pins must be configured as analog input. See the section on the IO controller for more information on IO configuration.

### 8.5.1 AFE MUX

The AFE MUX resides in the AFE and is used to select analog signals found in the CAFE.

The MUX select for the AFE MUX may also be controlled directly through the SOC registers or through the EMUX from the MCU's ADC sequencer.

When the ADC is configured for manual mode, the EMUX enable function in the AFE should be disabled. To select the AFE MUX channel using the SOC registers, set **SOC.SHCFG1.EMUXEN** to 0b (disabled). The MUX channel may be selected from **SOC.SHCFG2.MUXA**.

When the ADC is configured for ADC sequencer mode, the EMUX enable function in the AFE should be enabled. To select the AFE MUX channel using the EMUX set **SOC.SHCFG1.EMUXEN** to 1b (enabled). The AFE MUX channel may be selected from the EMUX data sent from the ADC sequencer.

The channels available on the AFE MUX are shown in the table below.



Table 8-3 AFE MUX channels

AFE MUX Channel	Value	Description
VCORE	0	VCORE
VCORE	1	VCORE / 2.5
VDDA	2	VDDA / 2.5
VCCIO	3	VCCIO / 2.5
VSYS	4	VSYS / 2.5
HVB_ISENSE	5	Current Sense High Voltage Buck
VPTAT	6	Internal temperature sensor (VPTAT).
VP	7	VP / 10
VREF	8	VREF / 2
FUSE	9	FUSE / 10
CHG	10	CHG / 50
DSG	11	DSG / 50
BAT	12	BAT / 50
AIO0A	13	Analog Input/Output 0 Amp Output
LOADDET	14	Load Detection Voltage
SCPDAC	15	SCP DAC Voltage
OCCDAC	16	OCC DAC Voltage
OCDDAC	17	OCD DAC Voltage
BATOVDAC	18	BAT Over Voltage DAC
VIN	19	VIN / 50
PACK+	20	PACK+ / 50
VCP	21	VCP / 50

For more information on the configuration and use of the EMUX, see the section below.

### 8.5.2 EMUX

The EMUX is a dedicated high-speed, low-latency serial interface to control the AFE MUX using the ADC sequencing engine.

To enable the EMUX, set the **SOC.AFEMUXCTL.EMUX\_EN** = 1b. This will enable the ADC sequencer to command the control of the AFE MUX using the EMUX data sent by the sequencer.

The format of the EMUX command used to control the AFE MUX is shown below. The EMUX data is transmitted MSb first.



Register 8-49. **EMUX Packet Structure**

BIT	NAME	DESCRIPTION
7	BIT7	Bit 7 should be set to 0b
6	BIT6	Bit 6 should be set to 1b
5	BIT5	Bit 5 should be set to 0b
4:0	AFEMUXSEL	AFE MUX Channel Selector:  0 = VCORE 1 = VCORE / 2.5 2 = VDDA / 2.5 3 = VCCIO / 2.5 4 = VSYS / 2.5 5 = HVB_ISENSE 6 = VPTAT 7 = VP / 10 8 = VREF / 2 9 = FUSE / 10 10 = CHG / 50 11 = DSG / 50 12 = BAT / 50 13 = AIO0A 14 = LOADDET 15 = SCPDAC 16 = OCCDAC 17 = OCDDAC 18 = BATOVDAC 19 = VIN / 50 20 = PACK+ / 50 21 = VCP / 50

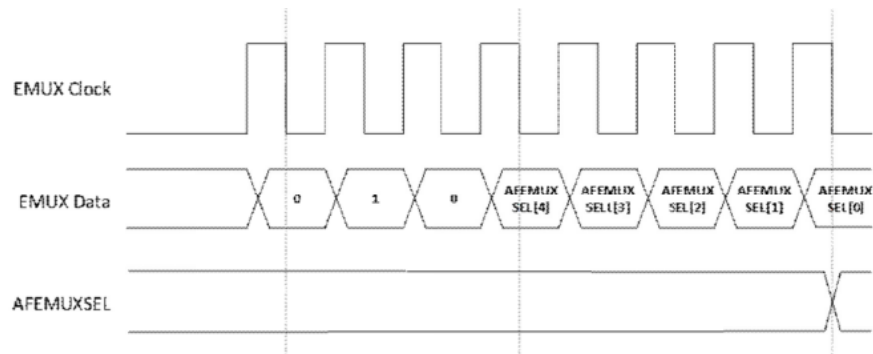
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8.5.2.1 The EMUX data is written on this bus MSb first from the ADC sequencer. See the timing diagram below.

Figure 9-1 EMUX Timing Diagram



Bits [7:5] should contain 010b so that the EMUX controller will recognize the EMUX data as valid.

At the 8<sup>th</sup> EMUX clock falling edge, the AFE will read the AFEMUXSEL[4:0] data. At this time the AFE will set the AFE MUX to the proper channel, according to this data.

### 8.5.3 High Voltage Signal EMUX Correction

The signals PACK+/50, VIN/50 and BAT/50 have a compensation coefficient available in INFO FLASH that can be used to obtain improve accurate measurements. The correction parameters will be stored in INFO FLASH and will indicate the compensation factor.

VM is corrected value, V2 = 80V, V1 = 20V; VMS2 = Stored Value in INFO-2, VMS1 = Stored Value in INFO-2; VADC is count from ADC; VADCREf = stored value in INFO-2

$$VM=(V2-V1) / (VMS2-VMS1) * [VADC*VADCREf/4095-VMS1] + V1$$

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## 9 ARM® CORTEX M4F REFERENCE

The PAC2514X contains an Arm® Cortex®-M4F MCU. The Arm® Cortex®-M4F has several configurable options.

For detailed information on the MCU and Digital Peripherals in the PAC2514X, see the [PAC55XX Family User Guide](#).

The options listed below are present on the PAC55XX/PAC25XXX family of controllers:

- IEEE754 single-precision Floating Point Unit
- Memory Protection Unit (MPU) included
- Number of interrupt priorities: 8 (3-bit priority)
- Wakeup Interrupt Controller (WIC) included
- Sleep Mode power-saving included
- Little Endian configuration
- 24-bit SysTick timer included
- Embedded Trace Module (ETM) included
  - Instruction trace only

ARM provides a full set of documentation for the Arm® Cortex®-M4F MCU.

You can retrieve the full set of documentation on the Arm® Cortex®-M4F from here:

<http://infocenter.arm.com/help/index.jsp>

The documents that are the most important are:

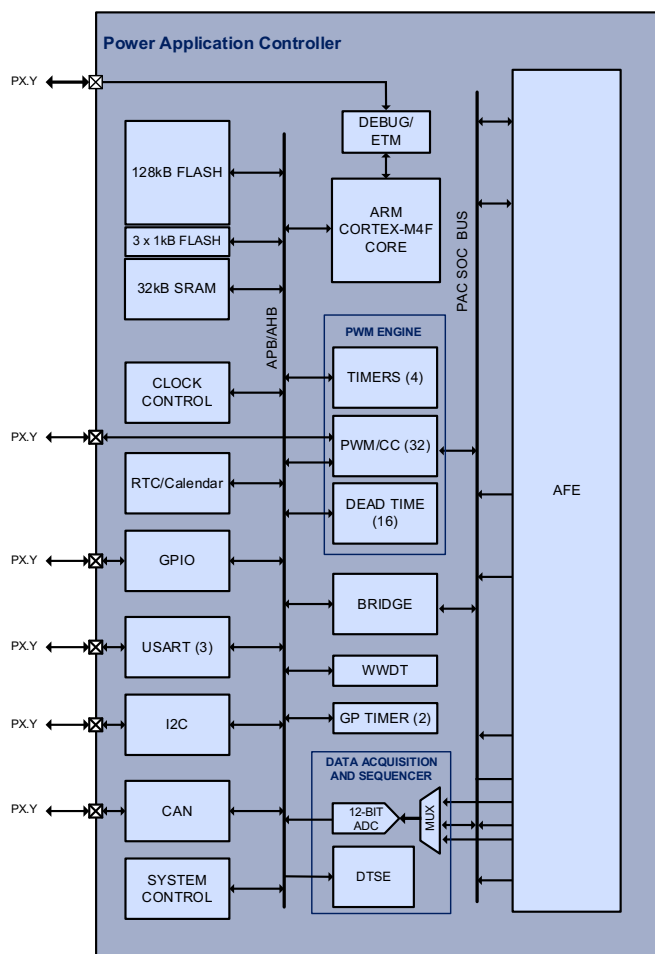
- [Arm® Cortex®-M4 Processor Technical Reference Manual](#)
- [Coresight ETM-M4 Technical Reference Manual](#)

The [Arm® Cortex®-M4 Processor Technical Reference Manual](#) contains documentation for the Arm® Cortex®-M4 processor, the programmer's model, instruction set, registers, memory map, floating point multimedia, trace and debug support.

The [Arm® Cortex®-M4 Devices Generic User Guide](#) contains documentation for the Arm® Cortex®-M4F's Embedded Trace Macrocell™

## 9.1 PAC25xxx Architecture

Figure 9-1 Top Level Block Diagram



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## 9.2 SYSTEM AND CLOCK CONTROL (SCC)

### 9.2.1 Overview

The System and Clock Control (SCC) module controls the clock and other system components for the PAC55XX family of devices.

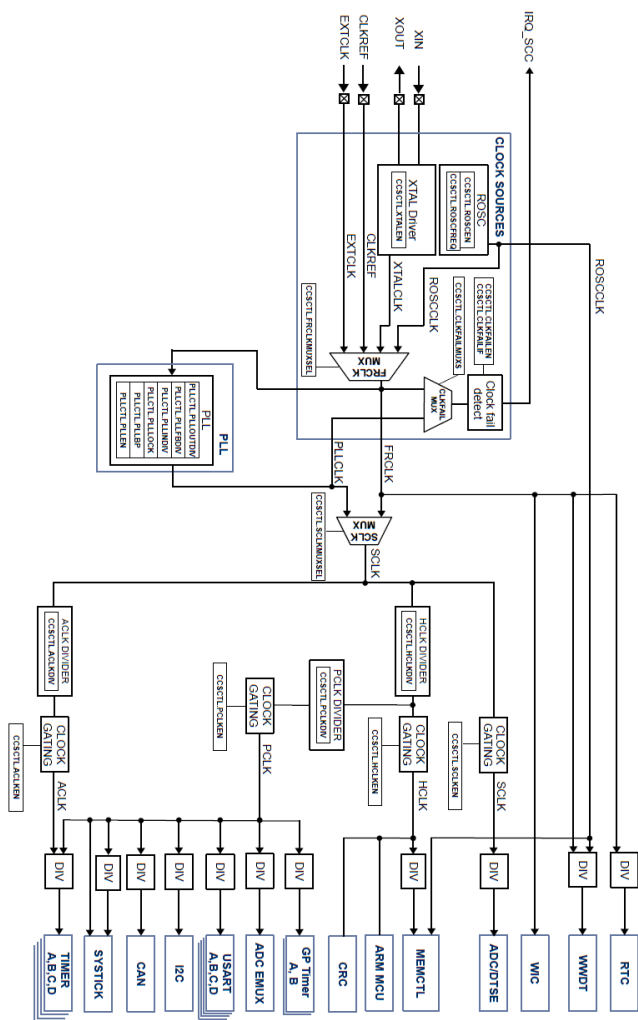
### 9.2.2 Features

- Clock Control System (CCS):
  - 4 clock sources:
    - 4MHz internally generated 2% RC oscillator
    - 16MHz Ring Oscillator
    - External clock input for up to 20MHz external clock sources
    - Crystal driver for up to 10MHz crystals or ceramic resonators<sup>2</sup>
  - 300MHz PLL
  - 5 system clocks for peripherals with programmable clock dividers
  - Clock gating for low-power mode support
- USART Mode Control
  - Selects between SSP or UART modes
- Interrupt Vector Table
  - 32 interrupts
  - 8 levels of priority

---

<sup>2</sup> Note that only some devices contain the pins for the crystal input and output.

Figure 9-2 Clock Control Block Diagram



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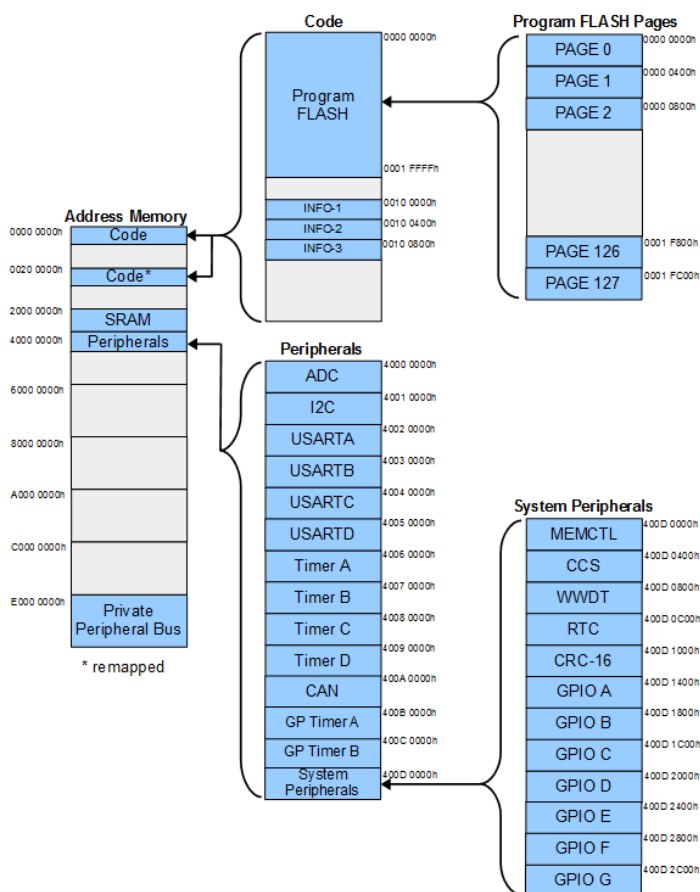
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### 9.3 MCU MEMORY MAP

Figure 9-3 High Level Memory



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### 9.4 INFO-2 Flash Register Map

The ADC channels that are available on the PAC2514X are shown in the table below.

Table 9-1 PAC2514X INFO-2 Flash Register Map

Address	OFFSET				Description
	3	2	1	0	
0010 0400h	RESERVED				
0010 0404h	RESERVED				
0010 0408h	PACDIR				ID of device
0010 040Ch	RESERVED				
0010 0410h	RESERVED				
0010 0414h	ADCOFFSET				ADCOFFSET is calculated from equation: ADCOFF = ROUND(ADCOFFSET*65535,0) and convert to signed number to store Ex: -38.4441 => 0xFFD98E78
0010 0418h	ADCGAIN				ADCGAIN is calculated from the equation: ADCGAIN = ROUND(ADC_GAIN*65535,0) to store Ex: 1609.916 => 0x0649E438
0010 041Ch	FTTEMP		TEMPS		ADC Result of TEMPS at room temp, it's VPTAT voltage. Ex: 0x0859
0010 0420h	RESERVED			SECEN	Security Code
0010 0424h	MAXADDR				Optional setting to restrict Flash memory size available
0010 0428h	ROSC				ROSC@8M/10*1e6. Example: 0x1E73AF is 1995695Hz
0010 042Ch	CLKREF				CLKREF is measured CLK_Post=CLKREF/40 Value of CLKREF= FCK_Post*40*1000 Example: 99.5609*40*1000=3982436Hz
0010 0430h	RESERVED				
0010 0434h	VREF		RESERVED		Value of ADCREF_Post= round(ADCREF_Post) in mV with 1 dig. Example: 25014 is 2.5014V
0010 0438h	RESERVED		VPTAT		Value of VPTAT= round(VPTAT) in mV with 1 dig. Example: 12907 is 1.2907V
0010 043Ch	SWDFUSE				Optional setting to restrict SWD communication
0010 0440h – 044Ch	RESERVED				
0010 0450h – 045Ch	"PAC2514X"				Code in ASCII
0010 0460h	VB01ADCAL VB01 Gain and Offset Calibration				Offset calibration of VADC_gain_10 and offset_10 to have SCLED_GAIN and SCALE_DELTA
0010 0464h	VB02ADCAL VB02 Gain and Offset Calibration				
0010 0468h	VB03ADCAL VB03 Gain and Offset Calibration				
0010 046Ch	VB04ADCAL VB04 Gain and Offset Calibration				
0010 0470h	VB05ADCAL VB05 Gain and Offset Calibration				
0010 0474h	VB06ADCAL VB06 Gain and Offset Calibration				
0010 0478h	VB07ADCAL VB07 Gain and Offset Calibration				
0010 047Ch	VB08ADCAL VB08 Gain and Offset Calibration				
0010 0480h	VB09ADCAL VB09 Gain and Offset Calibration				
0010 0484h	VB10ADCAL VB10 Gain and Offset Calibration				
0010 0488h	VB11ADCAL VB11 Gain and Offset Calibration				

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0010 048Ch	VB12ADCAL VB12 Gain and Offset Calibration		
0010 0490h	VB13ADCAL VB13 Gain and Offset Calibration		
0010 0494h	VB14ADCAL VB14 Gain and Offset Calibration		
0010 0498h	VB15ADCAL VB15 Gain and Offset Calibration		
0010 049Ch	VB16ADCAL VB16 Gain and Offset Calibration		
0010 04A0h	VB17ADCAL VB17 Gain and Offset Calibration		
0010 04A4h	VB18ADCAL VB18 Gain and Offset Calibration		
0010 04A8h	VB19ADCAL VB19 Gain and Offset Calibration		
0010 04ACh	VB20ADCAL VB20 Gain and Offset Calibration		
0010 04B0h	IADCAL1X_Gain		Gain calibration of IADC_1x, iadc1x_gain
0010 04B4h	IADCAL1X_Offset		Offset calibration of IADC_1x, iadc1x_offset
0010 04B8h – 04ECh	IADCAL#X_Gain, IADCAL#X_Offset		# = 2,4,8,16,32,64,128
0010 04F0h	VBATVMS2	VBATVMS1	Scaled VBAT Sensing voltage measured in mV when BAT(VMS1)=20V & BAT(VMS2)=80V Example: value of 400mV stored as 0x0190 and 1600mV stored as 0x0640
0010 04F4h	VINVMS2	VINVMS1	Scaled VIN Sensing voltage measured in mV when VIN=20V & 80V
0010 04F8h	VPCKVMS2	VPCKVMS1	Scaled VPACK+ Sensing voltage measured in mV when VPACK+=20V & 80V
0010 04FCh – 07EF	RESERVED		
0010 07F0h	CRC1_CLONE	CRC1	16-bit CRC and Checksum from INFO1
0010 07F4h	CRC2_CLONE	CRC2	16-bit CRC and Checksum of Reg. 40-7E of INFO2
0010 07F8h – 07FFh	RESERVED		

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## 10 Revision History

Revision	DESCRIPTION
1.0	PAC2514X Preview Release
1.1	Align format to PAC22140, Updated BATDACOV/2
1.2	Updated EMUX table; ASPD paragraph and add block diagram
1.3	Updated bookmarks, PA0, IMUX comment, added INFO Flash data, Includes all devices PAC25140, PAC25140N, PAC25141N
1.4	Corrected error in the default buck frequency setting from 200 kHz to 100 kHz.

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