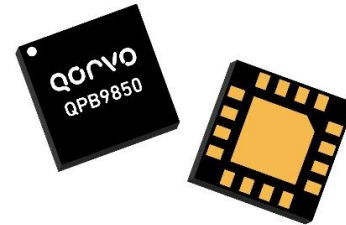


Product Overview

The QPB9850 is a highly integrated front-end module targeted for 5G TDD systems. The switch LNA module integrates an LNA with a high-power handling switch which can be used as a failsafe path to termination when radio is in transmitting mode. LNAs can also be powered down during Tx mode via SW control pin on the module.

The QPB9850 provides 34 dB of gain at 3.6 GHz with 1.1 dB noise figure while providing high linearity performance.

The QPB9850 is packaged in a RoHS-compliant, compact 3 mm x 3 mm LGA package. The switch LNA module is targeted for 5G wireless infrastructure applications configured for TDD-based architectures.

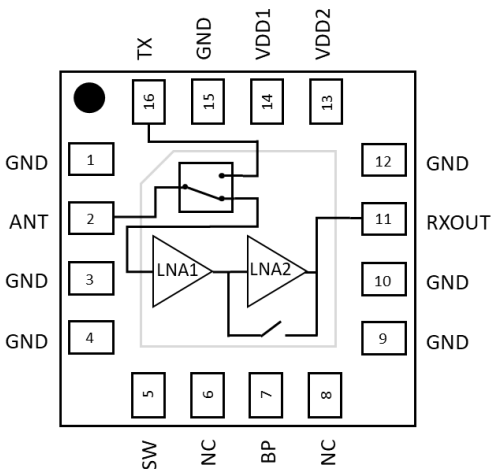


16 Pin 3 mm x 3 mm Leadless LGA Package

Key Features

- 2300 – 5000 MHz Frequency Range
- 2nd stage LNA with integrated bypass mode
- Ability to turn LNA and bypass mode OFF
- 1.1 dB typical NF at 3.6 GHz
- 34 dB gain at 3.6 GHz
- 36 dBm max input Power in Tx mode.

Functional Block Diagram



Top View

Applications

- Wireless Infrastructure
- 5G Massive MIMO systems
- TDD-based architectures

Ordering Information

Part No.	Description
QPB9850TR7	2500 pcs on 7" reel (standard)
QPB9850EVB01	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
Supply Voltage (VDD1, VDD2)	6 V
Max. Pin at ANT, Rx mode, CW, T=25°C	+20 dBm
Max. Pin at ANT, Tx mode, T=25°C, ≤10 sec (Avg, 9dB PAR, 8.8ms frame ≤ 88% DC)	+39 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Supply Voltage (VDD1, VDD2)	+3.3	+5	+5.5	V
ANT Pin, Rx mode, +25°C, > 10 yrs. (Avg, 9dB PAR, 8.8ms frame ≤ 88% DC)			+36	dBm
T _{CASE}	-40		+110	°C
T _J (Tx Path), MTTF > 1e5 hours			125	°C
T _J (Rx Path), MTTF > 1e6 hours			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions. Application of conditions to the device outside the Recommended Operating Conditions may reduce device reliability and performance.

Electrical Specifications

Test conditions unless otherwise noted: VDD1, VDD2 = +5V, Temp = +25 °C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
Operating Frequency		2300		5000	MHz
Test Frequency			3600		MHz
Gain	High Gain Mode		34		dB
	Low Gain Mode		16.5		dB
Gain Flatness	High Gain Mode, Any 200 MHz BW in band		0.5		dB
Noise Figure ⁽¹⁾	High Gain Mode, input trace loss deducted		1.1		dB
	Low Gain Mode, input trace loss deducted		1.1		dB
Output IP3	High Gain Mode, P _{out} = -3dBm/tone, Δf = 1MHz		31		dBm
	Low Gain Mode, P _{out} = -3dBm/tone, Δf = 1MHz		31		dBm
Output P1dB	High Gain Mode		18		dBm
	Low Gain Mode		17		dBm
Input Return Loss	Rx Mode		13		dB
	Tx Mode		15		dB
Output Return Loss	Rx Mode		13		dB
	Tx Mode		15		dB
Reverse Isolation	Rx High Gain Mode, RXOUT to ANT	40	50		dB
	Rx Low Gain Mode, RXOUT to ANT	20	32		dB
Switch Insertion Loss ⁽¹⁾	Tx Mode, ANT to TX		0.5		dB
Thermal Resistance, θ _{Jc}	Rx Mode (T _J to T _{CASE})		72.5		°C/W
	Tx Mode (T _J to T _{CASE})		178.1		°C/W

Notes:

- Trace loss deducted.

Electrical Specifications (Continued)

Test conditions unless otherwise noted: VDD1, VDD2 = +5V, Temp = +25 °C, 50 Ω system.

Parameter	Conditions	Min	Typ	Max	Units
TX-RXOUT Isolation	Tx Mode	30	48		dB
Harmonic, 2nd order	High Gain Mode, Pout -3dBm		-50		dBc
Harmonic, 3rd order	High Gain Mode, Pout -3dBm		-100		dBc
Switching time ⁽¹⁾	Tx to Rx Mode ANT to RXOUT Path		480		nsec
	Rx to Tx Mode ANT to TX Path		540		nsec
Control Voltage, V _{SW} , V _{BP}	V _{IH}	1.17		3.6	V
	V _{IL}	0		0.63	V
Current, I _D	High Gain Mode		90		mA
	Low Gain Mode		54		mA

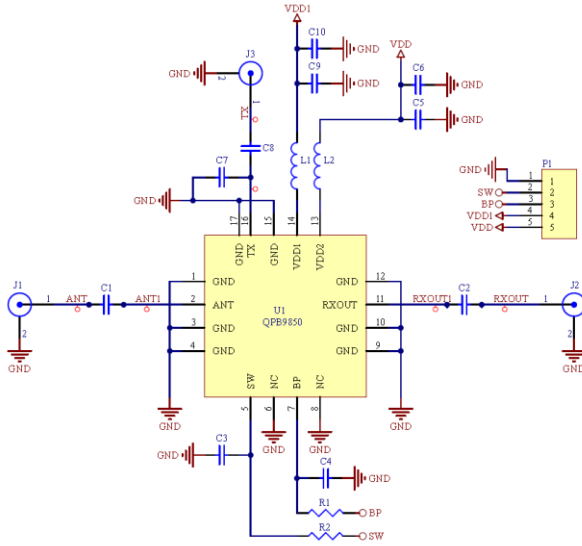
Notes:

- Control voltage thresholds to 10/90% steady state RF output of the active path.

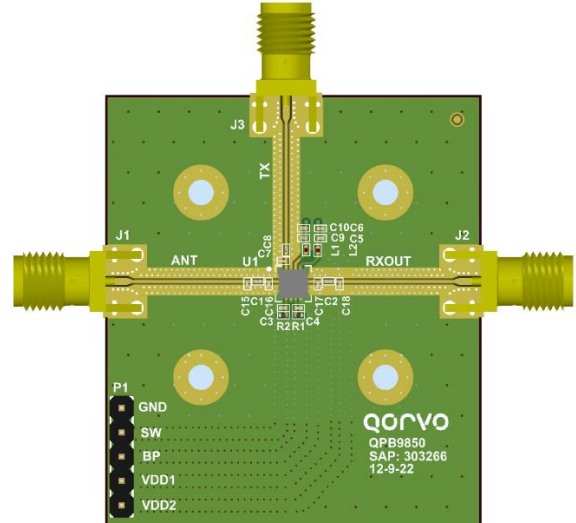
Control Logic

Logic	Switch Position & LNA State	SW	BP
00	Rx, LNA High Gain Mode (LNA1 ON, LNA2 ON - Bypass OFF)	0	0
01	Rx, LNA Low Gain Mode (LNA1 ON, LNA2 OFF - Bypass ON)	0	1
10	Tx, ANT to RFOUT High Isolation Mode (LNA1 OFF, LNA2 OFF - Bypass OFF)	1	0
11	Rx, ANT to RFOUT Low Isolation Mode (LNA1 OFF, LNA2 OFF - Bypass ON)	1	1

Evaluation Board and Schematic – QPB9850EVB01



EVB Schematic



EVB Top View

Bill of Material – QPB9850EVB01

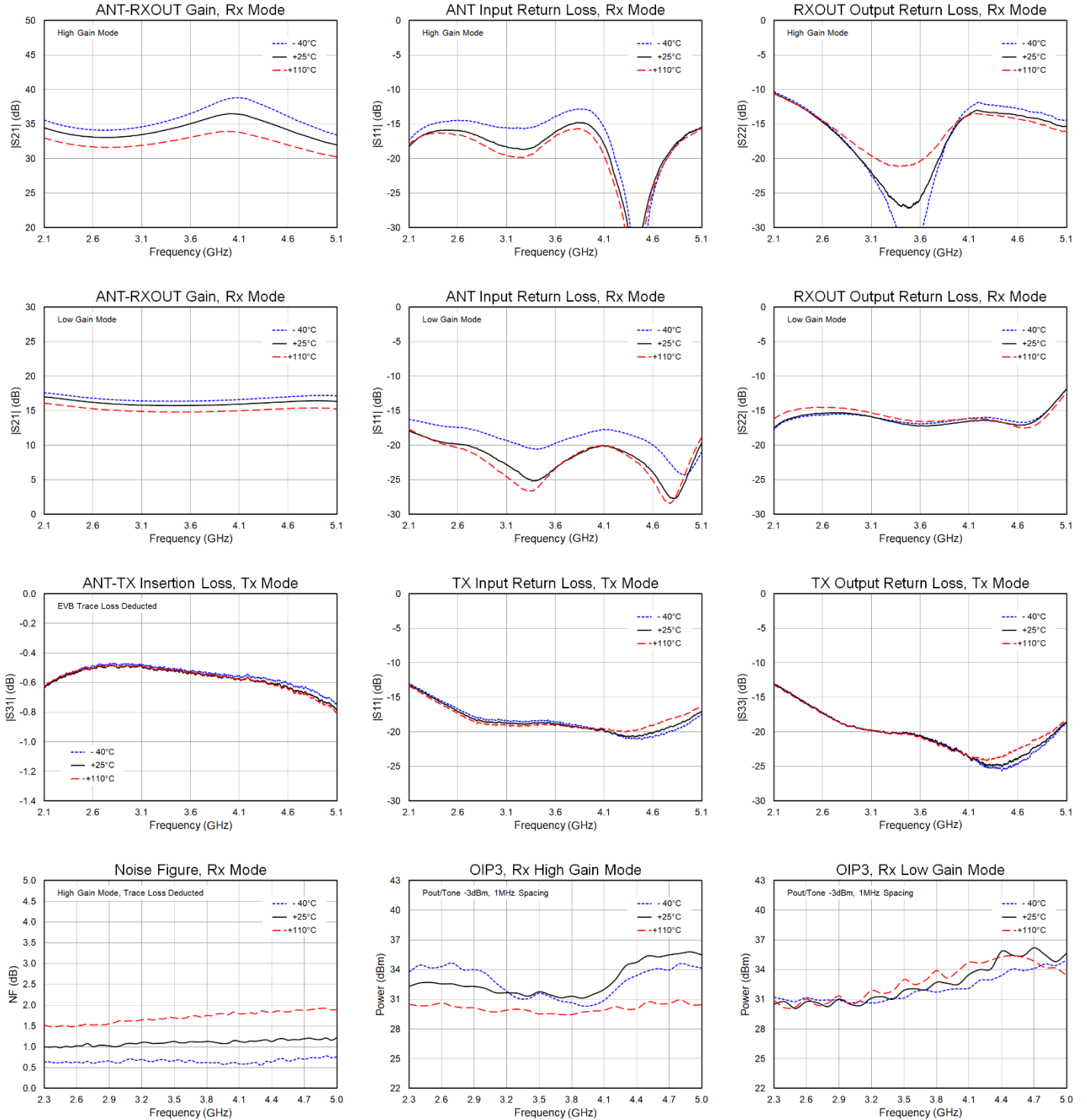
Reference Des.	Value	Description	Manuf.	Part Number
U1	-	2.3 – 5.0 GHz Single Channel Switch-LNA Module	Qorvo	QPB9362
C1, C2, C8, C11 ~ C14	10 pF	CAP, 10 pF, 2%, 25V, Hi-QC0G, 0201	Murata	GJM0335C1E100GB01D
C3, C4	18 pF	CAP, 18pF, 5%, 25V, HI-Q, 0201	Murata	GJM0335C1E180JB01D
C5, C9	0.01 µF	CAP, 0.01uF, 10%, 16V, X5R, 0201	Murata	GRM033R61C103KA12D
C6, C10	0.47 µF	CAP, 0.47 µF, 10%, 10V, X6S, 0201	Taiyo Yuden	LMK063BC6474KPLF
C7	0.3 pF	CAP, 0.3 pF, ±0.05 pF, 10V, Hi-Q, 0402	Murata	GJM0335C1ER30WB01D
L1, L2, R1, R2 (1)	0 Ω	RES, 0 Ω, 1/20W, 0201	Delta	PFR03S-000-XNH-87
J1, J2, J3	SMA	CON, SMA, EL FLT VIPER MAT-21-1038	AMPHENOL	901-10425
P1	-	CON, HER RT-ANG, 1x5, 0.100", T/H	SAMTEC	TSW-105-08-G-S-RA

Notes:

1. For system implementation, non-zero ohm recommended to R1 and R2 as damping resistors

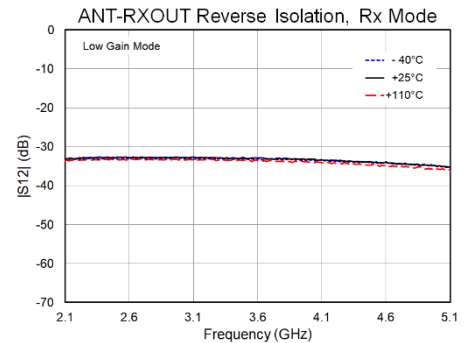
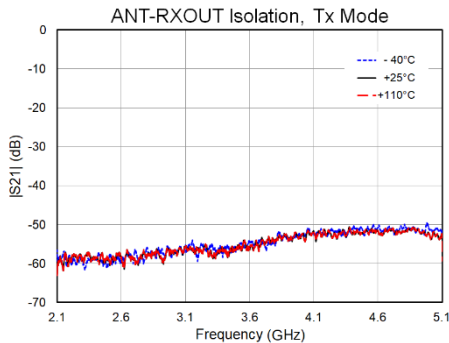
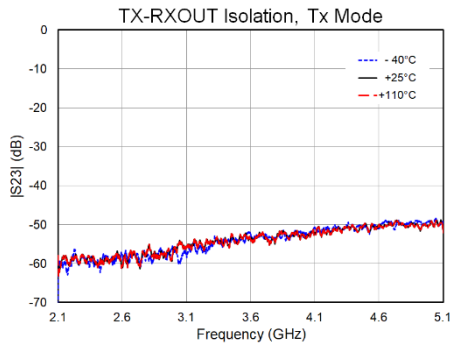
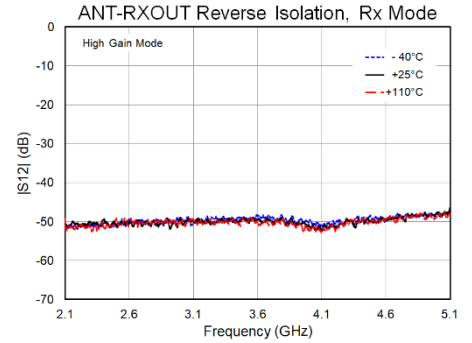
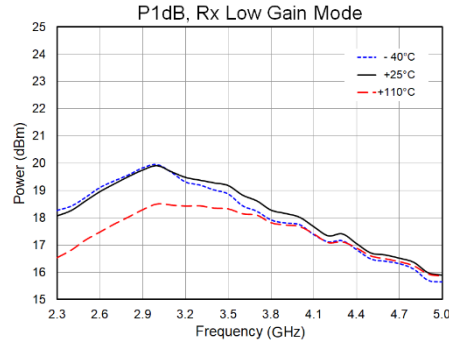
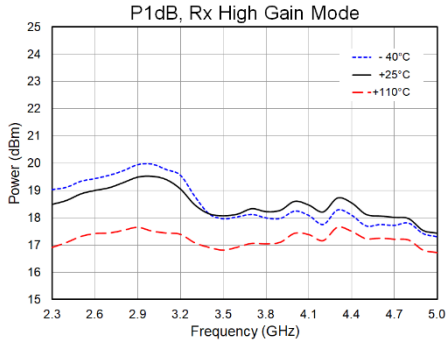
Performance Plots – QPB9850EVB01

Test conditions unless otherwise noted: VDD1, VDD2 = +5.0 V, Temp = +25°C, on Qorvo EVB.



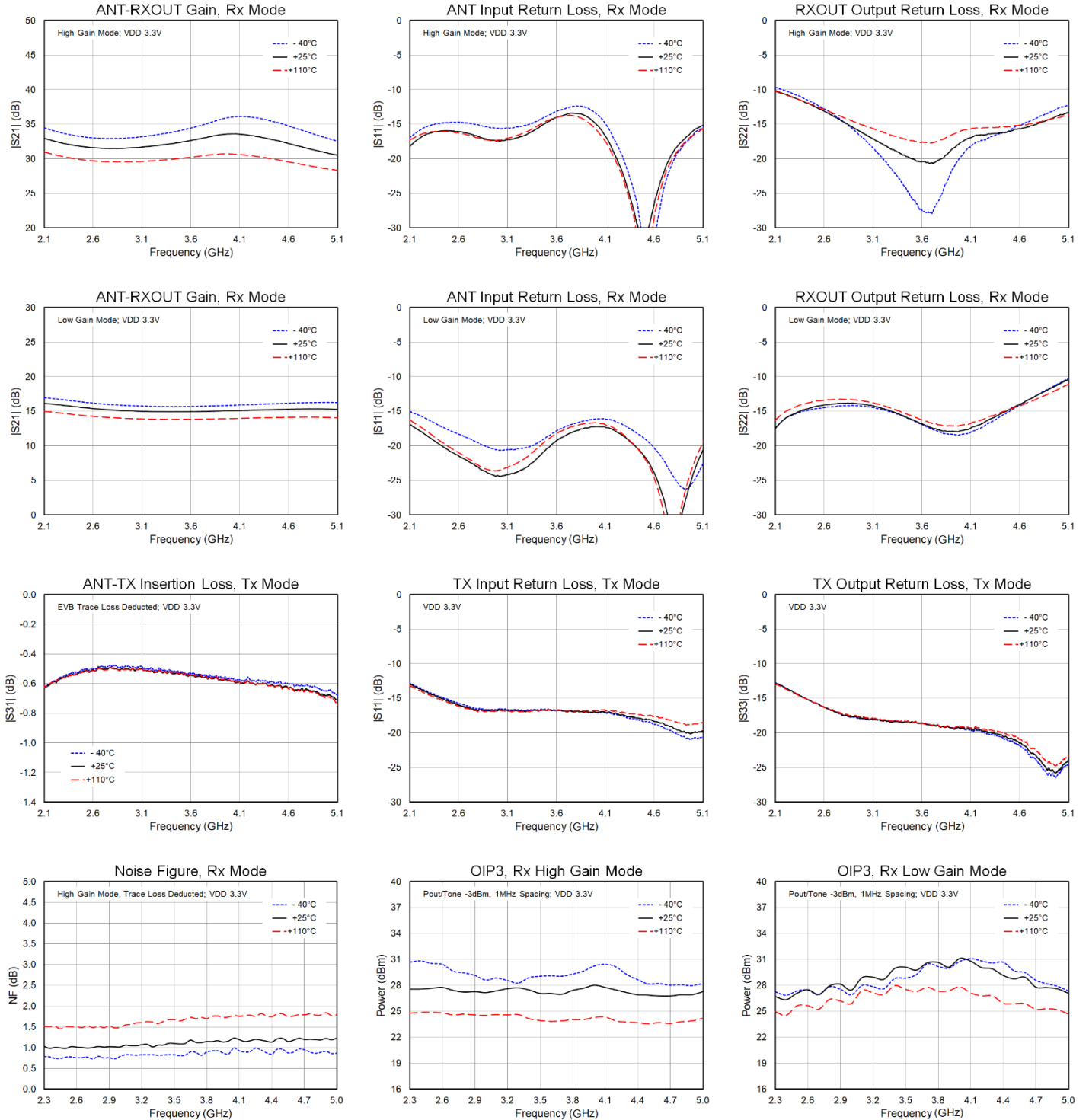
Performance Plots – QPB9850EVB01

Test conditions unless otherwise noted: VDD1, VDD2 = +5.0 V, Temp = +25°C, on Qorvo EVB.



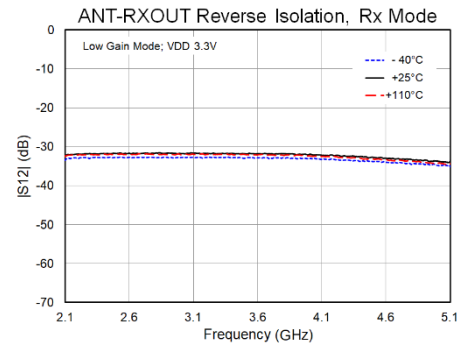
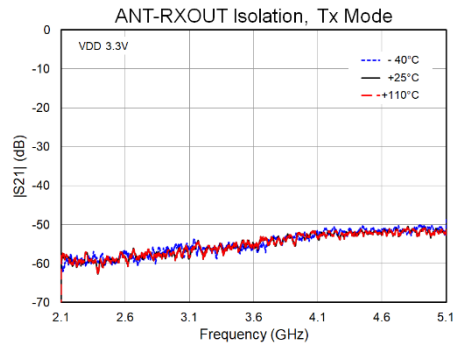
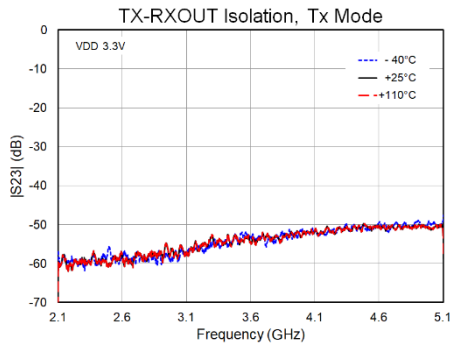
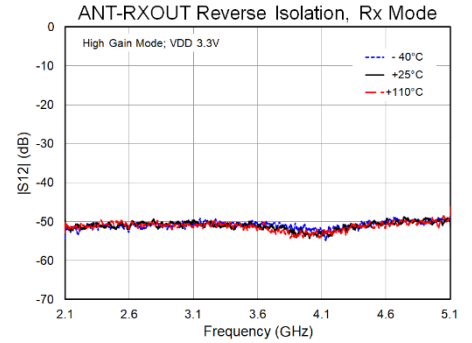
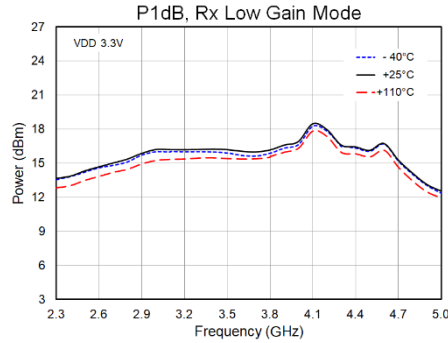
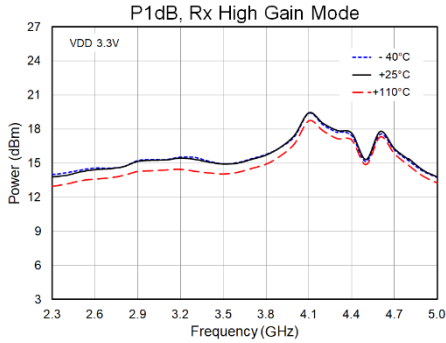
Performance Plots – VDD 3.3V

Test conditions unless otherwise noted: VDD1, VDD2 = +3.3 V, Temp = +25°C, on Qorvo EVB.

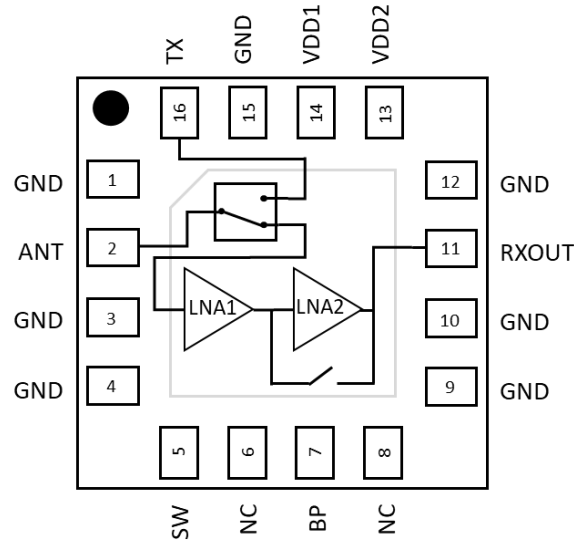


Performance Plots – VDD 3.3V

Test conditions unless otherwise noted: VDD1, VDD2 = +3.3 V, Temp = +25°C, on Qorvo EVB.



Pin Configuration and Description

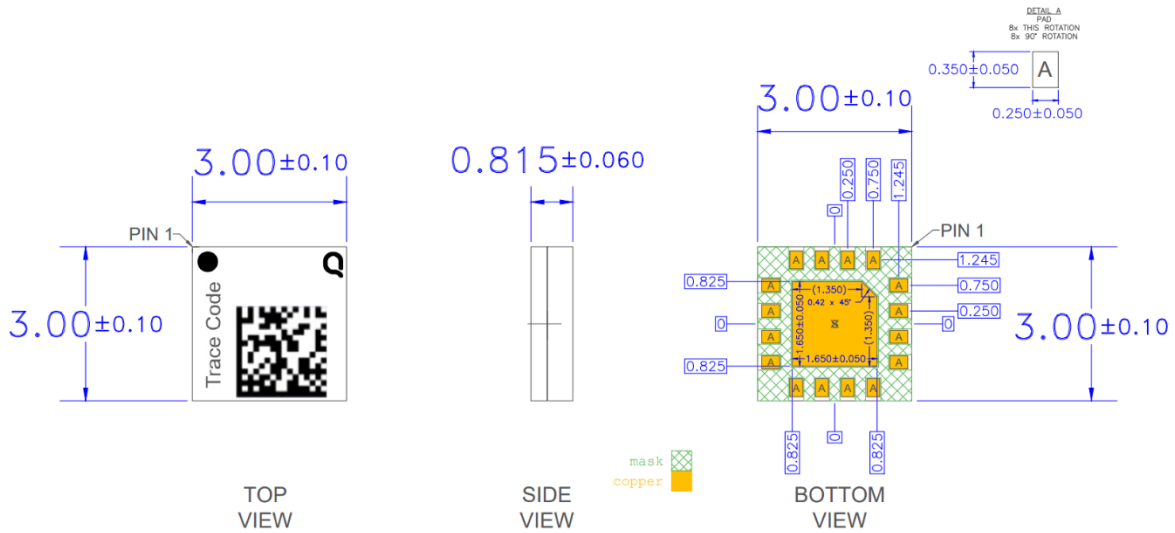


Top View

Pin No.	Label	Description
1, 3, 4, 9, 10, 12, 15	GND	RF/DC ground connection.
2	ANT	RF input.
5	SW	Mode SW control input for Rx and Tx modes
6, 8	NC	Not connected internally.
7	BP	Bypass control input for LNA2
11	RXOUT	RF output.
13	VDD2	LNA2 DC supply input, external RF choke is required.
14	VDD1	LNA1 DC supply input, external RF choke is required.
Backside Paddle	GND	RF/DC Ground. Use recommended via hole pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

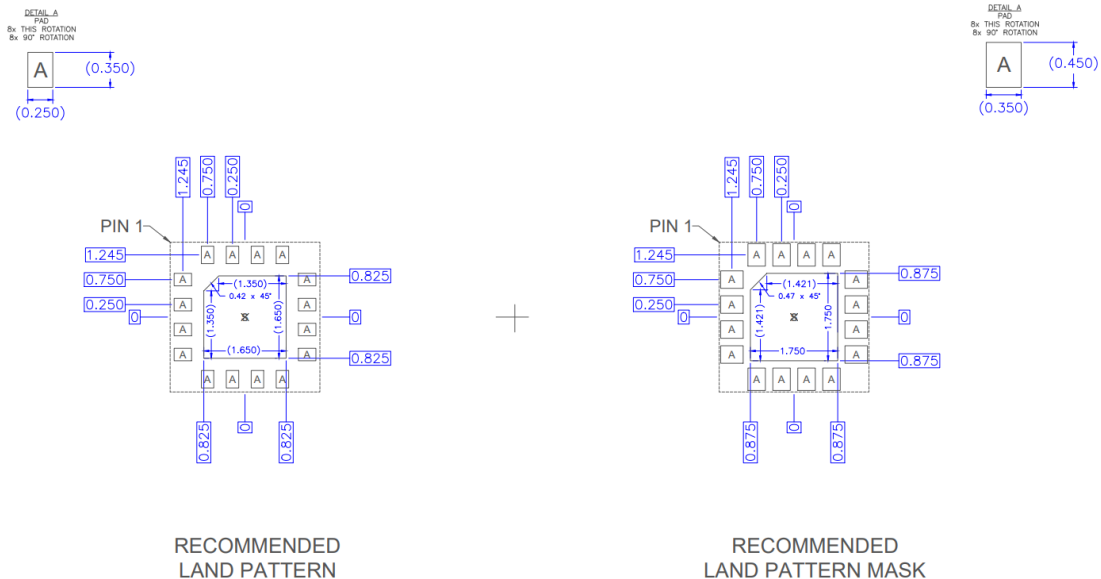
Package Marking and Dimensions

- Marking: ● – Pin 1 Indicator
Trace Code – Assigned by Sub-Contractor
2DID – Device Information



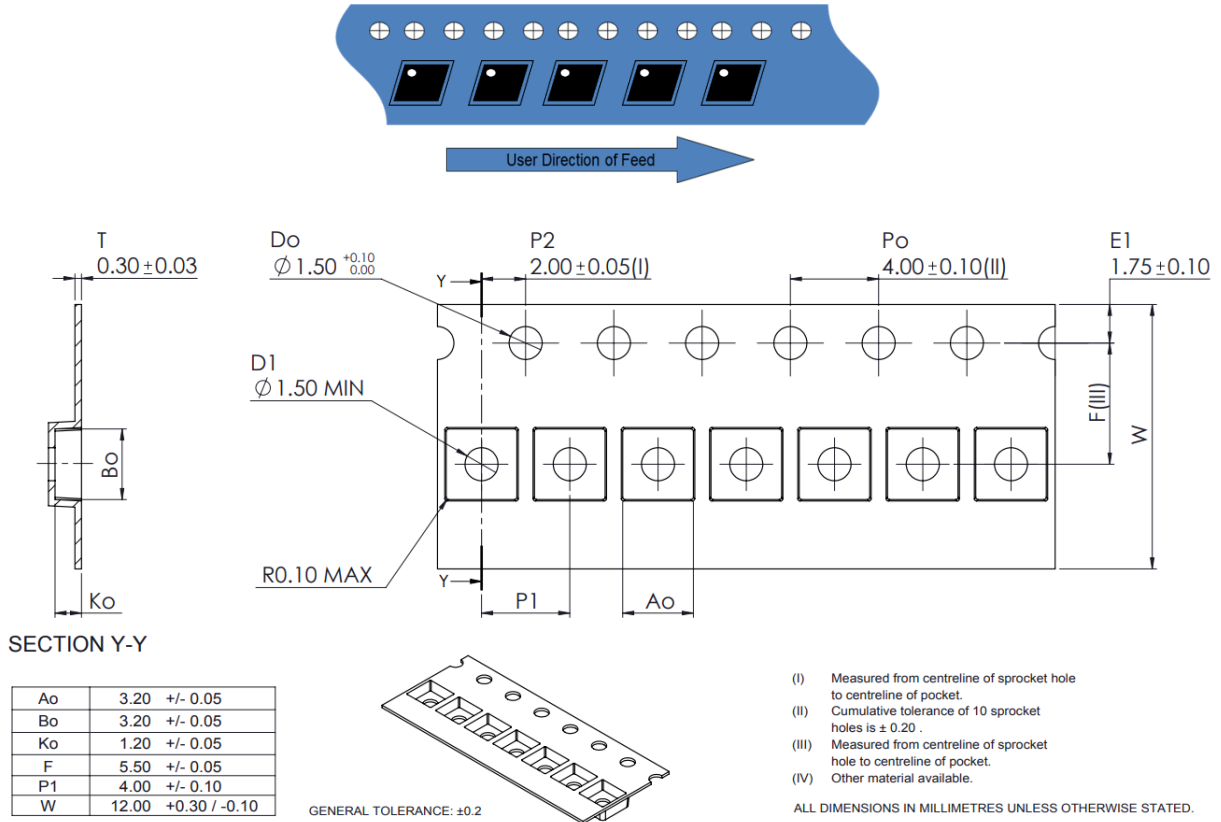
- Notes:
1. All dimensions are in mm. Angles are in degrees.
 2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
 3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



- Notes:
1. Use at least 9 via holes on the ground paddle. Ground via holes are critical for the performance and stability of this device. Via holes should use a 0.35 mm (#80 / .0135") diameter drill and have a final plated through diameter of $.25$ mm (.010").
 2. All dimensions are in mm. Angles are in degrees.
 3. A heat sink underneath the area of the PCB for the mounted device is recommended and add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

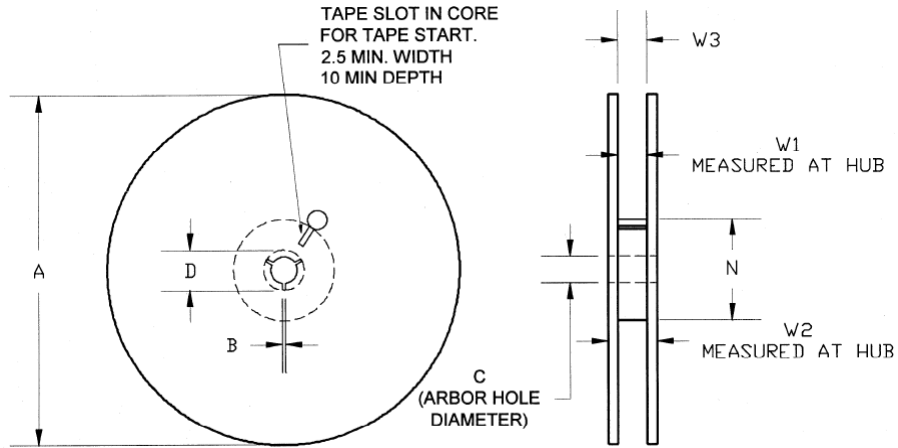
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.30
	Width	B0	0.209	5.30
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width (Reference Only)	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.00

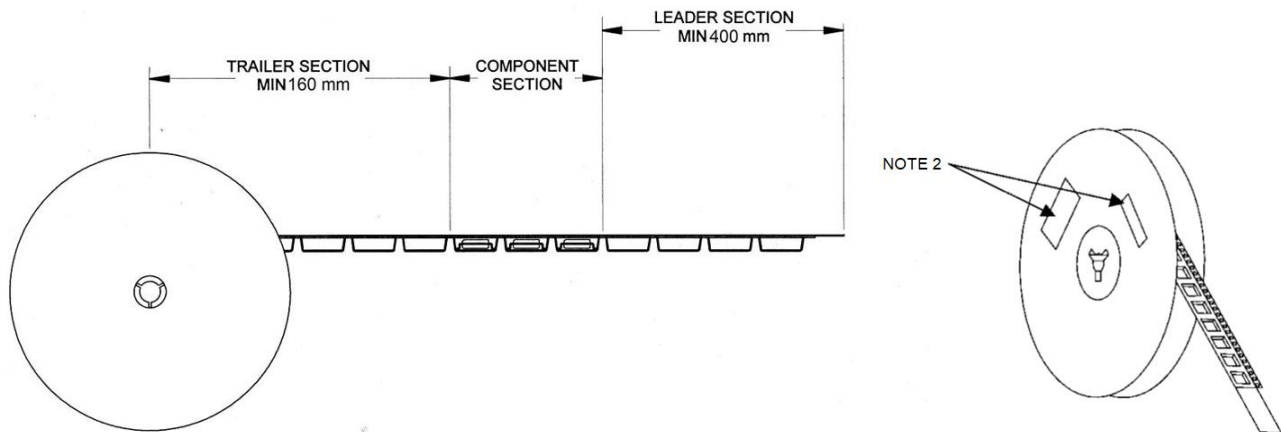
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



- Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
 2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ANSI / ESDA / JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	ANSI / ESDA / JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: NiPdAu (*Ni 0.40±0.10 μm; Pd 0.145±0.035 μm; Au 0.095±0.025 μm*)

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Tel: 1-844-890-8163

Web: www.qorvo.com

Email: customer.support@qorvo.com

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