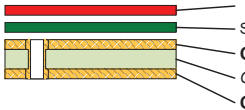
LAYER STACK LEGEND_SEE NOTE 3 FOR MATERIAL (COPPER THICKNESS IS @ FINISHED THICKNESS)



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	SILKSCREEN_TOP			Legend	GTO
Surface Material	SOLDERMASK_TOP	0.0004in	Solder Resist	Solder Mask	GTS
Copper	**METAL1_TOP**	**0.0018in**		**Signal**	**GTL**
Core		*0.0050in*	*ROGERS 6202*	*Dielectric*	
Copper	**METAL2_BOT**	**0.0018in**		**Signal**	**GBL**

Total thickness: 0.0090in

SUPPLIER MUST SEND EMAIL TO EVBHOLD@QORVO.COM IF JOB IS PLACED ON HOLD

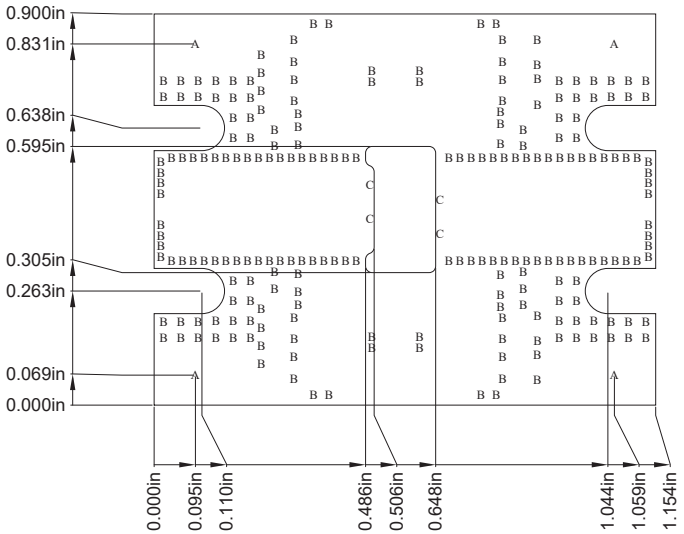
SUPPLIER SHALL SEND A COPY OF FINAL WORKING GERBERS TO CEADS@QORVO.COM

Drill Table (HOLE SIZES ARE DRILLED SIZE)

Symbol	Count	Hole Size	Plated	Drill Layer Pair
C	4	6.0mil(0.15mm)	Plated	METAL1_TOP - METAL2_BOT
B	221	15.0mil(0.38mm)	Plated	METAL1_TOP - METAL2_BOT
A	4	100.0mil(2.54mm)	Plated	METAL1_TOP - METAL2_BOT
	229 Total			

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
   FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
   GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. MATERIAL:
   NUMBER OF LAYERS: 2 LAYERS
   METAL 1 0.5oz. Rolled Copper (Plus plating)
   CORE 1: ROGERS 6202, .005in. THICK
   METAL 2 0.5oz. Rolled Copper (Plus plating)
   SOLDERMASK TOP: LPI (LIQUID PHOTO-IMAGEABLE), GREEN OR LDI (LASER DIRECT IMAGEABLE), GREEN. MAX FINISH THICKNESS OF SOLDERMASK TO BE 0.001in.
   SILKSCREEN TOP: HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK.
4. FINISH PLATING:
   A. METAL 1(TOP) AND METAL 2(BOTTOM):
   ENEPIG (ELECTROLESS NICKEL, ELECTROLESS PALLADIUM, IMMERSION GOLD)
   ENEPIG PLATING POST SOLDERMASK (ONLY ON OPENINGS)
5. FINISHED BOARD THICKNESS: (0.009in) ±.003IN.
6. COPPER IS PULLED BACK PER GERBER DATA FROM EDGE OF BOARD ON METAL 1 (TOP) AND METAL 2 (BOTTOM) EXCEPT IN AREA THAT IS EDGE PLATED PER INSTRUCTIONS ON PAGE 2.
7. TOLERANCE:
   A. PC BOARD OUTLINE: ±0.002in.
   B. POSITION OF INTERNAL CUTOUT RELATIVE TO PCB OUTLINE ± .002.
8. METALIZATION MUST BE FREE FROM CONTAMINATION AND DEBRIS.
9. BURRS SHALL NOT EXCEED 0.002in.
10. VIA PLATING/FILLING:
    ALL PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
11. SINGULATION: EXTERNAL OUTLINE AND INTERNAL CUTOUTS ARE TO BE COMPLETED VIA OPTICAL (LENZ) ROUTING OR LASER. LASER ROUTING IS AUTHORIZED ONLY IF IT YIELDS A WIRE-BONDABLE SURFACE ADJACENT TO THE LASER-SAWN EDGE.
12. FINISHED Cu THICKNESS TO BE .0018 ± .0005.
13. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
14. SOLDERMASK IN PLATED-THRU HOLES IS ACCEPTABLE AS LONG AS IT DOES NOT EXIST ON BACKSIDE OF BOARD.
15. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
16. NO VENDOR MARKING OR SERIALIZATION ALLOWED.
17. DELIVER BOARDS BAGGED AS SINGLES
18. NO ELECTRICAL TEST NEEDED.



REFERENCE NOTE: Uses TGA2222-4000[1]_CAL SAP No. 285104

* FOR MULTIPLE DRILL PROCESS JOBS SEE: *.DRL, *.DR1, *.DR2, etc.

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	SAP MATERIAL NUMBER: 291955		
	APPROVAL AND RELEASE RECORDS MAINTAINED IN PDE	DATE	
	DESIGNER: OMARRUFO	7/12/19	
	ENGR.: B.ZHAO		
INTERPRET DRAWING PER ANSI/ASME Y14.5 - 2009	PDE CONTROLLED		
THIRD ANGLE PROJECTION			
DO NOT SCALE DRAWING			

qorvo™

TITLE: QPA2226D EVALUATION PCB DESIGN PACKAGE

SIZE	DOCUMENT NUMBER:	PROTOTYPE INSTANCE:	REV.
B	QPA2226D-4000	N/A	A

SHEET 1 OF 7 | CAD: ALTIUM DESIGNER | SCALE: 2:1

Current Date & Time: 8/1/2019 5:51 PM

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