

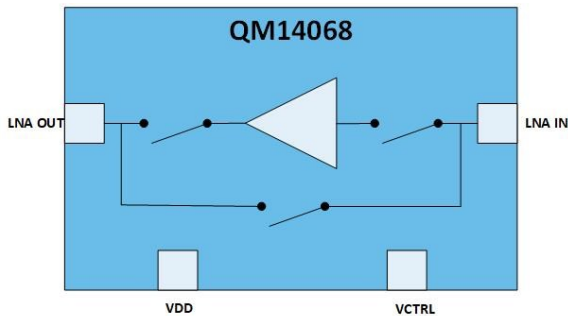


1 mm x 1.2 mm x 0.54 mm

## 1. Product Description

The QM14068 is a bypass switch and LNA to support wireless technology in the 6.2-8.3 GHz frequency range (UWB Channel 5 and 9). Control is via a single bit GPIO pin.

## 2. Functional Block Diagram



## 3. Feature Overview

- Typical NF of 1.8 dB across frequency range
- Typical Gain 15 dB
- Rx gain flatness in LNA mode -1.0 to +1.0 dB over max bandwidth (500 MHz)
- 1.8 V typical supply voltage
- Internal DC blocking on input and output pins
- Bypass to High Gain Switching Speed 400 nS

## 4. Applications

- 6.2 to 8.3 GHz Wireless Technology
- QM33/DW3000 based UWB applications with improved link budget

## 5. Ordering Information

PART NO.	DESCRIPTION
QM14068SB	5-pc Sample Bag
QM14068SR	100-pc, 7" Reel
QM14068TR7	3,000-pc, 7" Reel
QM14068EVB	Fully Assembled EVB + Sample Bag with 5 pieces

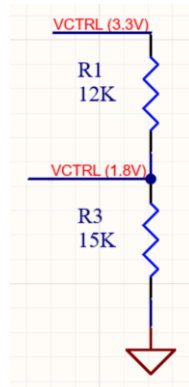
## 6. Absolute Maximum Ratings

PARAMETER	CONDITIONS	RATING	UNITS
Storage Temperature		-40 to 150	°C
VDD		2.2	V
Absolute max input power	HG Mode, 6:1 VSWR	9	dBm
Absolute max input power	Bypass Mode, 90°C, 50 Ω	22	dBm
Max DC voltage on RF pins		2.6	V

## 7. Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS
Supply voltage VDD	1.62	1.8	1.98	V
Control voltage High <sup>1</sup>	0.75 x VDD		1.98	V
Control voltage Low		0	0.4	V
Temperature	-40	25	85	°C

- For the DW3000/QM33-based applications, when the VDD1 supply rail is 3.3 V, the GPIO voltage level is also 3.3 V. When the DW3000/QM33 drives the VCTRL pin with VDD1 greater than 1.98 V, a resistive voltage divider is required to reduce the level of VCTRL to 1.8 V. Please see the diagram below as an example.



## 8. Electrical Specifications

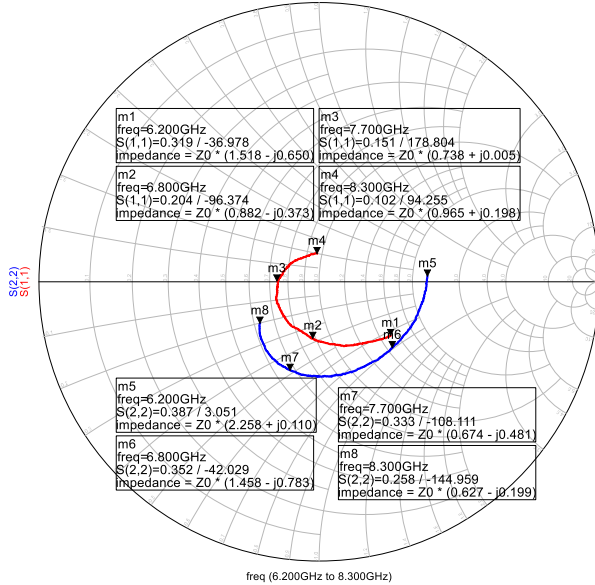
Test conditions unless otherwise stated: Input and Output = 50 Ω, T = 25 °C, V<sub>DD</sub> = 1.8 V / 0 V.

FREQUENCY RANGE: 6200 MHz TO 6800 MHz					
PARAMETER	MODE	MIN	TYP	MAX	UNITS
Gain	HG		15.0		dB
	Bypass		-0.86		dB
Gain Flatness	HG		0.4		dB
Noise Figure	HG		1.85		dB
Input Return Loss	HG		12.3		dB
	Bypass		18.2		dB
Output Return Loss	HG		8.5		dB
	Bypass		19.7		dB
Vdd Current	HG		10.4		mA
	Bypass		6		nA
HG → Bypass switching time (10-90%)	HG		128		ns
Bypass → HG switching time (10-90%)	Bypass		255		ns
Input P1dB	HG		-9		dBm

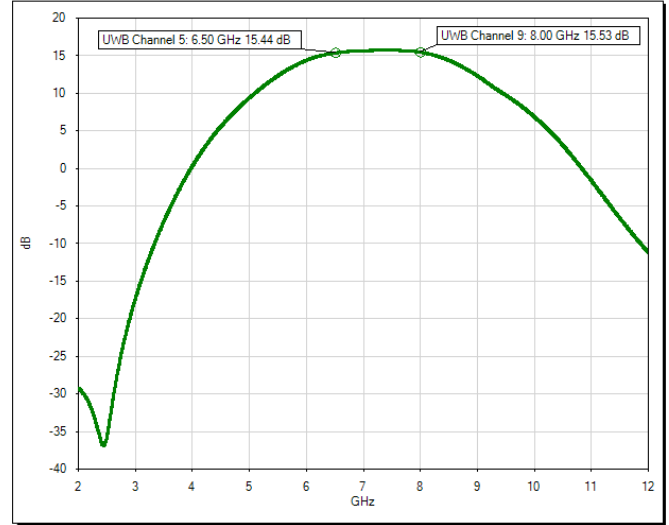
FREQUENCY RANGE: 7700 MHz TO 8300 MHz					
PARAMETER	MODE	MIN	TYP	MAX	UNITS
Gain	HG		15.3		dB
	Bypass		-0.9		dB
Gain Flatness	HG		0.5		dB
Noise Figure	HG		1.7		dB
Input Return Loss	HG		19.7		dB
	Bypass		27		dB
Output Return Loss	HG		11.7		dB
	Bypass		24.5		dB
VDD Current	HG		10.6		mA
	Bypass		6		nA
HG → Bypass switching time (10-90%)	HG		123		ns
Bypass → HG switching time (10-90%)	Bypass		321		ns
Input P1dB	HG		-11		dBm

**9. Performance Plots – High Gain Mode**

Input/output return loss – (6.2 GHz to 8.3 GHz)

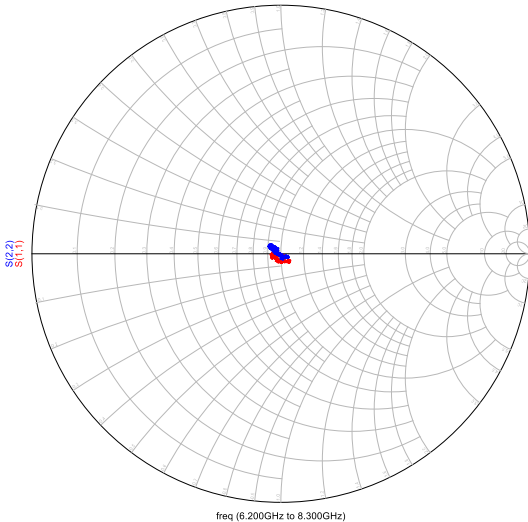


Gain (S21) vs Frequency

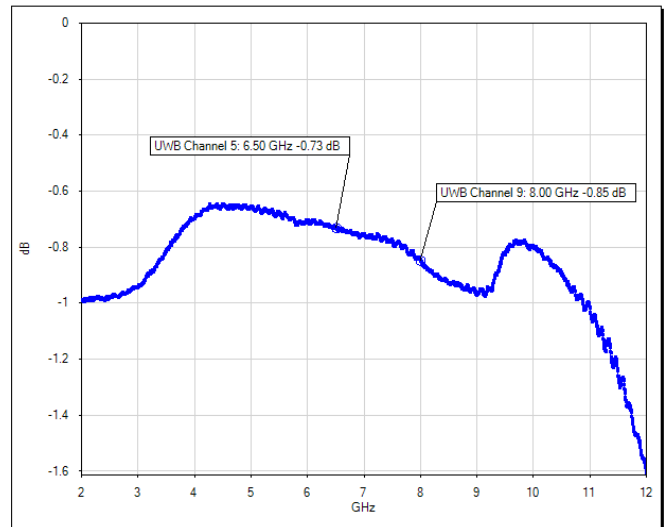


**10. Performance Plots – Bypass Mode**

Input/output return loss – (6.2 GHz to 8.3 GHz)



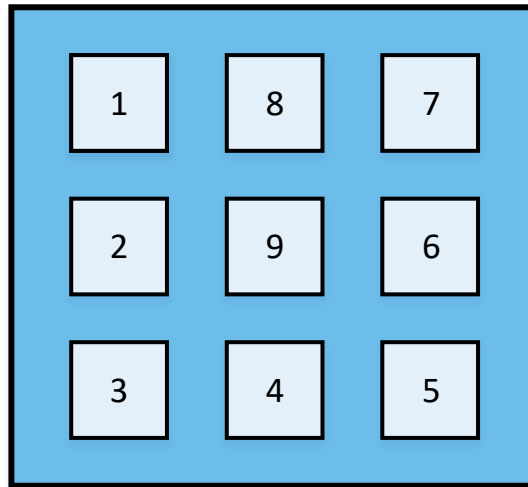
Gain (S21) vs Frequency



## 11. Truth Table

VDD	VCTRL	DESCRIPTION	PARAMETERS
High	1	HG Mode	LNA On
High	0	Bypass Mode (bi-directional)	LNA Off

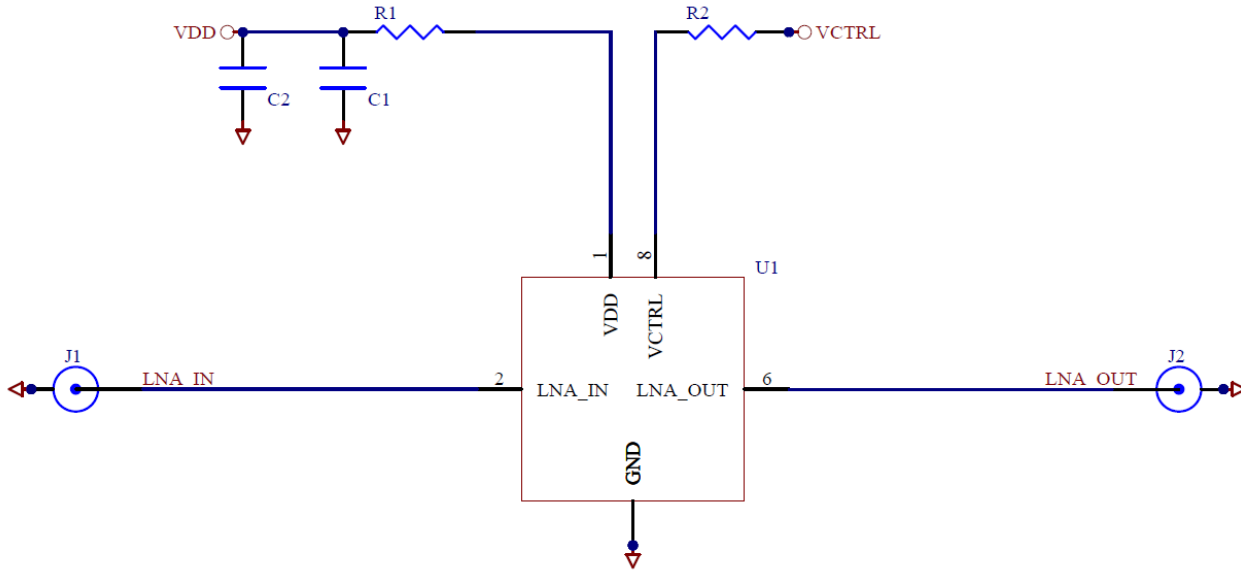
## 12. Pin Configuration and Description



Top View

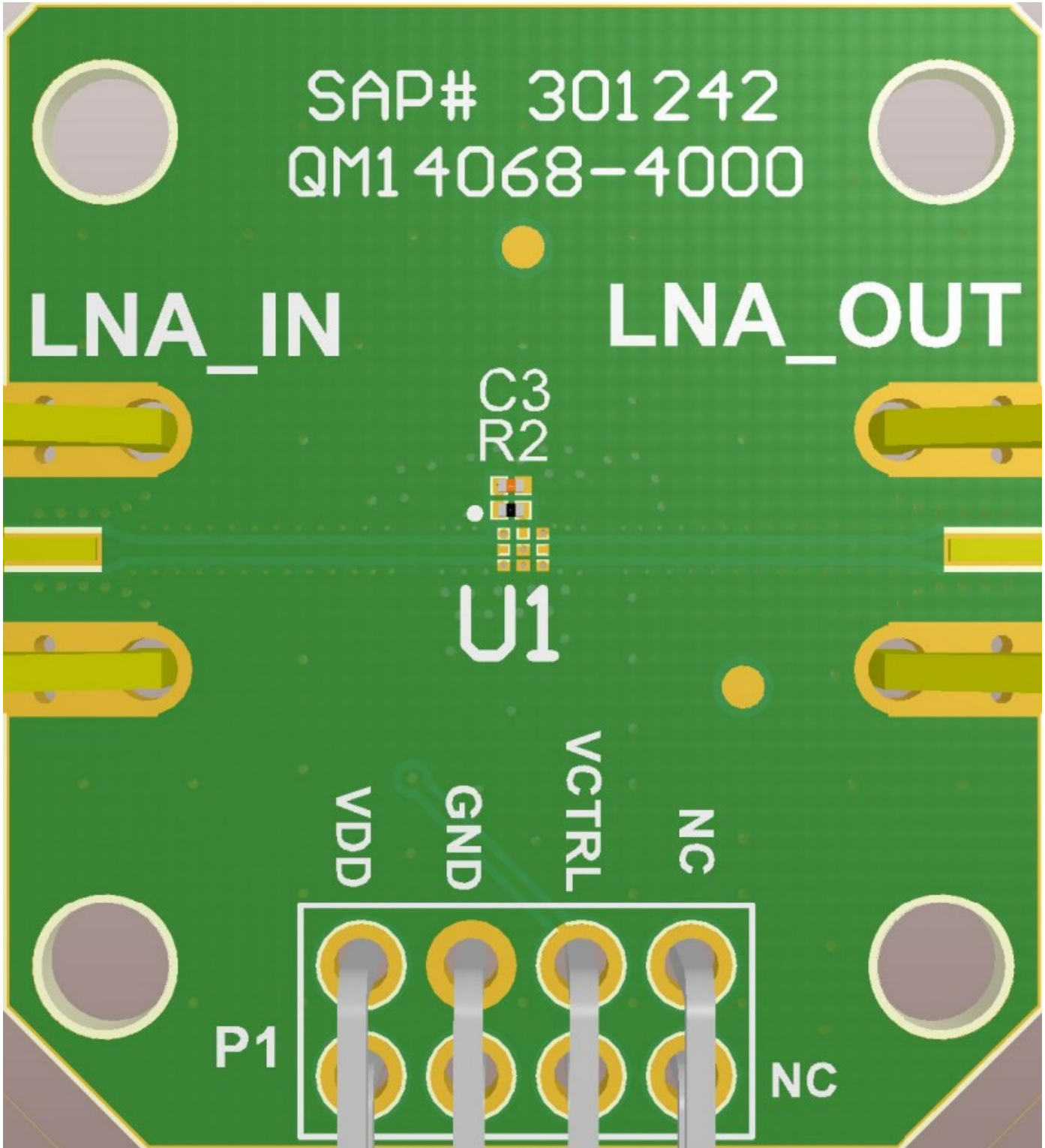
PIN NO.	LABEL	DESCRIPTION	PIN NO.	LABEL	DESCRIPTION
1	VDD	Voltage Supply	6	LNA OUT	LNA Output
2	LNA IN	LNA Input	7	GND	Ground
3	GND	Ground	8	VCTRL	GPIO Control Line
4	GND	Ground	9	GND	Ground
5	GND	Ground	-	-	-

13. Application Circuit



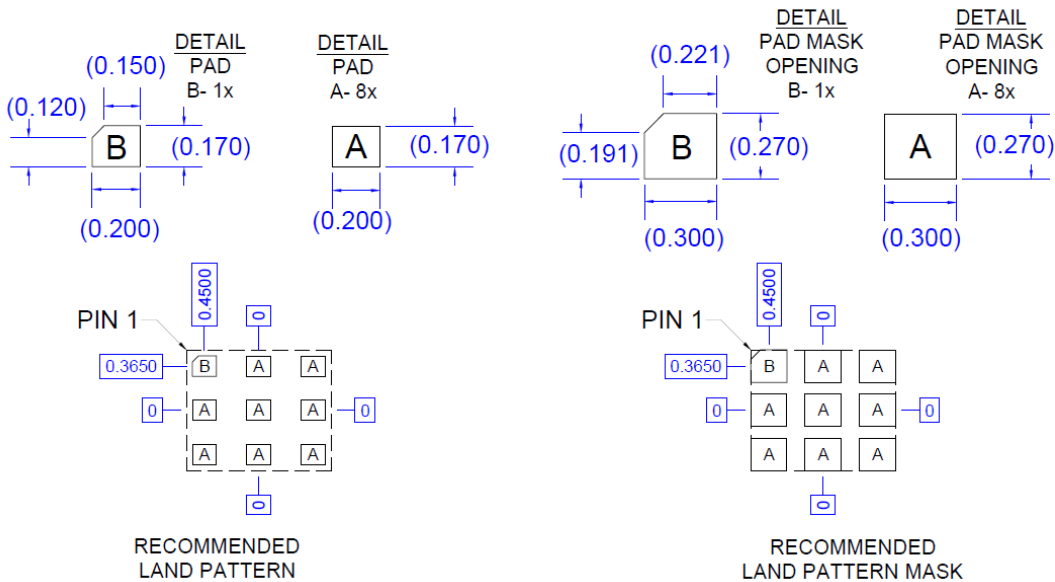
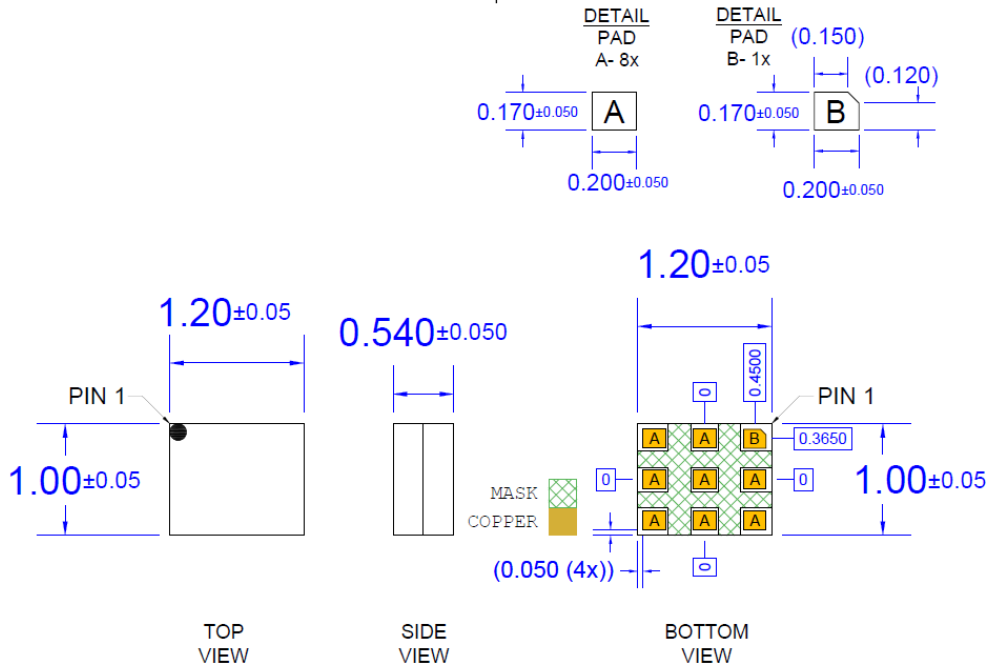
DESCRIPTION	DESIGNATOR	FOOTPRINT
CAP, 100 pF, 5%, 25 V, C0G, 0201	C1	0201_C
CAP, 0.1 $\mu$ F 5%, 25 V, X7R, 0201	C2	0201_C
RES, 0 $\Omega$ 1%, 1/20 W, 0201	R1, R2	0201_R

14. Evaluation Board Details

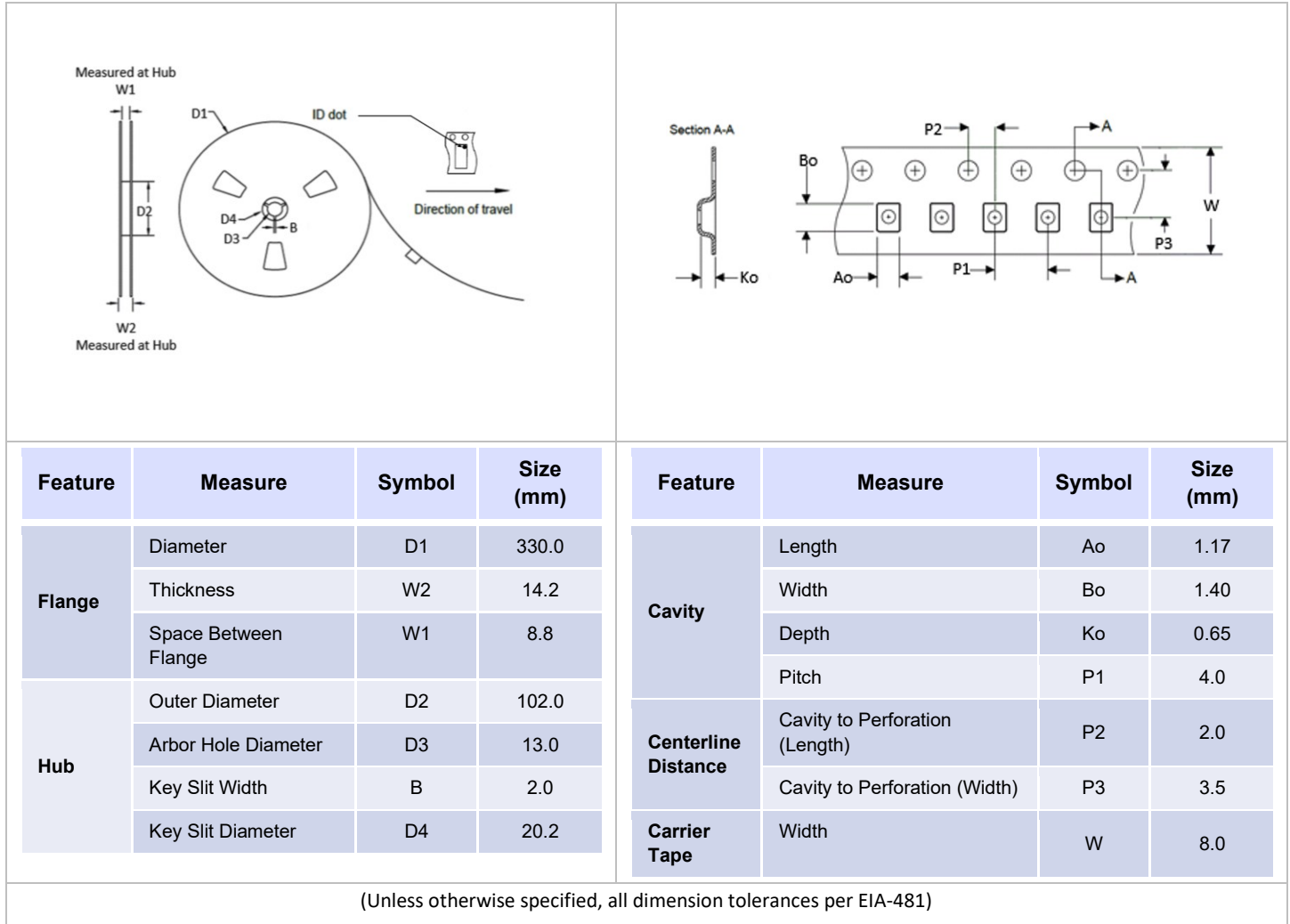


**15. Mechanical Information**

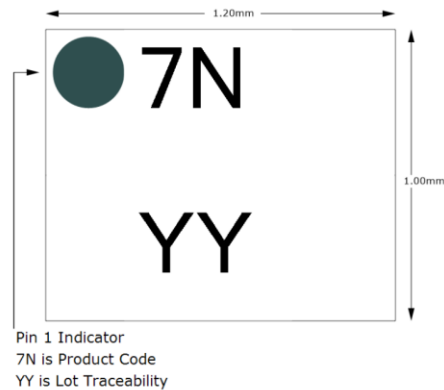
**Package Drawing**



16. Tape and Reel Information



17. Marking Diagram



**18. Handling Precaution**

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 1C	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	ANSI/ESDA/JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!  
 ESD sensitive device

**19. Solderability**

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.  
 Package lead plating: Electrolytic plated Au over Ni.

**20. RoHS Compliance**

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- SVHC Free.

## 21. Revision History

Data sheet Revision Code	Comments
A	Initial Release
B	Update Mechanical Drawing
C	Electrical Performance update
D	Updated Package Dimensions
E	Updated ESD rating, pin labelling
F	Updated MSL to Level 3 and pin number update
G	Updated Control Voltages and Ordering Information
H	Updated AMR, Electrical Specs, and EVB Information
I	Updated AMR, Operating Conditions, and Handling Precautions
J	Added Tape and Reel Information
K	Removed "Preliminary" Watermark and updated AMR
L	Updated Application circuit. Added frequency vs gain plots. Updated Tape and Reel information. Updated ordering information. Corrected the gain flatness specification. Added a note to indicate the LNA is bidirectional in bypass mode. Added a note for the requirement and a diagram of a voltage divider for the VCTRL pin. Minor text and format changes.

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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