Design Rules Verification Report

Filename : C:\Users\tt032358\Desktop\Torrance\ICQ-11942_PCB_QBK1SGLB-4000_MZhu_1

Warnings 0
Rule Violations 1

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (All),(All)	0
Clearance Constraint (Gap=78.74mil) (InNet('SWITCH_NODE')),(InNet('DC_GND') or InNet('LS_Source'))	0
Clearance Constraint (Gap=78.74mil) (InNet('DC+') or InNet('DC+2') or InNet('AC1') or InNet('AC2') or InNet('NetC34_2')	0
Clearance Constraint (Gap=78.74mil) (InNet('HS_Source')),(InNet('LS_Source'))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	1
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.1mil) (Max=196.85mil) (Preferred=19.685mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Minimum Annular Ring (Minimum=5mil) (All)	0
Hole Size Constraint (Min=0.1mil) (Max=500mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Silk To Solder Mask (Clearance=1mil) (IsPad),(All)	0
Silk to Silk (Clearance=0.039mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=3149.606mil) (Prefered=500mil) (All)	0
Total	1

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net DC+ Between Track (10824.803mil,4933.071mil)(10830.709mil,4927.165mil) on Top Layer And Pad