

Qorvo Defense and Aerospace Front - End Module Products and Applications

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Introduction

The Front-End Module (FEM) is a critical component in modern communication and Electronic War (EW) systems, playing a pivotal role in the transmission and reception of wireless signals. The FEM consists of a switch, a transmit channel (PA) and a receive channel (LNA), it is the gateway where signals transmit and receive to and from the open space. This note described Qorvo's state of the art RF front-end module products, exploring their functionality, application and integration in wireless communications and radar systems. Qorvo is investing a lot of effort and technologies to develop these modules to meet the ever-increasing market demands. Among these, products targeting radar applications such as QPF5001, QPF5002, QPF5005, QPF5010, QPM5811, QPM2637, QPF0219, QPM2100, QPM2101. Similarly, Qorvo has also developed a range of FEM modules for 5G communication in the FR2 bands such as QPF4005, QPF4006, QPF4001, QPF4002, QPF4010. These components incorporated innovative technologies, particularly high-performance III-V and GaN RF MMIC technologies. Additionally, due to the large number of RF front-end elements used in modern communication and radars systems, there is a tremendous advantage using high-performance, low-cost RF components, and peripheral biasing and control circuits. This note describes the details of using these components with bias control, signal routing, and timing controls.

Referenced Documents

The reference documents below take precedence over the contents of this application note, and should always be consulted for the latest information.

[1] Phased Array Radar Power Solution with Bias Autocalibration,

<https://www.qorvo.com/applications/defense-aerospace/radar/power-radar-chipset>

[2] Qorvo Product Datasheet, QPF5002 X band Front End Module

<https://www.qorvo.com/products/p/QPF5002>

[3] Qorvo Product Datasheet, AWS0103 X Band Silicon RADAR Quad Core IC

<https://www.Qorvo.com/products/AWS0103.html>

[4] Application Note: GaN Bias Circuit Design Guidelines

<https://www.qorvo.com/products/d/da006903>

[5] A Bias Sequencing Circuit for Amplifiers Requiring a Negative Gate voltage, Qorvo Application Note 107

<https://www.qorvo.com/products/d/da007774>

System and Application Configurations

Modern 5G communication systems or radar systems often employ active beamforming techniques so that signals can be electronically steered in different directions without the need to physically move the antenna. In addition, other modes of operations may be enabled including the support of multiple simultaneous beams, dynamic beam shaping, null steering, and multi-function apertures. Such a system requires a large number of Transmit/Receive (T/R) modules. Integration of multi-function components into a compact module simplifies system design and reduces complexity. Qorvo's multi-function FEM integrates several blocks into one package, enabling the seamless integration of RF front-end modules into the Active Electronically Steered Antenna (AESA).

A typical FEM device will have an antenna port and a T/R switch to direct RF signals to the Transmit and Receive signal chains. Dual-channel FEMs that include a second T/R Switch/PA/LNA combination may be required to support multiple data streams. Figure 1 shows a typical functional diagram of an FEM (QPF5002). The device transmit channel is normally a power amplifier (PA), while the receive channel has a low noise amplifier (LNA). Many times the LNA may have a front-end limiter for stress protection. The switch will have controls to route the RF signals between the two channels. These control signals may be either received directly from a host control interface or buffered by a dedicated controller IC within the FEM for more complex functions.

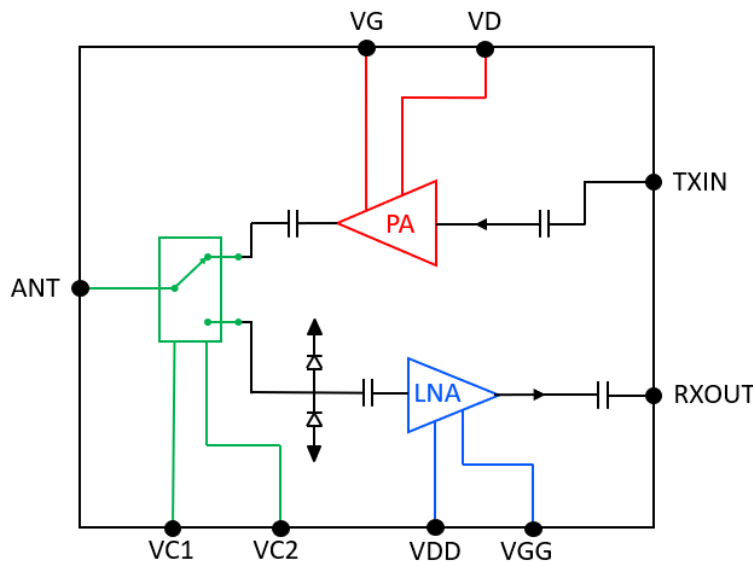


Figure 1. Functional block diagram of a typical FEM (QPF5002)

Whether used on radar or 5G applications, the FEM input/output port will be connected to an antenna, while the TX input and RX output will be connected to a beamformer circuit which contains multi-bit amplitude and phase controls to control the beam weighting for each radiating element. The summation across the full aperture of the individual FEM beam weightings determines the aggregated beam vector (pattern, direction). An additional driver amplifier may be needed between the beamformer and the FEM if the beamformer IC cannot deliver enough power to the PA. A typical FEM interfacing with a beamformer is shown in Figure 2.

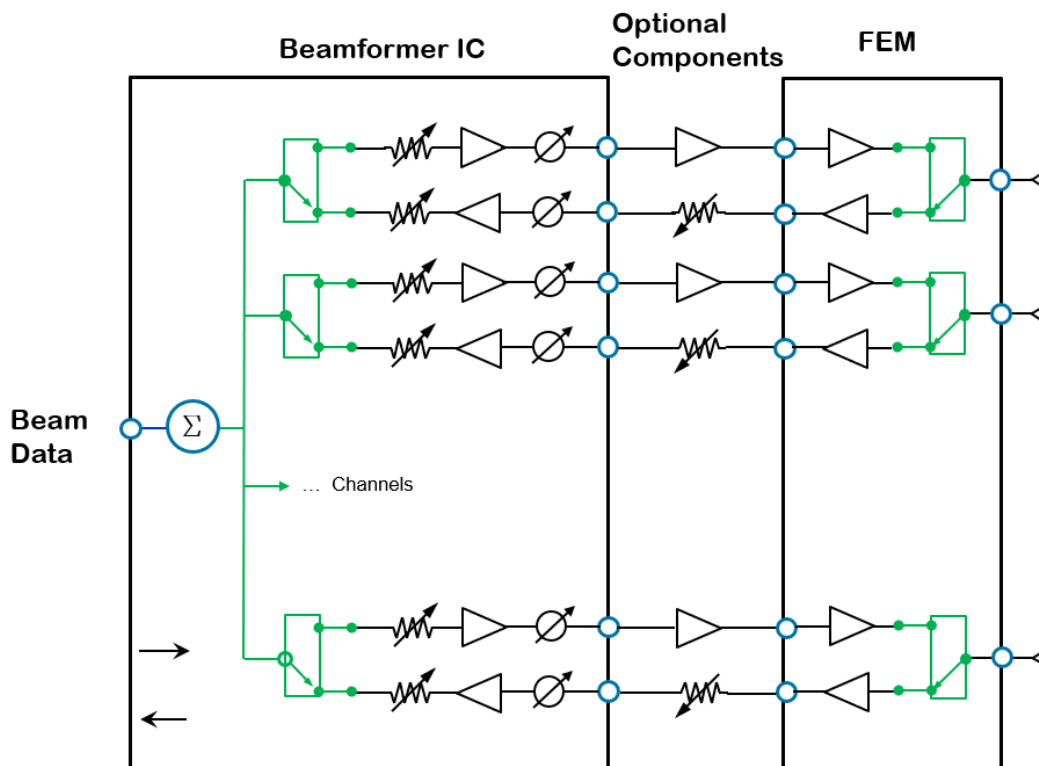


Figure 2. Beamforming block diagram for radar and 5G systems

FEM Biasing

Qorvo can provide a full solution with Serial Peripheral Interface(SPI) controlled bias reference designs for the FEM series product applications. These include the biasing required for PA, LNA, and Switches inside the FEMs. Qorvo also has a long-term plan to develop system-in-package solutions that support the ever-increasing demands for FEM applications to enable tiled phased arrays with tighter lattice spacings.

The biasing blocks to serve the FEM include PA and LNA drain supplies, gate controls, and switch controls. The GaN PA drain controller block is to supply up to 50 V (example shows 24 V) to the FEM PA. Generally, FEM PAs are designed using Qorvo's high power GaN processes, especially for radar applications. Some PAs are designed with GaAs processes where lower supply voltages can be used. The gate drivers provide gate controls to both the PA and LNA. Additionally, there is the SPDT controller to toggle the SPDT switches inside the FEM. Figure 3 (using the QPF5002 as an example) shows a functional block diagram with biasing blocks to work with the FEM. These biasing circuits can be controlled with a digital SPI interface to turn the PA or LNA ON and OFF as required; these features are desirable for systems to operate either in pulsed or Time-Division Duplexing (TDD) modes for which most radar or 5G systems are designed.

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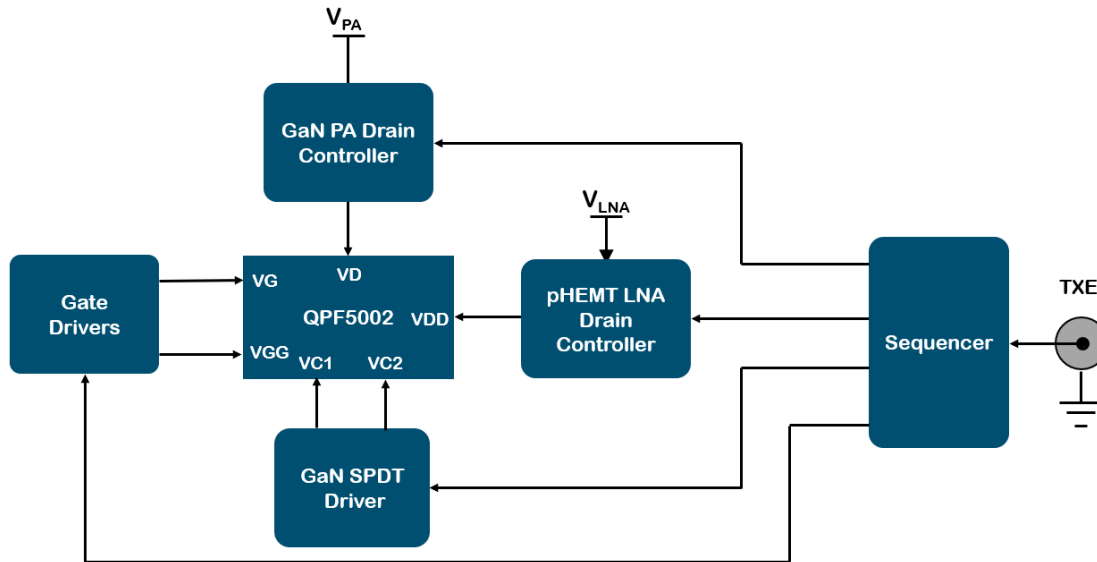


Figure 3. Functional diagram for FEM (Example QPF5002) biasing and control.

Power Amplifier Drain Controller

The drain power supply normally comes from a Low Drop-Out regulator (LDO) from a power management module. Many times, the supply will use a MOSFET driver switch controlled by a digital signal; this is to enable power supply ON/OFF functionality. This control can be used as a mechanism to protect the PA in case the gate is not turned ON prior to the drain, which we call negative voltage lockout. This can also be used to pulse control the amplifier as is sometimes required in TDD mode operation or for radar pulse mode applications. Figure 4 shows a block diagram of a typical circuit while the schematic is depicted in Figure 5.

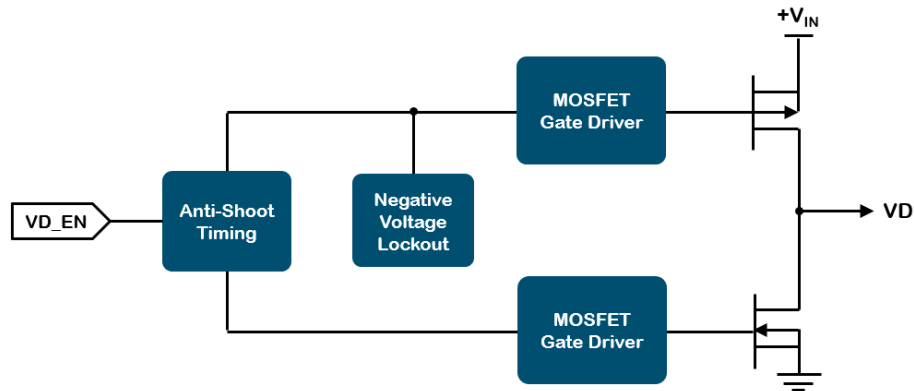


Figure 4. Block diagram of amplifier drain power controller.

By choosing different components, different voltage and current handling capabilities can be achieved. The diagram also includes a negative voltage lockout control circuit, whose function is similar to a sequencing circuit, which will disable the drain supply if a negative gate voltage not present.

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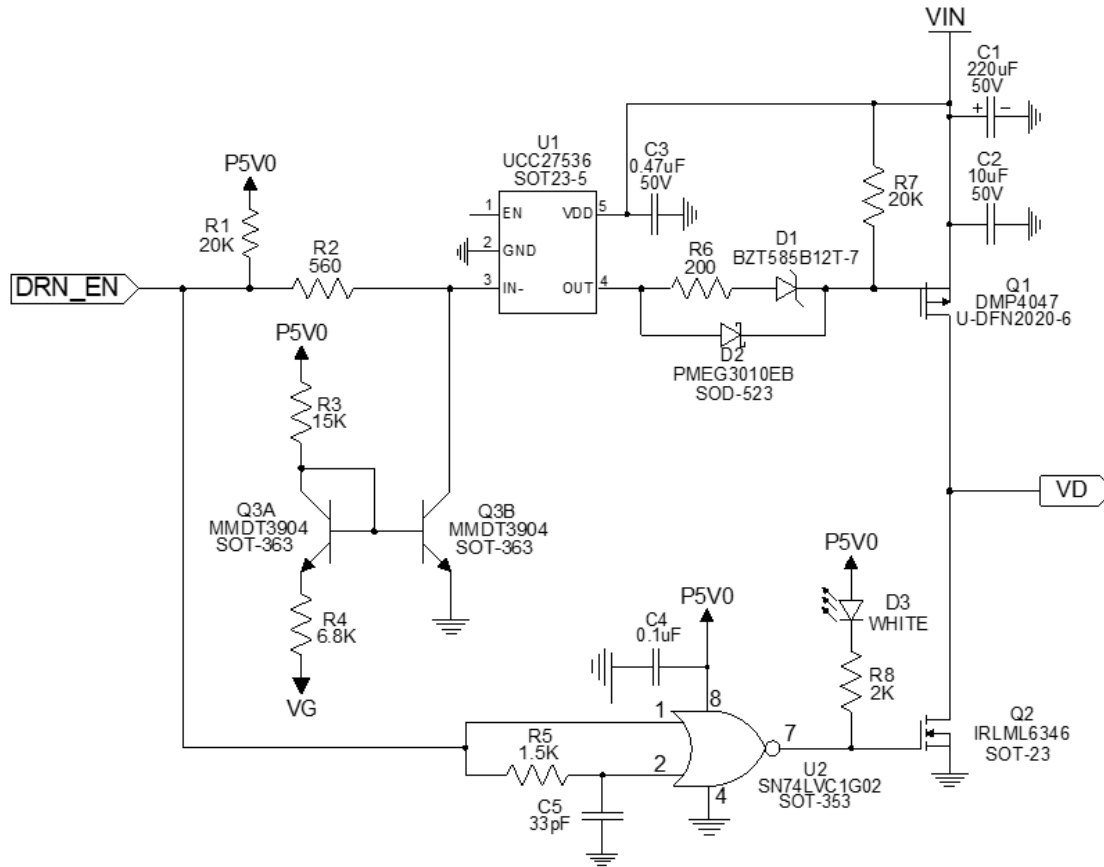


Figure 5. GaN amplifier drain controller schematic.

It is critical that the PA and LNA be tuned ON and OFF as quickly as possible. This will improve the communication system signal latency, and radar system response time and detection range. Reducing parasitic inductances between MOSFETs and load is key to achieve fast switching speeds. As an example, for a typical quad array, parasitic inductances are minimized by driving a pair of modules in parallel illustrated in Figure 6. This allows the MOSFETs to be co-located next to a module pair without long trace lengths. Both PA and LNA gate drivers are powerful enough to drive up to 4 MOSFETs in parallel. Performance is relatively insensitive to longer traces from MOSFETs back to the MOSFET gate drivers, allowing for convenient placement of components.

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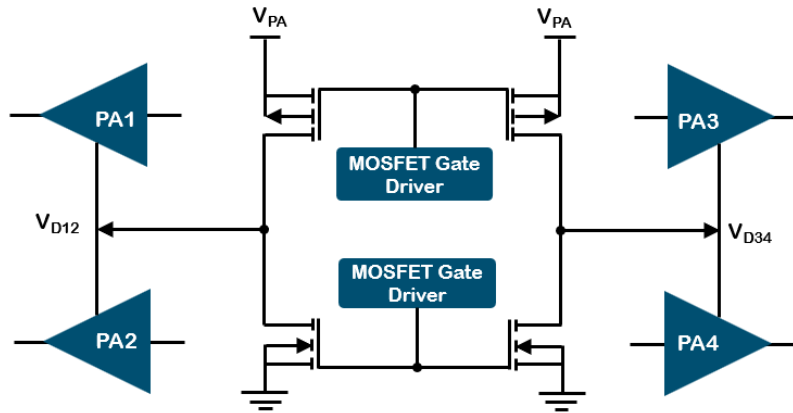


Figure 6. Driving quad PA modules in parallel and use drain drivers near PA to reduce parasitic inductance and reduce amplifier pulse ON and OFF transient time

Figure 7 shows the measured rise and fall times for a PA power supply which is enabled and disabled by drain switching control.

A similar drain controller can be used for LNA design with an example shown in Figure 8. This circuit can also be used to switch the LNA power ON and OFF for TDD or pulse applications.

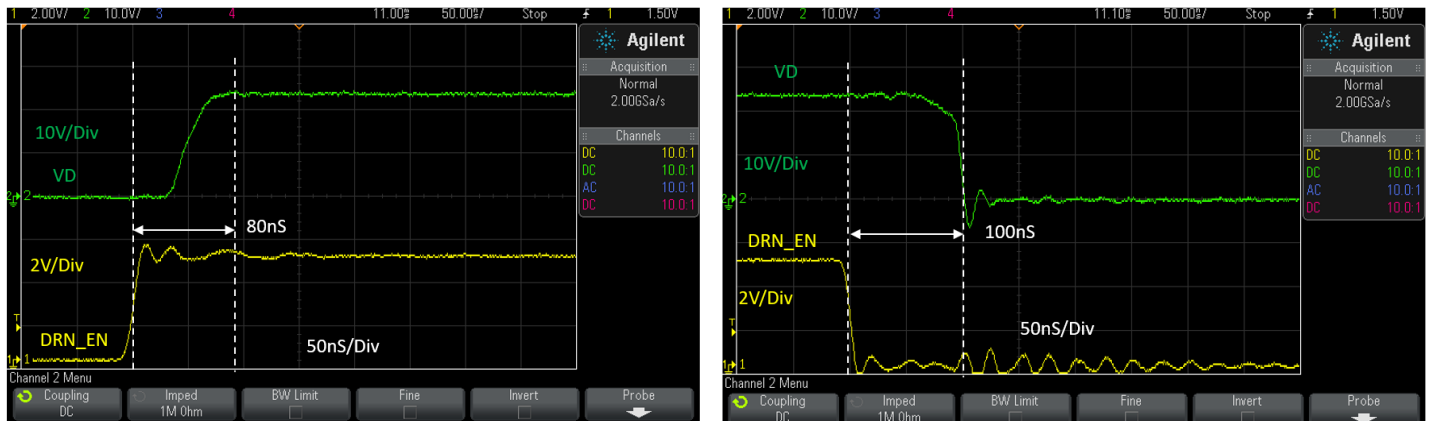


Figure 7. Rise/Enable (left) and Fall/Disable (right) times measured for GaN drain controller
 $V_{in} = 24\text{ V}$, $PW = 100\ \mu\text{S}$, $DC = 50\%$, $CI = 1\ \text{nF}$, $\text{Current} = 1\ \text{A}$, $T = 25\ \text{°C}$.

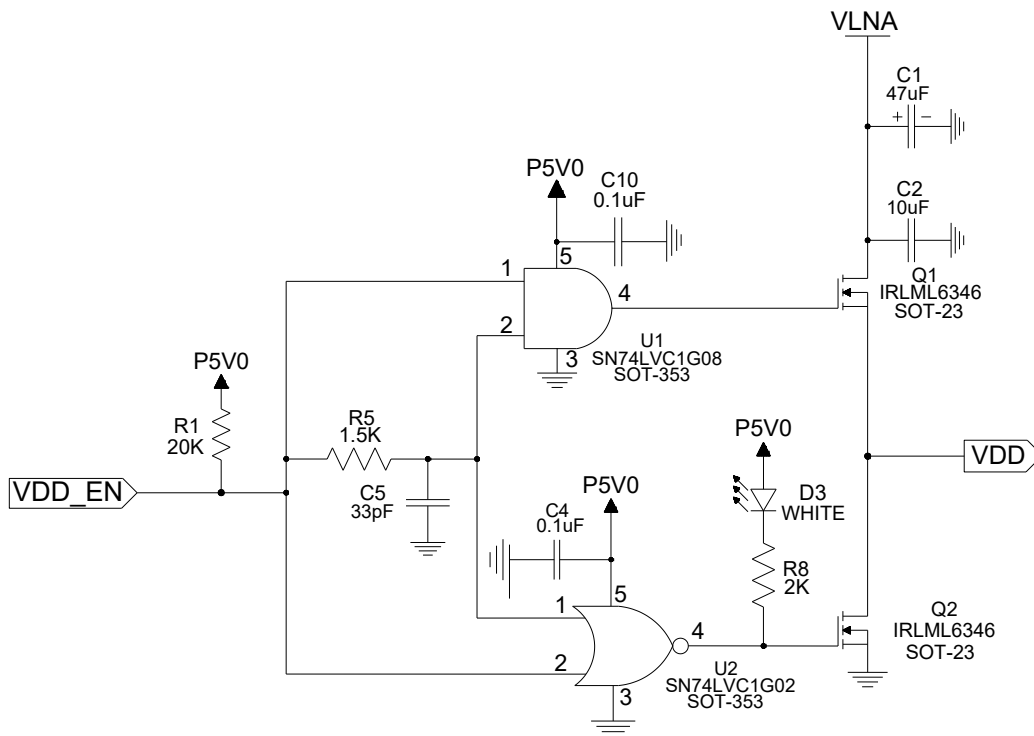


Figure 8. LNA Drain Controller

Amplifier Gate Controls

The gate control of the amplifiers is to set the gate voltage such that the amplifier will be biased either at the proper current or pinched off. Most of Qorvo FEMs used GaN or GaAs pHEMT for RF signal amplification or deliver RF power output. GaAs pHEMT devices can have either E-mode or D-mode operation depending on the fabrication process. For E-mode devices, they will turn on when the gate voltage increases to a certain level above 0 V. For D-mode devices, the gate control normally needs a negative voltage to bias to get nominal current. If the gate is left open or grounded, the FET will conduct current when drain voltage is applied. This will normally lead to parts being stressed or even damaged due to large current. Therefore, a sequencing, or sometimes called drain lock out, circuit is needed to turn ON the gate voltage first before the drain voltage is turned ON. During the bias OFF procedure, the gate voltage will stay on for a certain time after the drain voltage is switched OFF.

In this note we will not describe details on this sequencing circuit, focusing instead on gate switching controls. For more details on the sequencing circuits, the user may refer to Qorvo application note 107 [5].

Figure 9 depicted a biasing circuit to both PA and LNA with temperature compensation mechanism. The circuit makes use of DAC to tune the voltages to get proper PA or LNA current. Figure 10 is the detailed circuit schematic.

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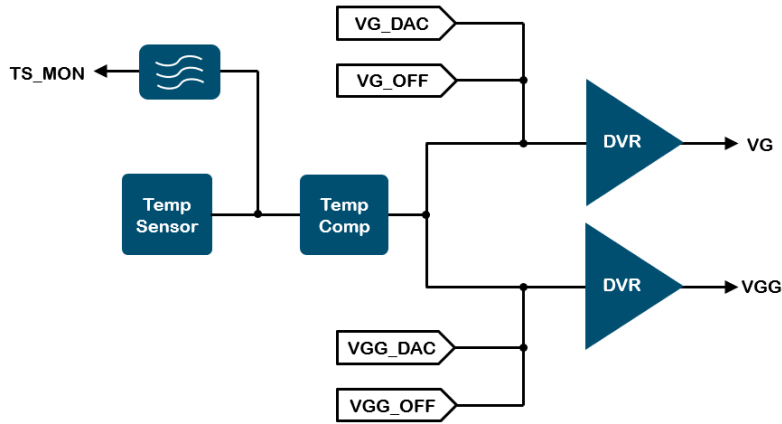


Figure 9. Gate Controller Functional Diagram

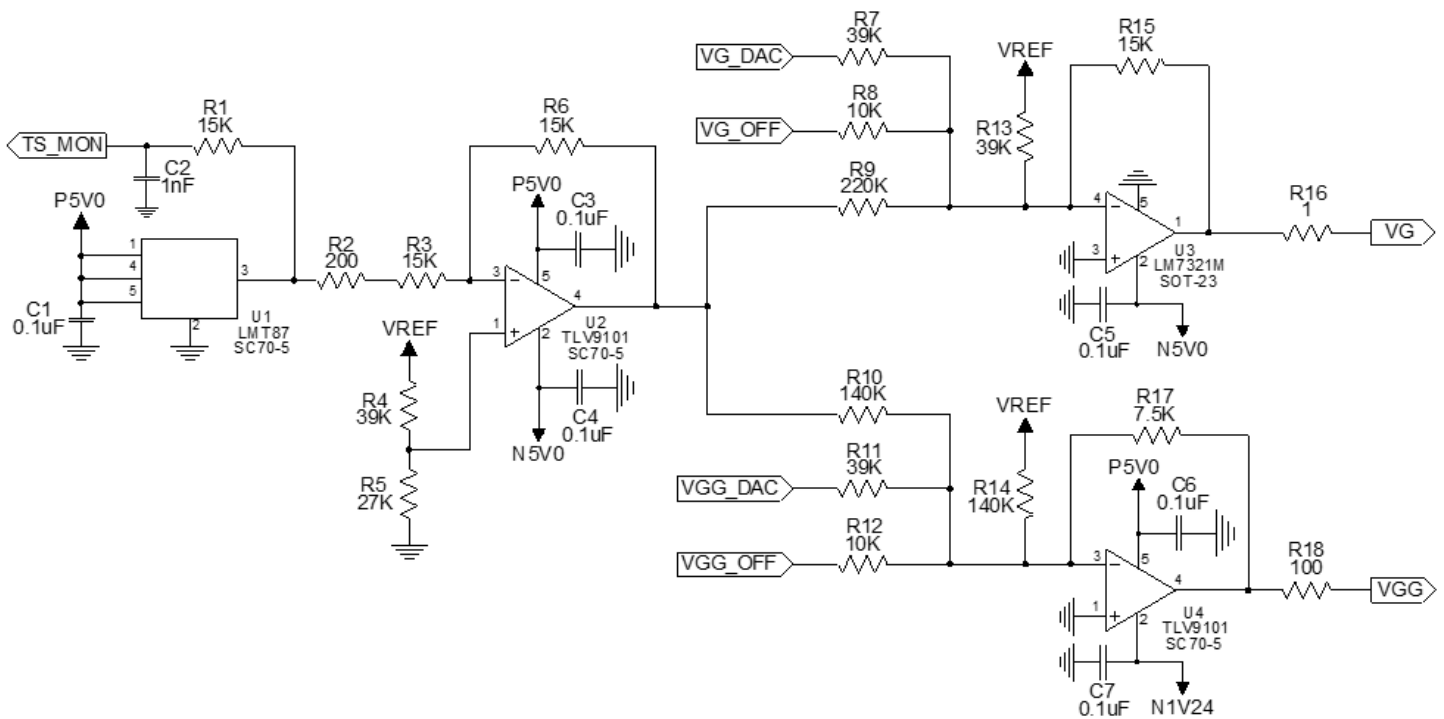


Figure 10. Gate Controller Diagram with temperature compensations

For a 5G communication systems or pulsed radar application, a TDD mode or pulse mode is required. The gate switcher circuit is needed to turn the amplifier ON and OFF by toggling the gate voltage between a nominal voltage and the pinch off voltage. Figure 11 and Figure 12 show the switcher block diagram and detailed schematic diagram, respectively. The diagram works for both the PA and LNA. The difference is that the nominal bias value comes from the PA gate driver and LNA gate drivers. The pinch off voltage is usually different for the PA and LNA. For GaN devices the pinch off voltage is normally set to -5 V, while for GaAs the pinch off voltage is between -1 V to -2 V depending on the fabrication process used.

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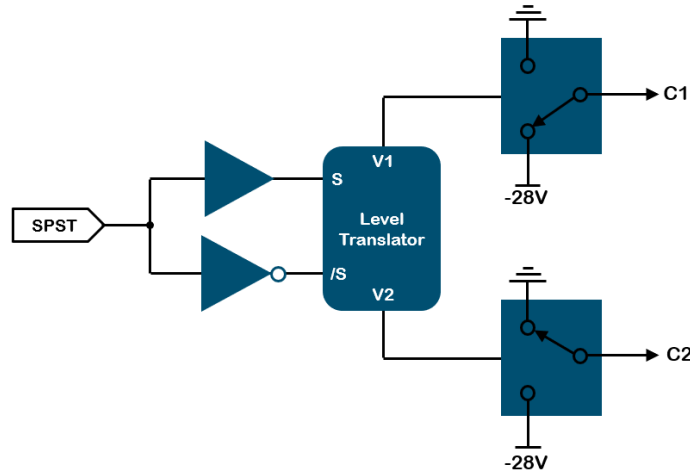


Figure 13. SPDT Switch Control Functioning Diagram

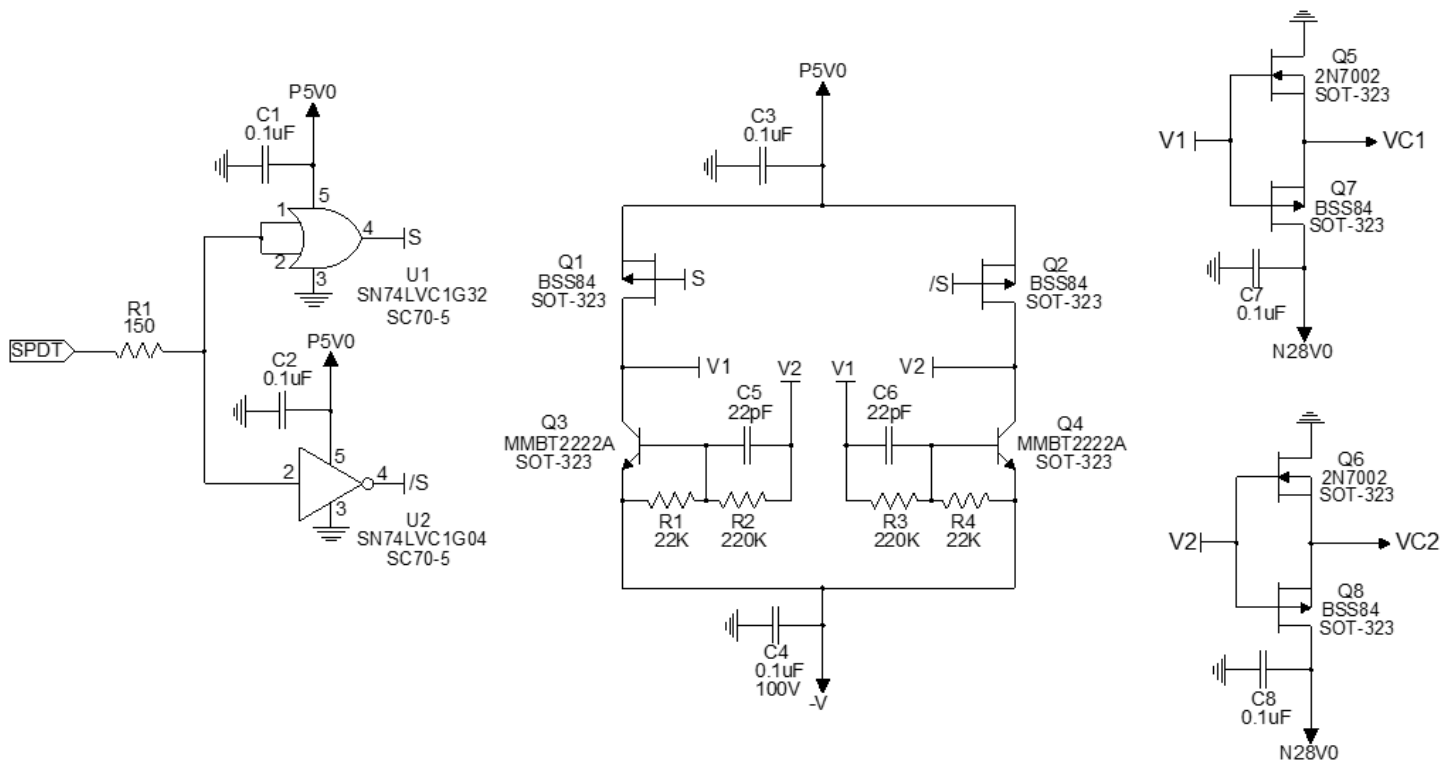


Figure 14. Switch Control Schematics

The time domain simulated control signal of the switching circuit is shown in Figure 15. A typical switching time is around several tens of nanoseconds.

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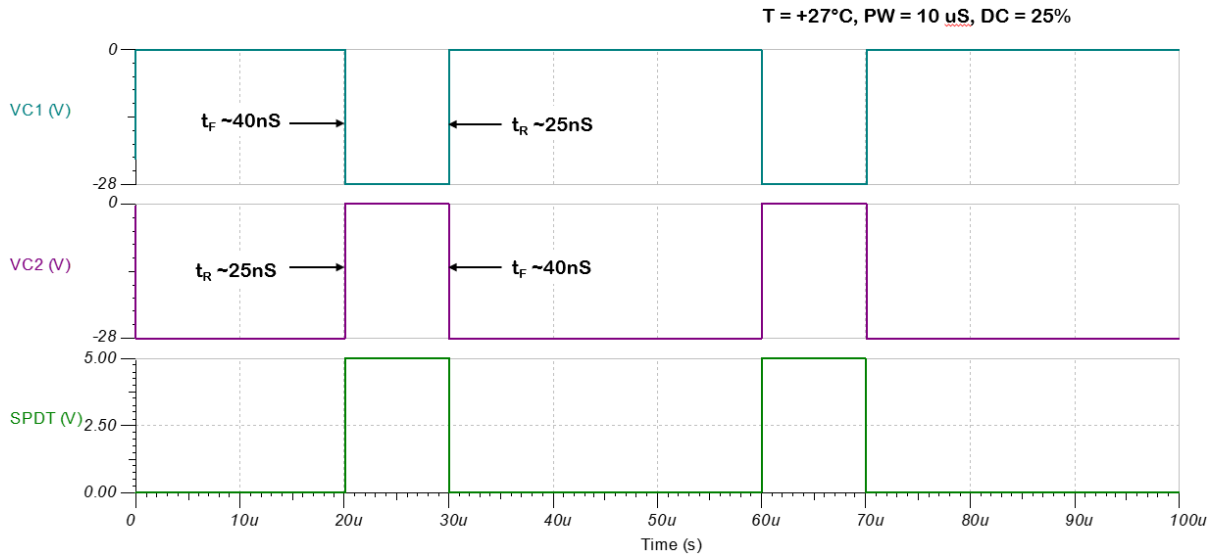


Figure 15. Time Domain Simulated Response for SPDT Switch Control

Power Supplies for FEM Biasing and Controls

It is often desirable to use negative gate or switch control voltages. A charge pump inverter can be used to invert a positive voltage to negative voltage for gate biasing or switch controls. A block diagram of such a circuit is shown in Figure 16. In this case a positive +5 V is used to obtain various negative voltage sources.

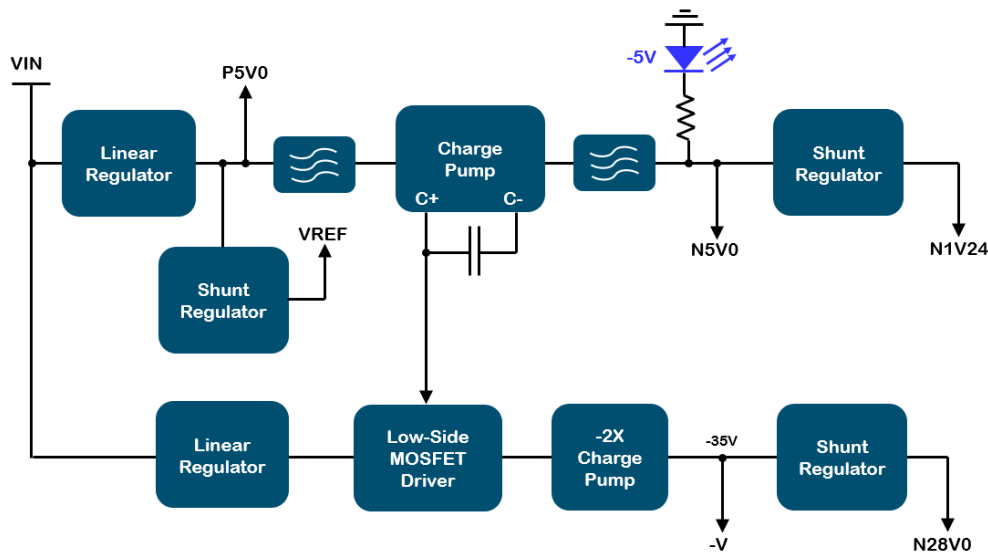


Figure 16. Charge Pumping Negative Inverter, Example to Generate -5 V from a +5V Power Supply

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A more challenging requirement is to generate -20 V to -40 V of switch control voltages. Figure 17 shows a detailed voltage inverter using a +5 V power supply. It can generate a control voltage down to -40 V, as well as other negative voltages.

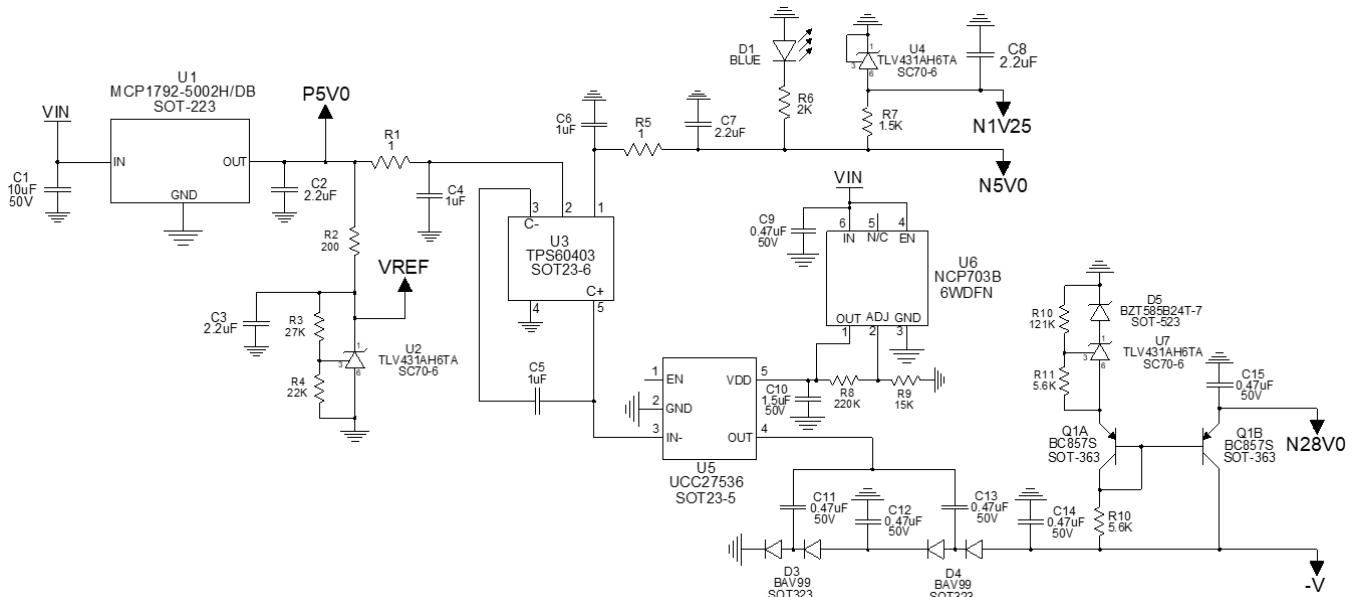


Figure 17. Negative Voltage Invertor for GaN Switches

RF Signal Routing, Switching and Timing Controls

The sophistication of RF signal control has evolved with higher performance components and increasingly complex communication architectures. This allows for rapid operation mode switching to enable short latency for communications system and faster response for radar systems. Most of these systems employ a beamforming IC as a driver to drive T/R modules. Figure 18 is a diagram showing the signal flow for a x4 beamforming lattice using Qorvo’s AWS0103 beamformer. This beamformer IC can drive 4 T/R modes with phase and magnitude control. It has four TR channels, each pair of RXn and TXn feed to one of the T/R modules (for instance, the QPF5002).

This functioning diagram consists of drain supply drivers, gate drivers and switchers, FEM switch control drivers, and sequencing circuits. The bias control signals can be designed to toggle the amplifiers ON and OFF. Users can either pulse control the drain power supply or control the gate as described in previous sections. The sequencing circuits are used to send control signals to enable or disable components and perform RF signal routings. The sequencing circuits can introduce time delays to control signals to turn OFF and ON functional components in a certain sequence; this will ensure system stability and have a smooth transition between operation modes. The cost is more complicated circuits, but will have better RF performance such as pulse-to-pulse magnitude and phase balance and consistency. Figure 19 shows an example of sequencing circuits with delay mechanisms. Figure 20 shows the sequencing steps and timing diagrams for transitioning from TX to RX modes. Figure 21 shows the sequencing steps and timing diagrams for transitioning from RX to TX modes. These diagrams show how and when each functional block is turned ON and OFF and how and when signals are routed and operation modes are switched.

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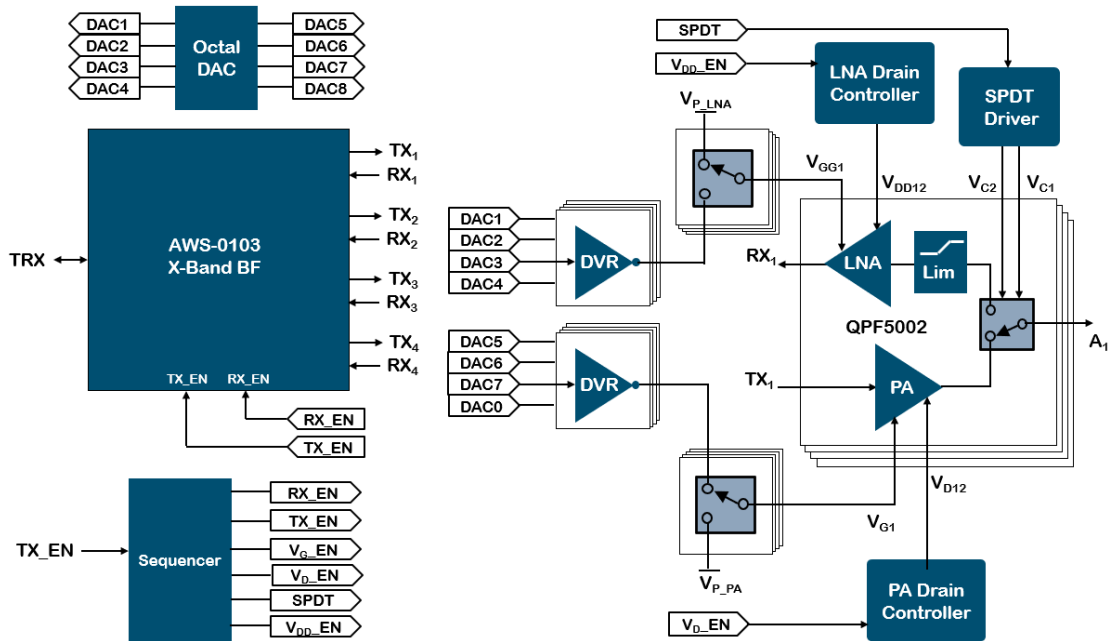


Figure 18. Signal Flow and Control of a x4 QPF Modules with AWS-0103 Beamformer

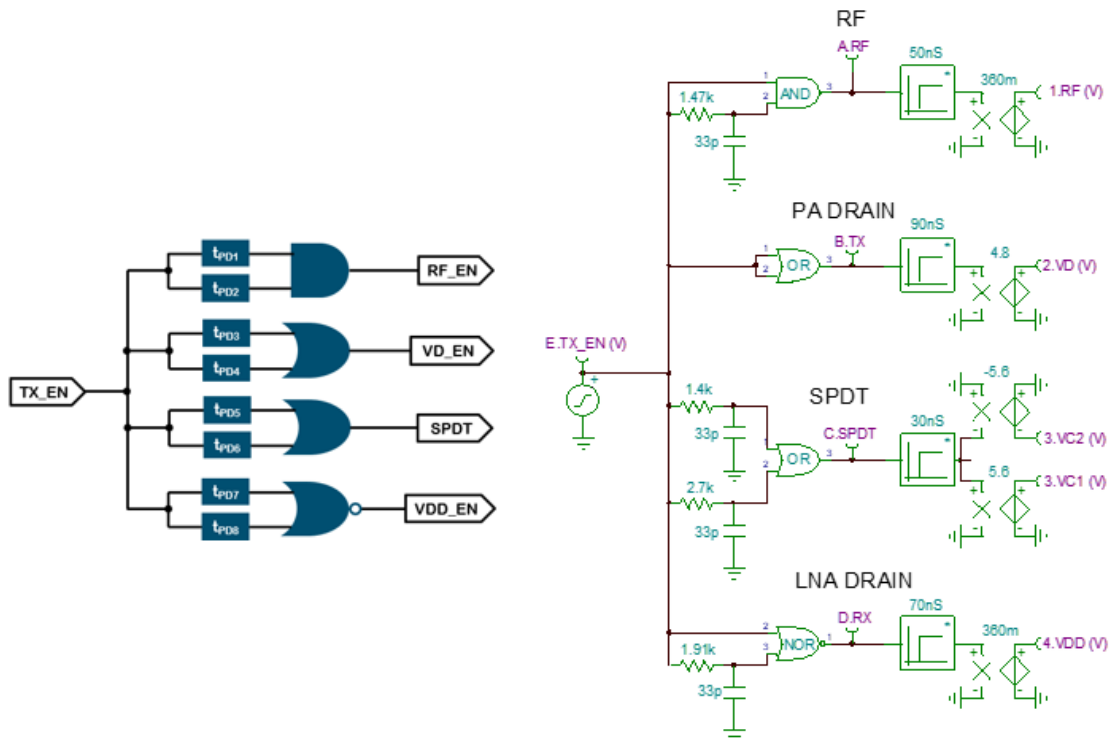


Figure 19. Sequencing circuits with time delays

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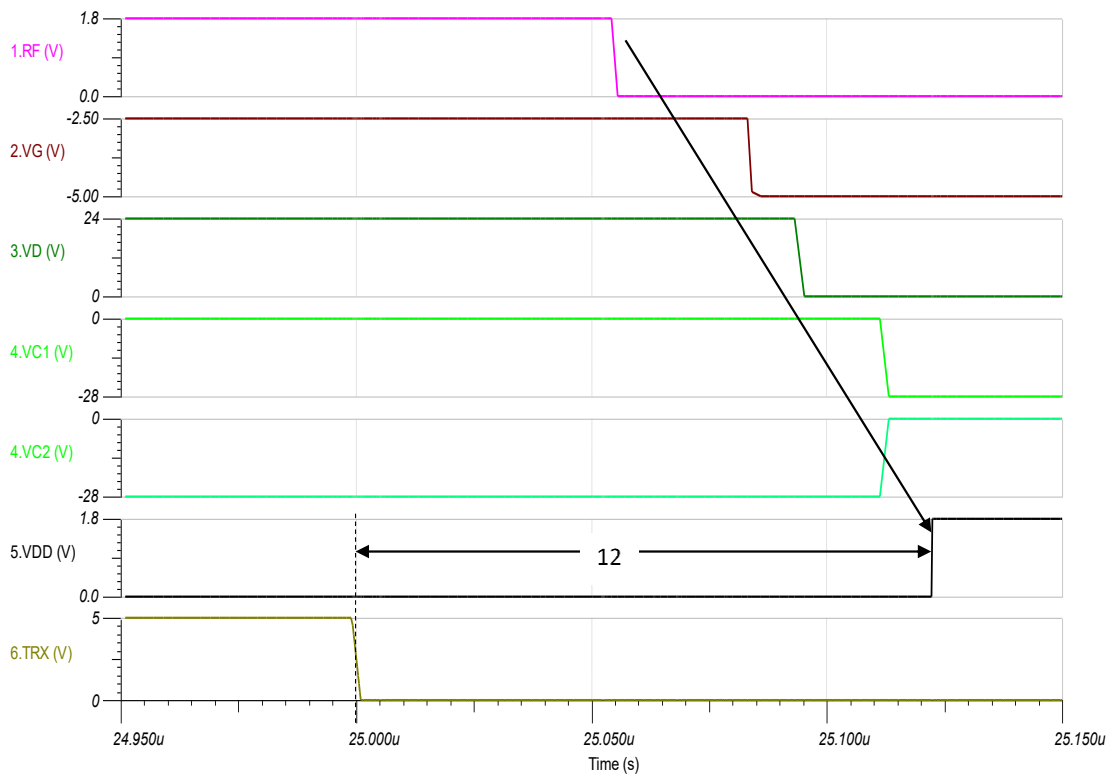


Figure 20. Transition from TX to RX Timing Diagram for FEM Controls

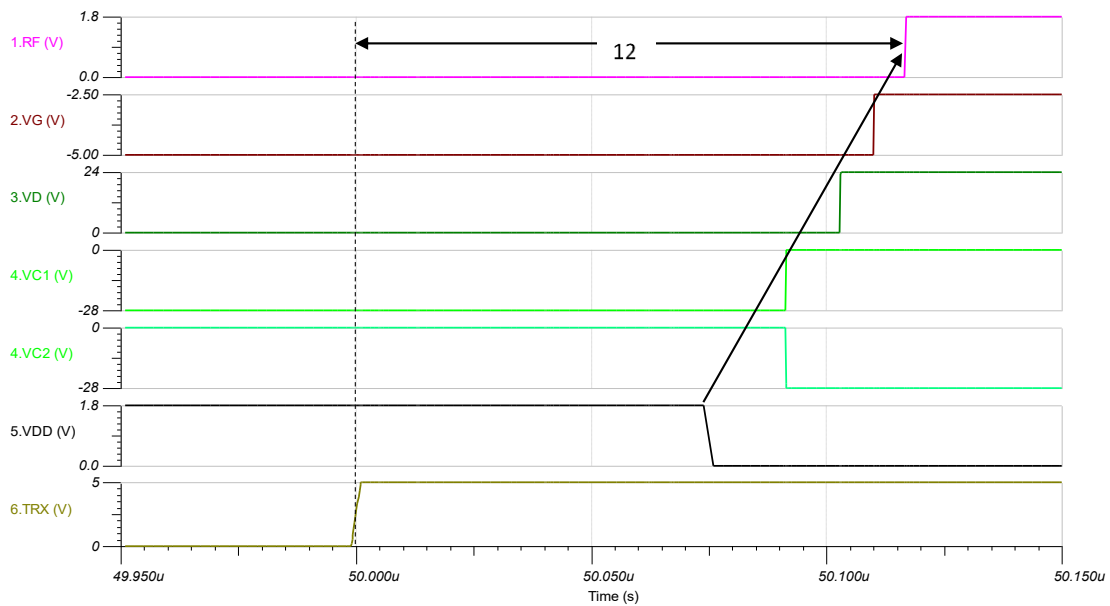


Figure 201. Transition from RX to TX Timing Diagram for FEM Controls

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The transition time needed for devices between ON and OFF states or mode switching for the array system is critical for system operation. This response time is dictated by the bias control circuit elements and RF chain components and their parasites. These usually include external bias circuit and off-chip components such as bias chokes and stability circuits. Normally on-die elements include bias chokes and stability circuits which usually have small value capacitors (ranging from a few picofarads to several hundred picofarads), as well as some additional resistors as well. The time constant of these on-die elements is usually in the range of 10 ns to 200 ns. Therefore, the main cause of time delays are off-chip components which may use up to several hundred microfarads of capacitance. These components are primarily for stability purposes. Sometimes they can be adjusted to smaller values or even removed since they can be redundant. If these elements are desirable for stability purposes, they can be either absorbed in the biasing circuitry or use an equivalent charge storage mechanism on the bias side to enable fast charging or discharging mechanism to improve response times. (If users need these reference designs, please contact the Qorvo Support Team.)

Figure 22 is an example of a quad lattice design as described in this note. It consists of one BFIC and four T/R FEMs. The demo board also includes the required biasing and signal control circuits for element control for radar applications. The board feature X-band applications with 15 mm of lattice spacing with full CMOS digital controls. Users interested in this or similar designs can contact Qorvo Support Team for reference.

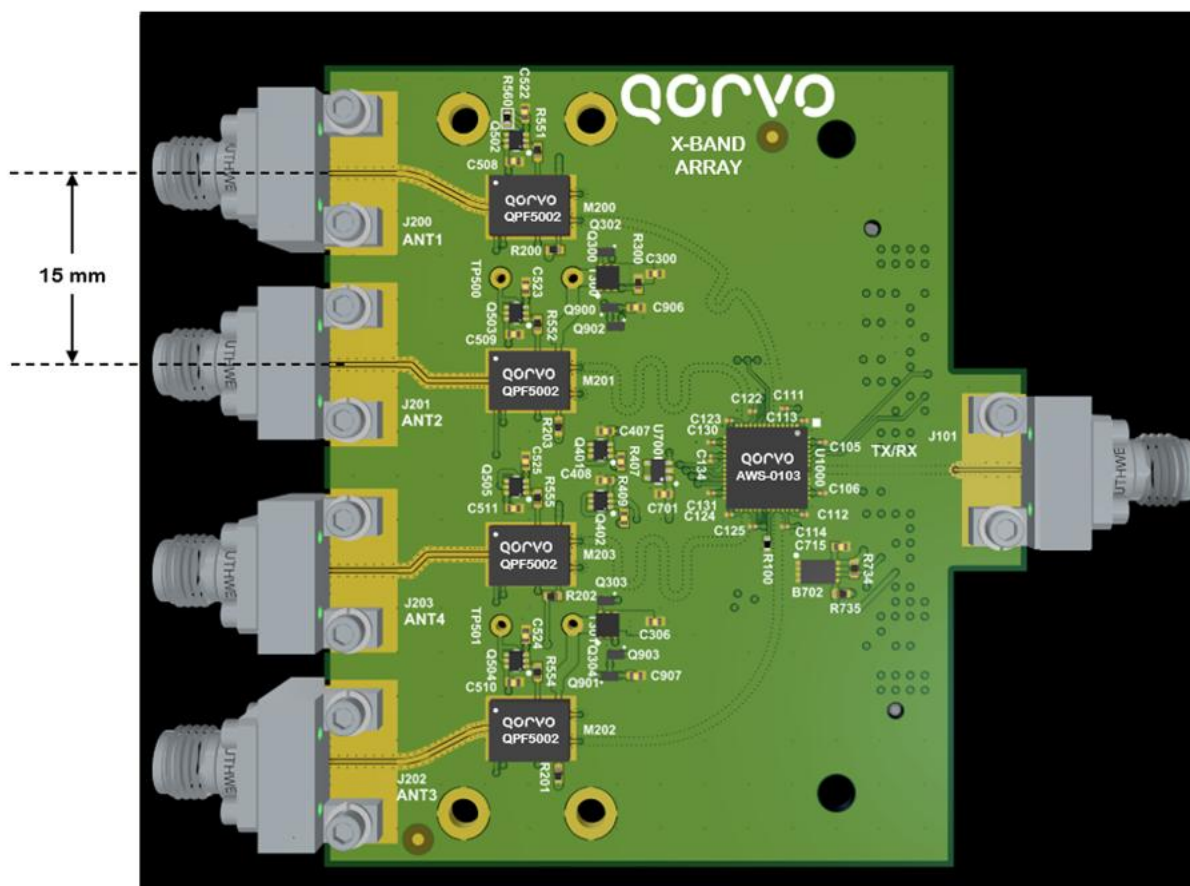


Figure 22. X-Band Quad Lattice Demo Board using AWS0103 Beamformer and QPF5002

Summary

With a large portfolio of RF/Microwave Front End Modules and leading-edge GaAs and GaN semiconductor technologies, Qorvo is poised as a forerunner in Phased Array radar and 5G communication array systems. Qorvo also has mature resources to provide full solutions for the development of radar and 5G system designs and implementations. As shown in this application note, Qorvo can provide detailed solutions to bias the T/R module amplifiers and switching control of signals. Qorvo also has a full array of power managements modules to enable efficient and reliable array system architectures.

For more information on these products and technical references, users can browse Qorvo website or contact Qorvo Support Teams for more details.

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Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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