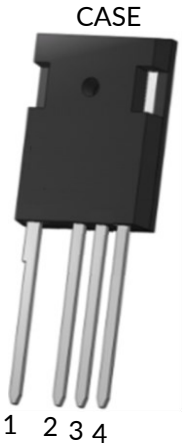
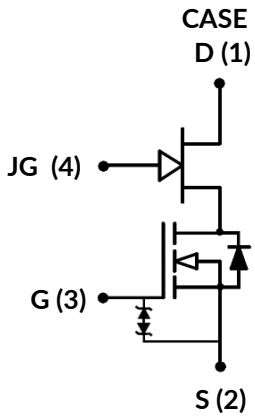
DATASHEET

UG4SC075009K4S





Part Number	Package	Marking
UG4C075009K4S	TO-247-4L	UG4SC075009K4S

RoHS COMPLIANT | Pb LEAD FREE | HF HALOGEN FREE

750V-9mΩ Dual-Gate SiC FET

Rev. B, May 2024

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. This device is assembled in the TO-247-4L package with gates of both JFET and MOSFET accessible. This configuration provides more strategies for controlling the switching performance and makes the device suitable for a wide range of applications. This device has an ultra-low on-resistance and is well suited for solid state circuit breaker and motor drive applications.

Features

- Dual-gate configuration for improved switching speed control
- On-resistance $R_{DS(on)}$: 9mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} =368nC
- Low body diode V_{FSD}: 1.1V
- Low gate charge: Q_G =75nC
- Threshold voltage $V_{G(th)}$: 4.5V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3

Typical applications

- Protection circuits
- DC-AC Inverters
- Switch mode power supplies
- Motor drives

Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750V	V
JFET Gate (JG) to source voltage	V_{JGS}	DC	-30 to +3	V
		AC [1]	-30 to +30	V
MOSFET Gate (G) to source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current [2]	I_D	T_C < 61°C	106	A
		T_C = 100°C	86	A
Pulsed drain current [3]	I_{DM}	T_C = 25°C	344	A
Single pulsed avalanche energy [4]	E_{AS}	L=15mH, I_{AS} = 5.2A	202	mJ
Power dissipation	P_{tot}	T_C = 25°C	375	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J,T_{STG}		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	°C

1. +30V AC rating applies for turn-on pulses <200ns applied with external R_G > 1Ω.
2. Limited by bondwires
3. Pulse width t_p limited by $T_{J,max}$
4. Starting T_J = 25°C

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.31	0.40	°C/W

Electrical Characteristics (T_J = +25°C and V_{JGS} = 0V unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions		Value			Units
				Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	V_{GS}=V_{JGS}=0V, I_D=1mA		750			V
Total drain leakage current	I_{DSS}	V_{DS}=750V, V_{GS}=0V, V_{JGS}=0V, T_J=25°C			4	84	µA
		V_{DS}=750V, V_{GS}=0V, V_{JGS}=0V, T_J=175°C			35		
Total JFET gate leakage current	I_{JGSS}	V_{JGS}=-20V, V_{GS}=+12V			0.1	65	µA
Total MOSFET gate leakage current	I_{GSS}	V_{GS}=-20V / +20V			2	20	µA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=12V I_D=70A	V_{JGS}=2V T_J=25°C		8.4		mΩ
			T_J=25°C		9	11.5	
			T_J=125°C		14.8		
			T_J=175°C		19.4		
JFET gate threshold voltage	$V_{JG(th)}$	V_{DS}=5V, V_{GS}=12V, I_D=110mA		-11.3	-9.3	-6.7	V
MOSFET gate threshold voltage	$V_{G(th)}$	V_{DS}=5V, V_{JGS}=0V, I_D=10mA		3.5	4.5	5.5	V
JFET gate resistance	R_{JG}	f=1MHz, open drain			0.8		Ω
MOSFET gate resistance	R_G	f=1MHz, open drain			2.3		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current [1]	I_S	T_C < 61°C			106	A
Diode pulse current [2]	$I_{S,pulse}$	T_C = 25°C			344	A
Forward voltage	V_{FSD}	V_{GS}=0V, V_{JGS}=0V, I_S=35A, T_J=25°C		1.10	1.24	V
		V_{GS}=0V, V_{JGS}=0V, I_s=35A, T_J=175°C		1.14		
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=70A, V_{GS}=V_{JGS}=0V, R_{JG}=0.7Ω di/dt=4400A/µs, T_J=25°C		368		nC
Reverse recovery time	t_{rr}			31		ns
Reverse recovery charge	Q_{rr}	V_{DS}=400V, I_S=70A, V_{GS}=V_{JGS}=0V, R_{JG}=0.7Ω di/dt=4400A/µs, T_J=150°C		433		nC
Reverse recovery time	t_{rr}			35		ns

Typical Performance - Dynamic with MOSFET gate as control terminal and V_{JGS}=0V

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
MOSFET input capacitance	C_{iss}	V_{DS}=400V, V_{GS}=0V, V_{JGS}=0V, f=100kHz		3340		pF
Output capacitance	C_{oss}			230		
Reverse transfer capacitance	C_{rss}			1.4		
Effective output capacitance, energy related	$C_{oss(er)}$	V_{DS}=0V to 400V, V_{GS}=0V, V_{JGS}=0V		286		pF
Effective output capacitance, time related	$C_{oss(tr)}$			605		pF
C_{OSS} stored energy	E_{oss}	V_{DS}=400V, V_{GS}=0V, V_{JGS}=0V		23		µJ
Total Gate charge	Q_G	V_{DS}=400V, I_D=70A, V_{JGS}=0V, V_{GS} = 0V to 15V		75		nC
Gate-drain charge	Q_{GD}			13		
Gate-source charge	Q_{GS}			22		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6 V_{DS}=400V, I_D=70A, V_{GS}=0V to +15V, R_{G_ON}=1Ω, R_{G_OFF}=10Ω, R_{JG_ON}=0.7Ω, R_{JG_OFF}=4.7Ω, Inductive Load, FWD: same device with V_{GS} = 0V, R_G =10Ω, V_{JGS}=0V, R_{JG}=0.7Ω, T_J=25°C		26		ns
Rise time	t_r			21		
Turn-off delay time	$t_{d(off)}$			112		
Fall time	t_f			42.5		
Turn-on energy	E_{ON}			1135		µJ
Turn-off energy	E_{OFF}			1013		
Total switching energy	E_{TOTAL}			2148		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6 V_{DS}=400V, I_D=70A, V_{GS}=0V to +15V, R_{G_ON}=1Ω, R_{G_OFF}=10Ω, R_{JG_ON}=0.7Ω, R_{JG_OFF}=4.7Ω, Inductive Load, FWD: same device with V_{GS} = 0V, R_G =10Ω, V_{JGS}=0V, R_{JG}=0.7Ω, T_J=150°C		24		ns
Rise time	t_r			25		
Turn-off delay time	$t_{d(off)}$			114		
Fall time	t_f			40		
Turn-on energy	E_{ON}			1170		µJ
Turn-off energy	E_{OFF}			953		
Total switching energy	E_{TOTAL}			2123		

5. Measured with the half-bridge mode switching test circuit in Figure 23.

6. Devices are driven with the ClampDRIVE method as descriped in the section "Recommended Gate Drive Approach: ClampDRIVE method".

Typical Performance - Dynamic with JFET gate as control terminal and V_{GS}=+12V

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
JFET input capacitance	C_{Jiss}	V_{DS}=400V, V_{JGS}=-20V, f=100kHz		1965		pF
JFET output capacitance	C_{Joss}			226		
JFET reverse transfer capacitance	C_{Jrss}			222		
JFET total gate charge	Q_{JG}	V_{DS}=400V, I_D=70A, V_{JGS} = -18V to 0V		304		nC
JFET gate-drain charge	Q_{JGD}			159		
JFET gate-source charge	Q_{JGS}			50		

Typical Performance Diagrams - MOSFET gate as control terminal and V_{JGS}=0V

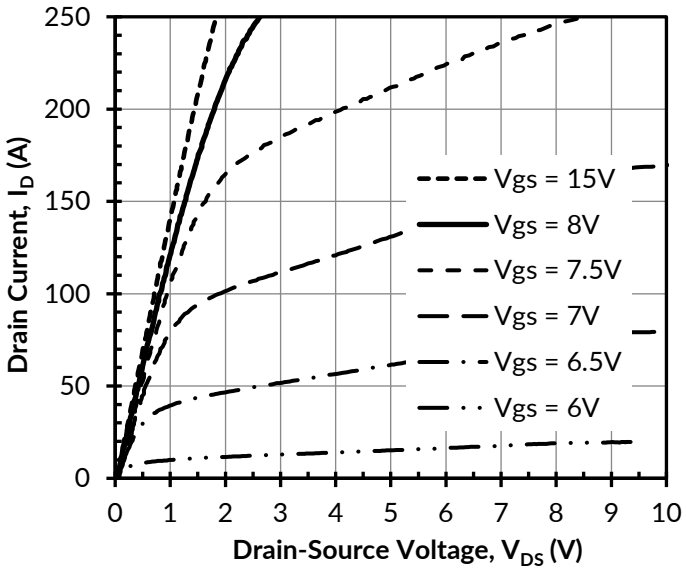


Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250µs

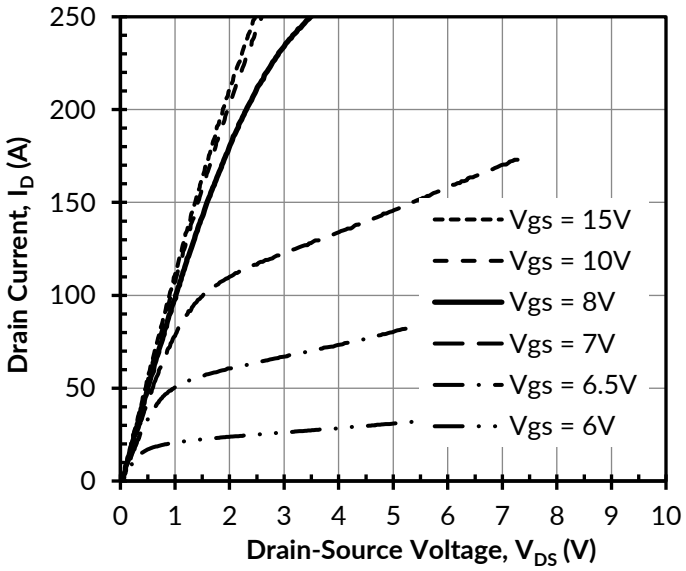


Figure 2. Typical output characteristics at T_J = 25°C, tp < 250µs

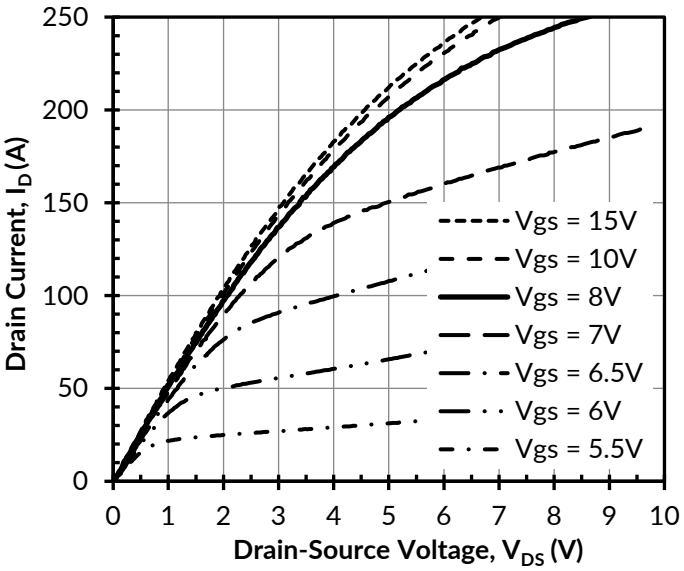


Figure 3. Typical output characteristics at T_J = 175°C and tp < 250µs

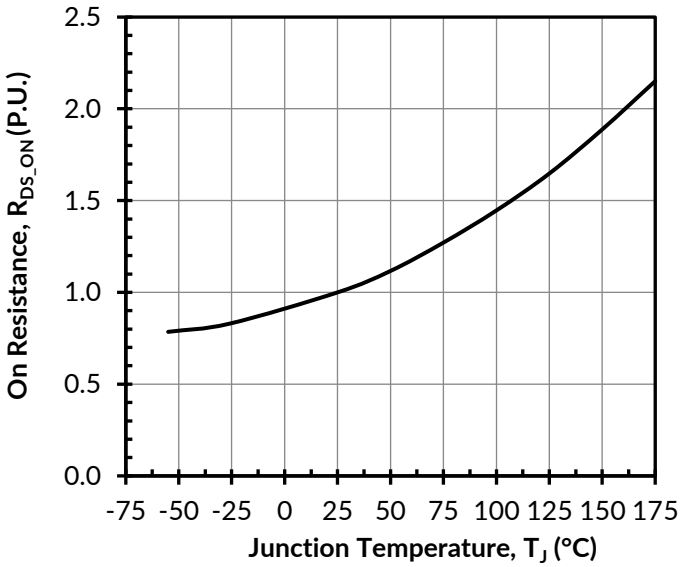


Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 70A

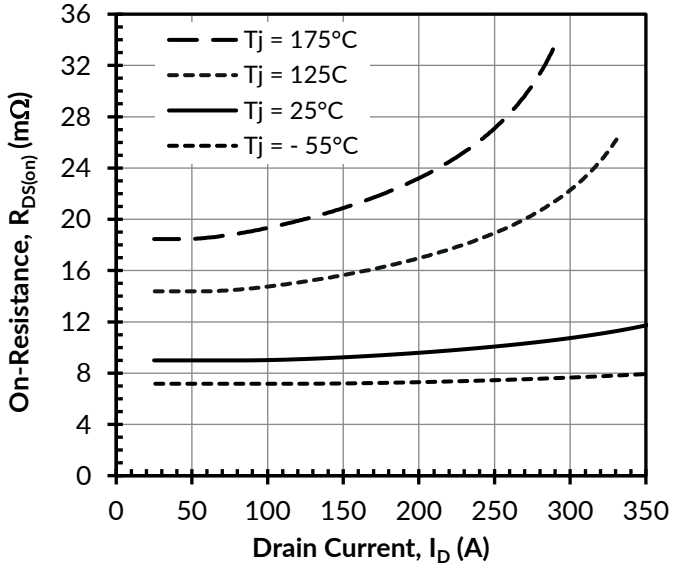


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

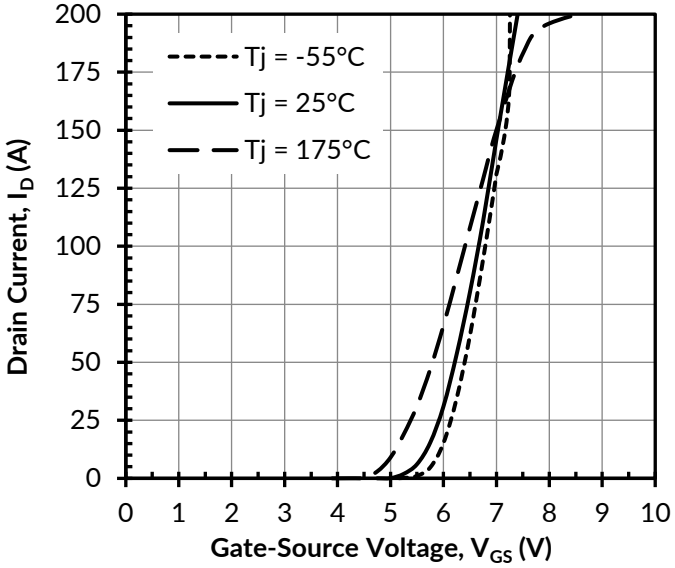


Figure 6. Typical transfer characteristics at V_{DS} = 5V

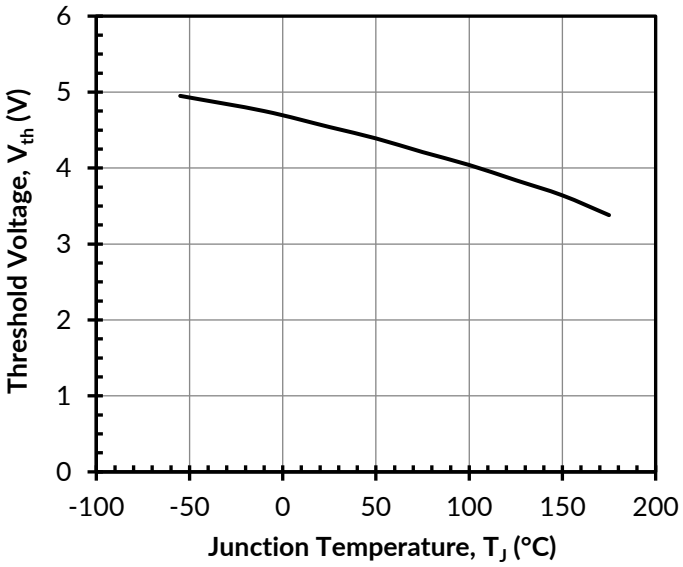


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_D = 10mA

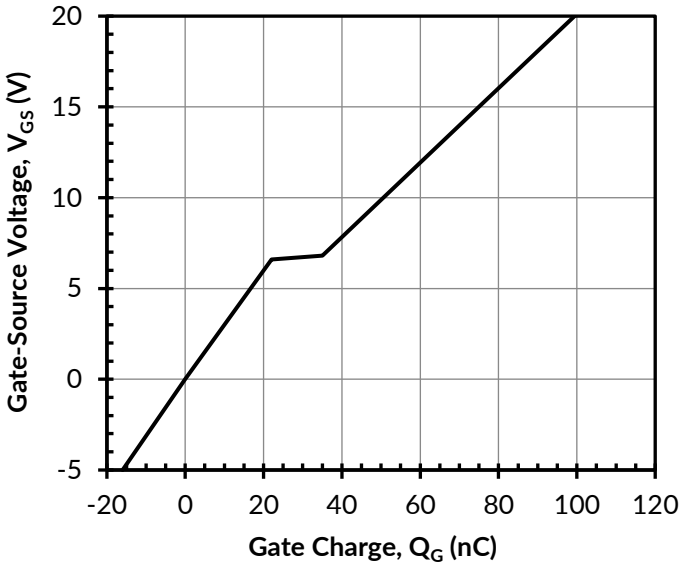


Figure 8. Typical gate charge at V_{DS}=400V and I_D = 70A

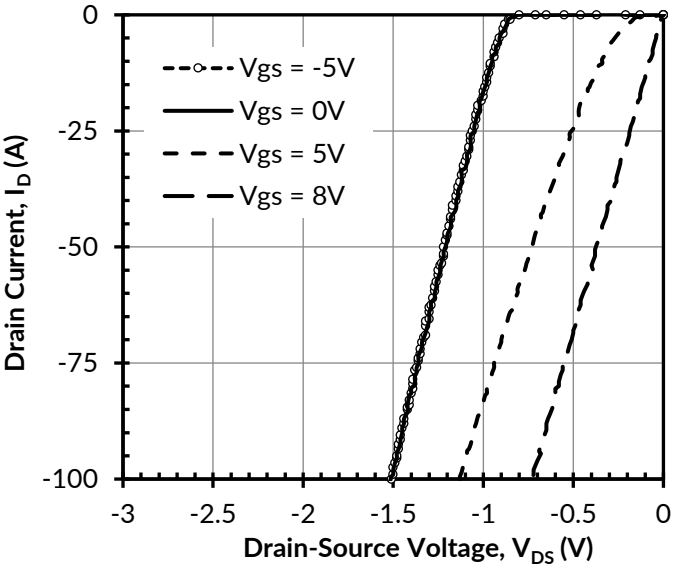


Figure 9. 3rd quadrant characteristics at T_J = -55°C

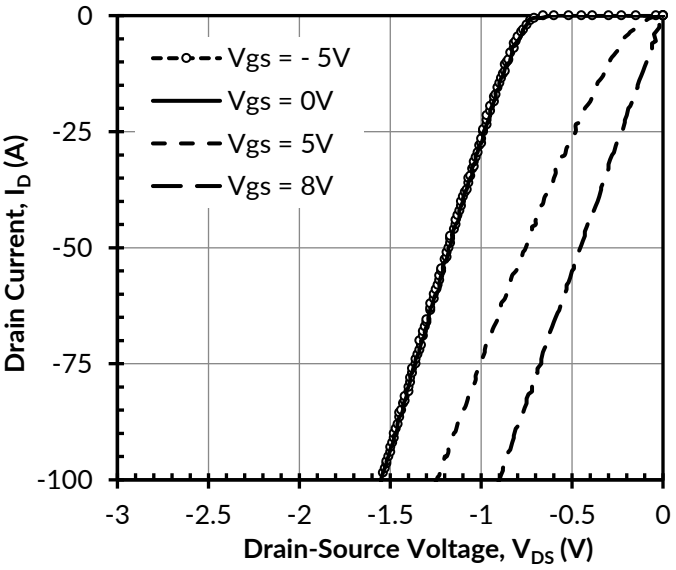


Figure 10. 3rd quadrant characteristics at T_J = 25°C

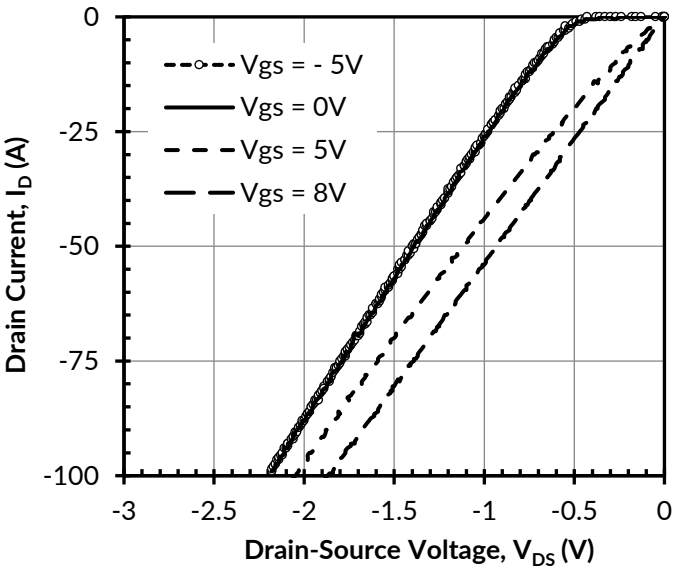


Figure 11. 3rd quadrant characteristics at T_J = 175°C

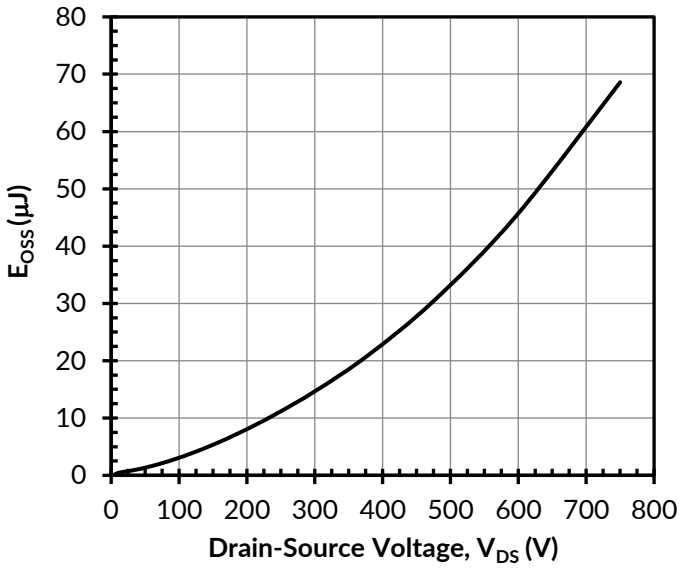


Figure 12. Typical stored energy in C_{OSS} at V_{GS} = 0V

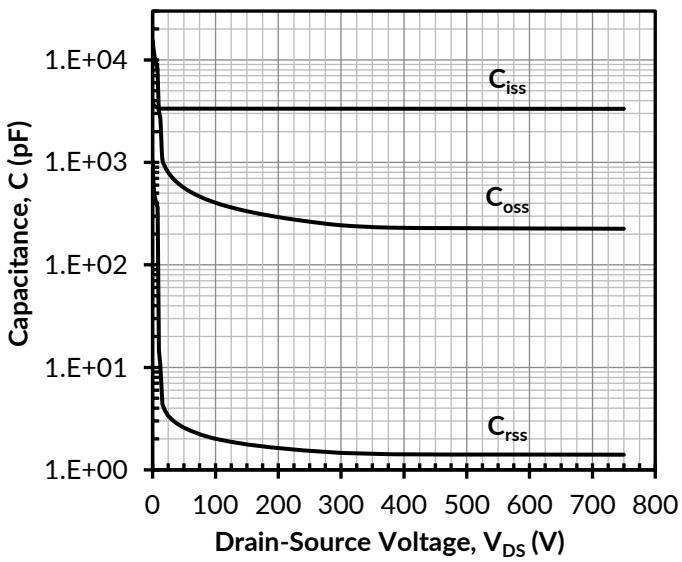


Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

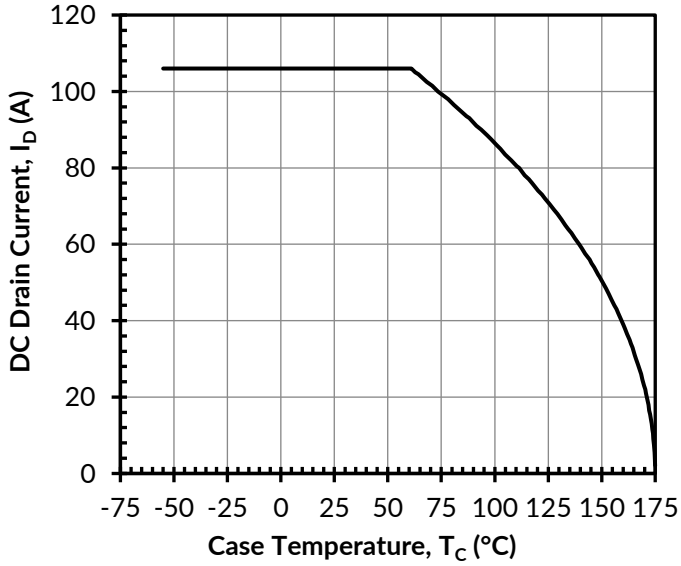


Figure 14. DC drain current derating

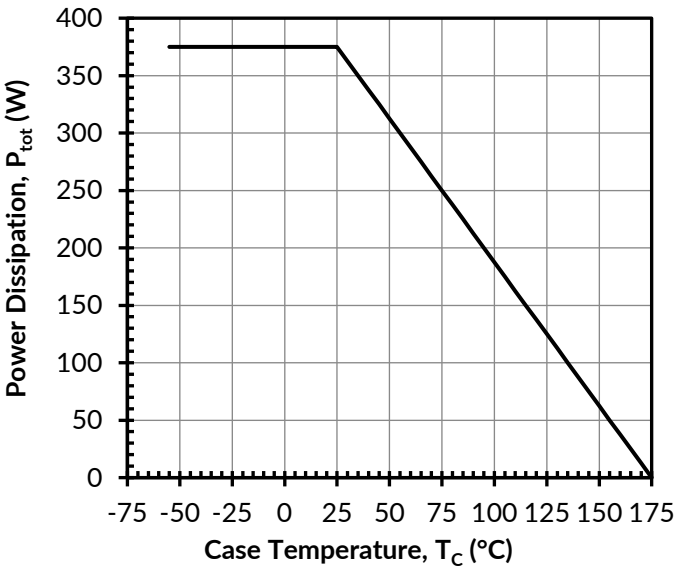


Figure 15. Total power dissipation

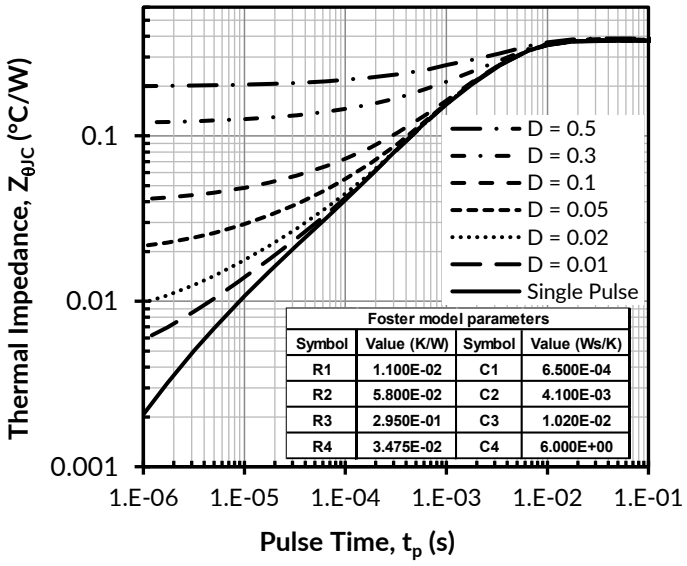


Figure 16. Maximum transient thermal impedance

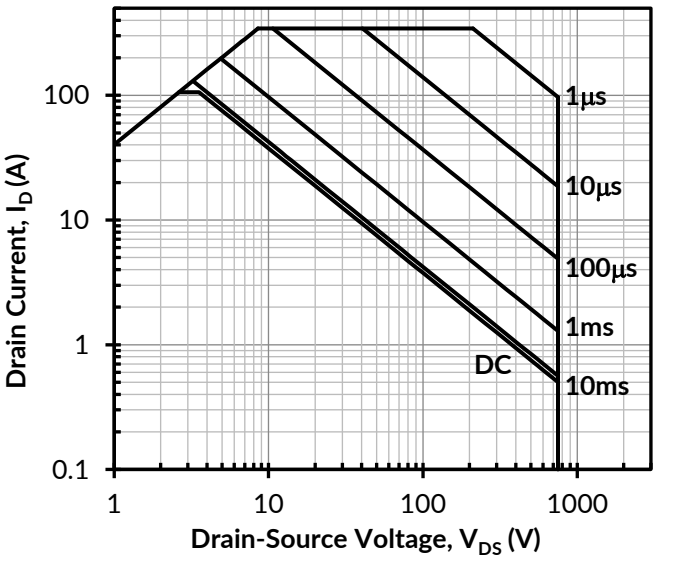


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

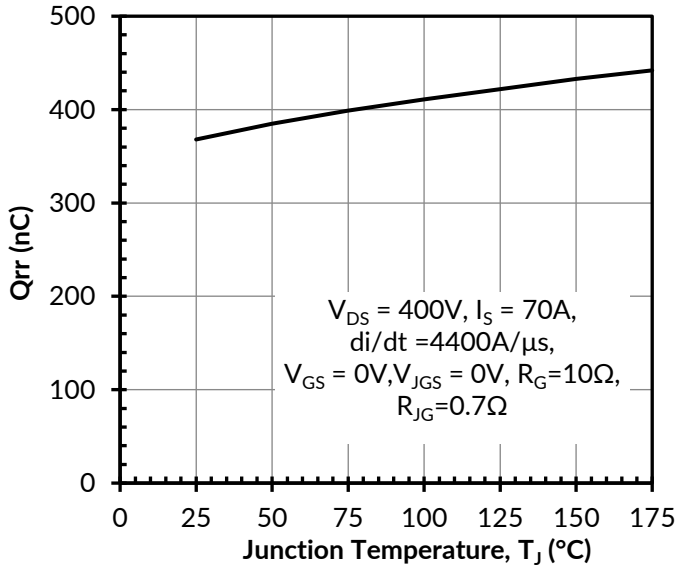


Figure 18. Reverse recovery charge Qrr vs. junction temperature

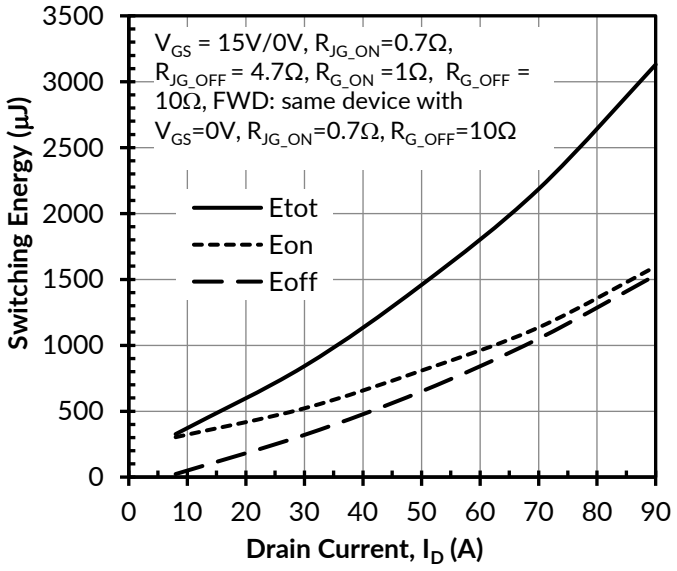


Figure 19. Clamped inductive switching energy vs. drain current at V_{DS} =400V and T_J = 25°C

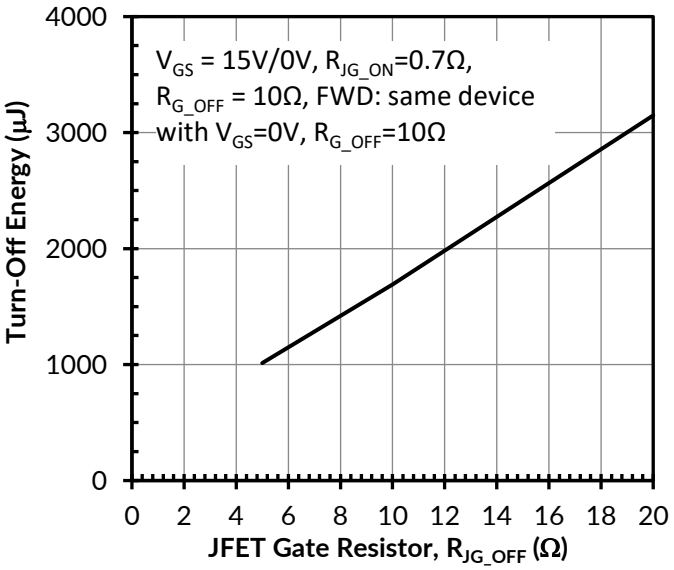


Figure 20. Clamped inductive switching energies vs. JFET gate resistor R_{JG_OFF} at V_{DS} = 400V, I_D =70A, and T_J = 25°C

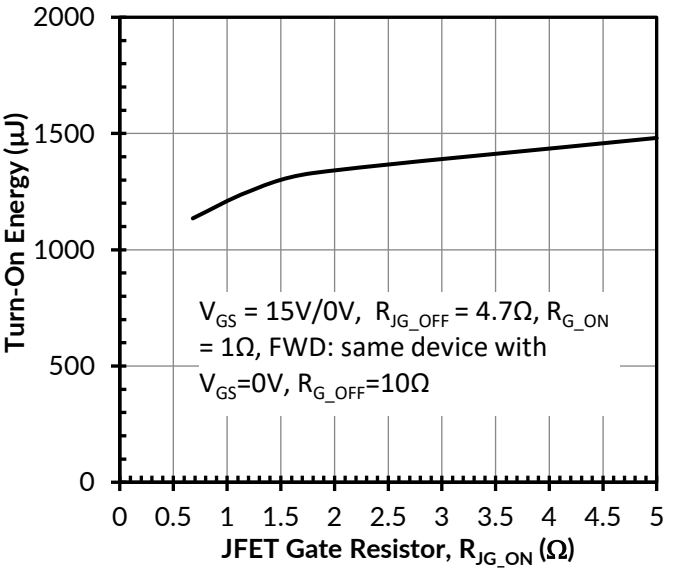


Figure 21. Clamped inductive switching energies vs. JFET gate resostor R_{JG_ON} at V_{DS} = 400V, I_D =70A, and T_J = 25°C

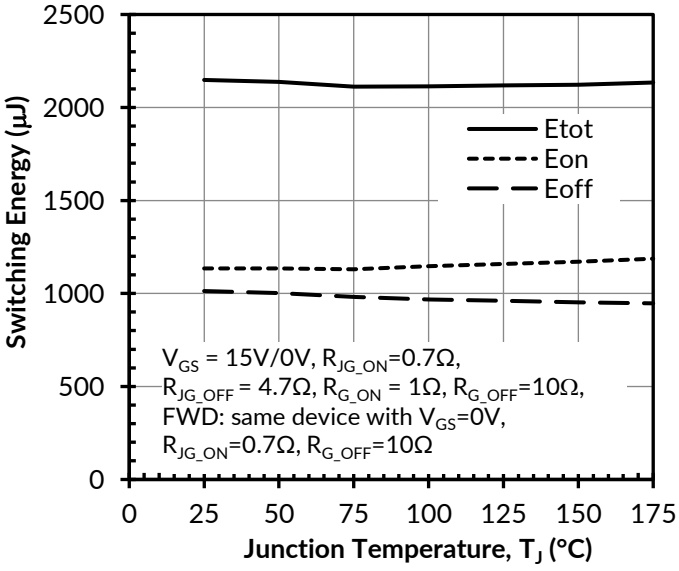


Figure 22. Clamped inductive switching energy vs. junction temperature at V_{DS} =400V and I_D =70A

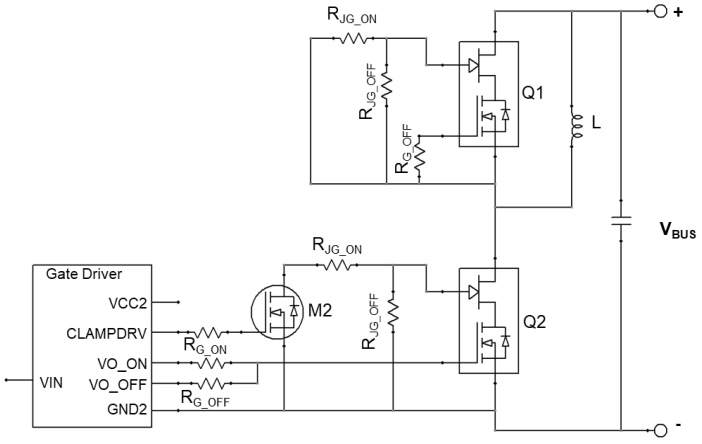


Figure 23. Schematic of the half-bridge mode switching test circuit with ClampDRIVE method.

Typical Performance Diagrams - JFET gate as control terminal and V_{GS}=+12V

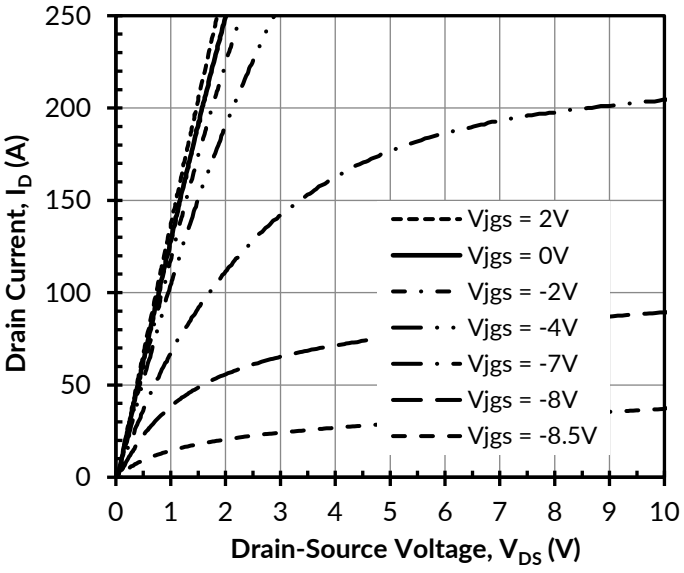


Figure 24. Typical output characteristics with JFET gate as control at T_J = - 55°C, t_p < 250µs

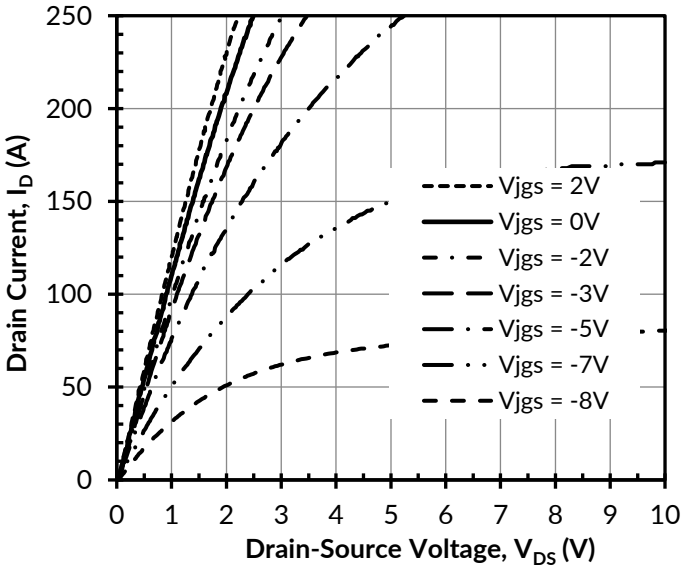


Figure 25. Typical output characteristics with JFET gate as control at T_J = 25°C, t_p < 250µs

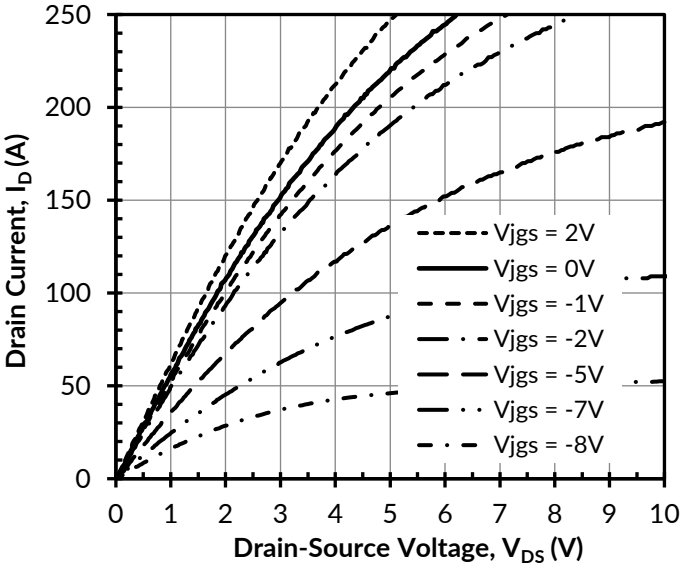


Figure 26. Typical output characteristics with JFET gate as control at T_J = 175°C, t_p < 250µs

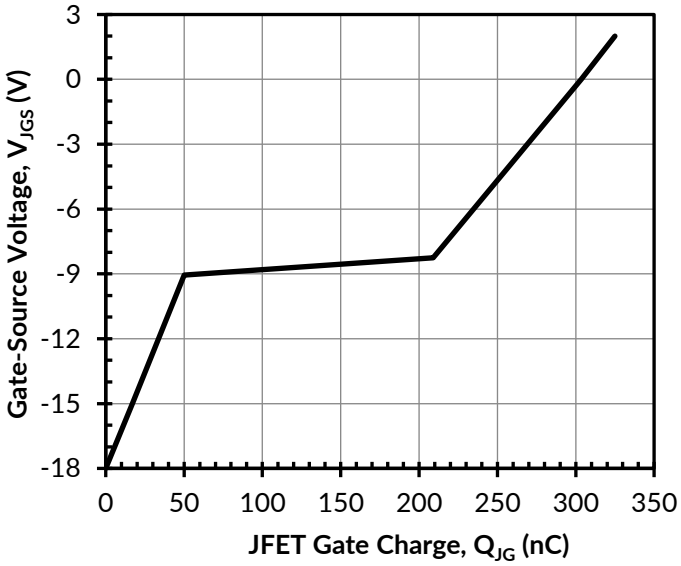


Figure 27. Typical JFET gate charge at V_{DS} = 400V and I_D = 70A

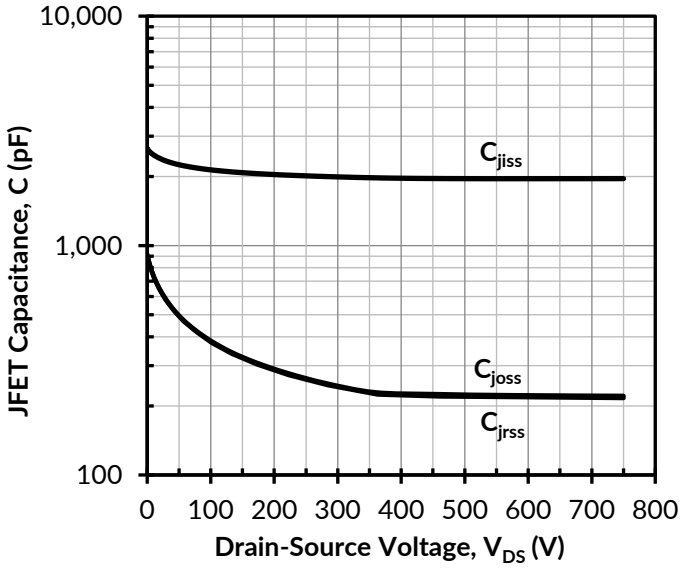


Figure 28. Typical JFET capacitances at f = 100kHz and V_{JGS} = -20V

Recommended Gate Drive Approach: ClampDRIVE method

Since both JFET gate and MOSFET gate are accessible, more parameters and approaches can be used to control the switching behavior of the device and make the device suitable for a wide range applications from solid state circuit breakers requiring ultra-high current turn-off capability to motor drives requiring well controlled switching speed. The recommended gate drive approach is the ClampDRIVE method, with which the desired turn-on speed, turn-off speed and reverse recovery performance can be achieved at the same time. The main idea of this method is to dynamically tune the JFET gate resistor value R_{JG} such that, in the off-state, R_{JG} is small enough not to cause a reverse recovery issue, and during turn-off transient, R_{JG} is set to a higher value for the desired turn-off performance. This method can be easily implemented using a commercial off-the-shelf gate driver with miller clamp pre-driver output, as illustrated in Figure A. VIN is the gate driver input signal. VO is the gate driver output and CLAMPDRV is the gate driver miller clamp pre-driver output. M2 is the clamp MOSFET used to control the JFET gate resistance. The MOSFET M2 is directly controlled by the CLAMPDRV signal.

In the on-state, CLAMPDRV is low which turns the MOSFET M2 off, thus, the effective JFET gate resistance is R_{JG_OFF}. During the turn-off transient, CLAMPDRV is kept low until the device is fully off. This means the JFET gate resistance is R_{JG_OFF} during the turn-off process, and R_{GJ_OFF} can be used to effectively control turn-off speed. After the device is fully off, CLAMPDRV is changed to high level, which turns the MOSFET M2 on.

In the off-state, CLAMPDRV is high and the clamp MOSFET M2 is in on-state. The effective JFET gate resistance is equal to the parallel combination of R_{JG_OFF} and R_{JG_ON}. R_{JG_ON} can be selected small enough to prevent the reverse recovery issue. During the turn-on transient, the JFET gate current may flow from the cascode source through the body diode of the MOSFET M2 and R_{JG_ON} into the JFET gate, so, the turn-on process is also determined by R_{JG_ON}.

In summary, the optimum switching performance of the SiC cascode FETs can be realized with the ClampDRIVE method by selecting proper JFET gate resistors R_{JG_ON} and R_{JG_OFF}.

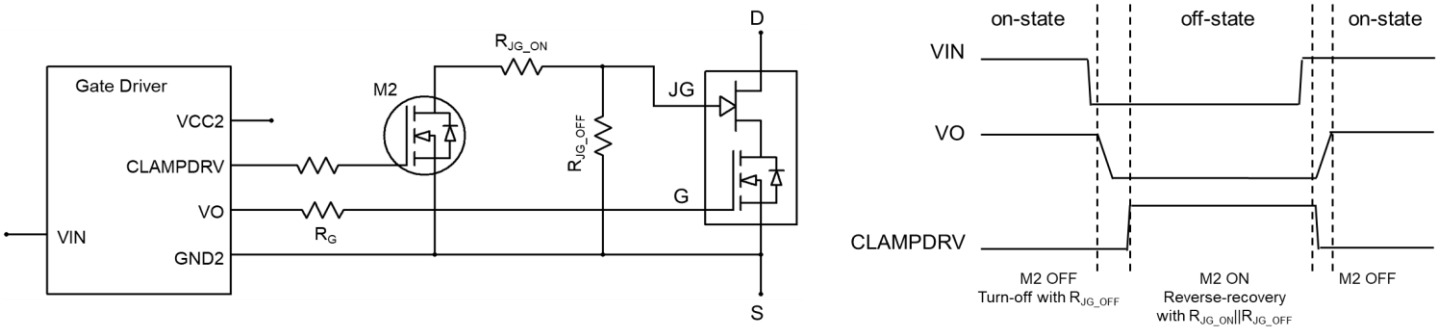


Figure A. Circuit schematic and timing diagram of the ClampDRIVE method

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