APPLICATION NOTE

APH5801

QM3582x Hardware Design Guide

Referenced Documents

The reference documents below take precedence over the contents of this application note, and should always be consulted for the latest information:

QM35822S / QM35825 Data Sheet

APH001 and APH301 Application Notes provide general recommendations about power management, capacitive decoupling, RF connectors, RF layout, antenna design and placement, and electromagnetic interferences. It should also be consulted before starting a design.

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1 Overview

1.1 Introduction

This document provides guidelines for the hardware design of systems based on QM35825 and QM35822S UWB SoCs.

Included are the application circuit schematic, the recommended pin assignment, the power supply scheme, some PCB layout guidelines based on the QM3582x evaluation boards, and some recommendations for component placement.

The main difference between the two SoCs is the number of RF ports. The QM35825 has 4 RF ports, while the QM35822S has 2 RF ports.

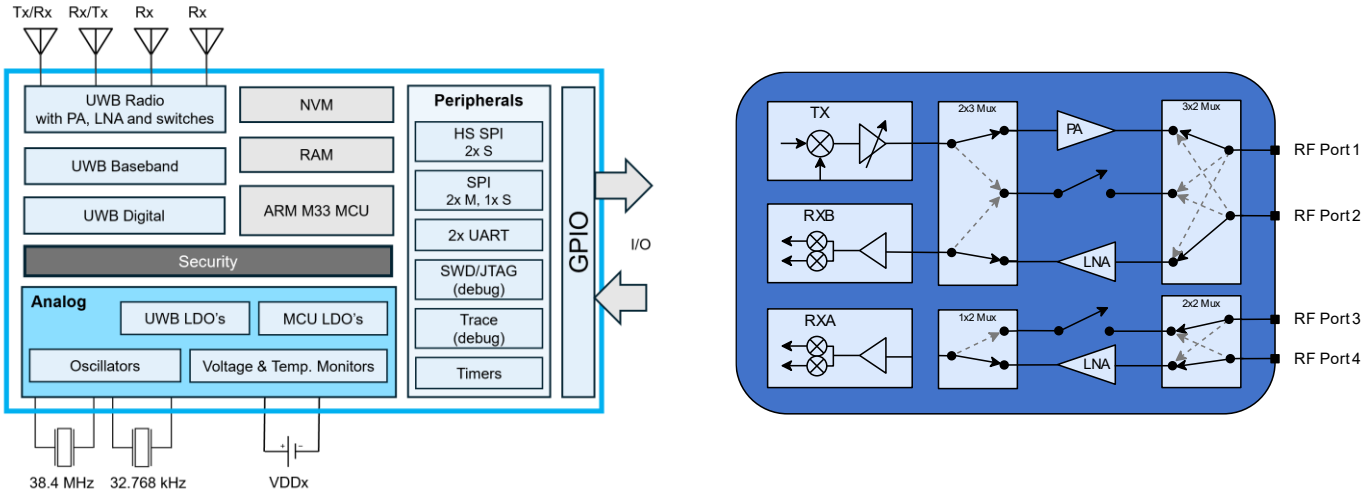


Figure 1: QM35825: DSMBGA-74 (3.38x4.08x0.624 mm)

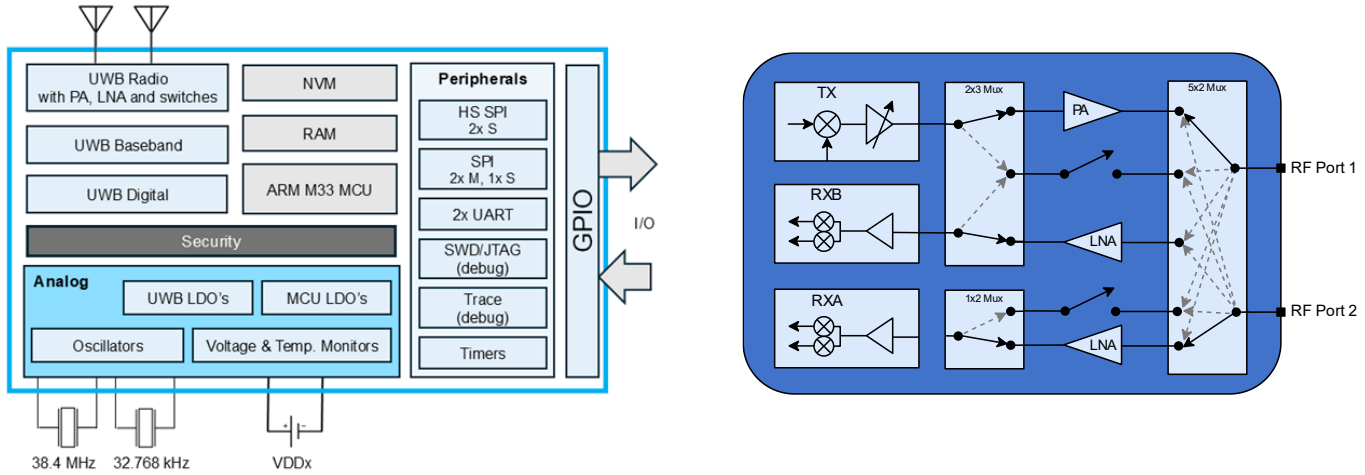


Figure 2: QM35822S: DSMBGA-74 (3.38x4.08x0.630 mm)

1.2 System Block Diagram

The following functional diagram illustrates a typical application based on the QM3582x SiP.

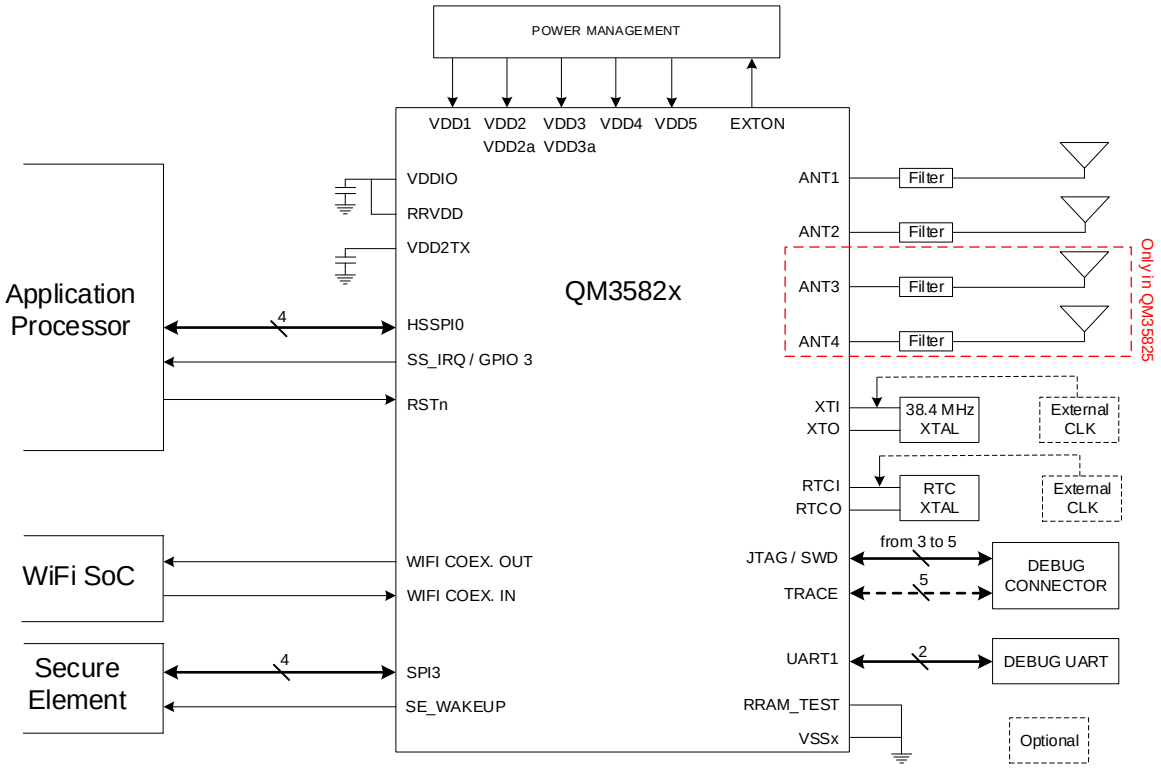


Figure 3: QM3582x System Block Diagram

Below is an example of how to connect the four RF ports of the QM35825 in the context of a 3D-AoA application.

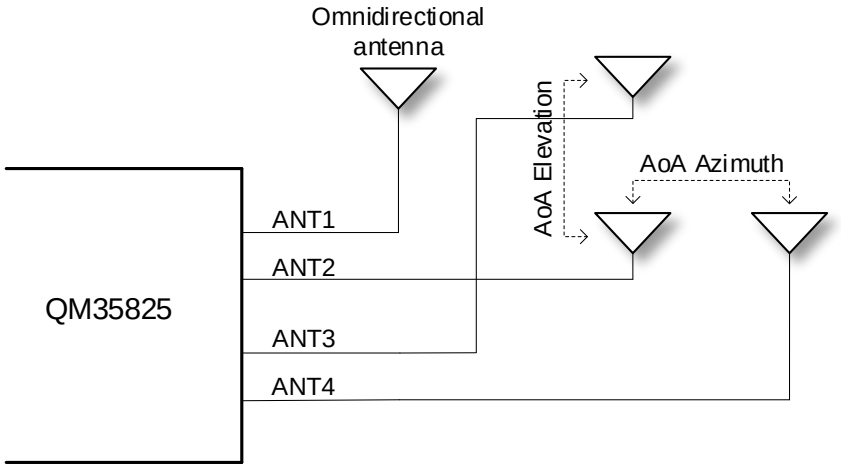


Figure 4: Typical 3D-AoA connections

2 Application Circuits

2.1 QM35822S Application Circuit (1.8V IO)

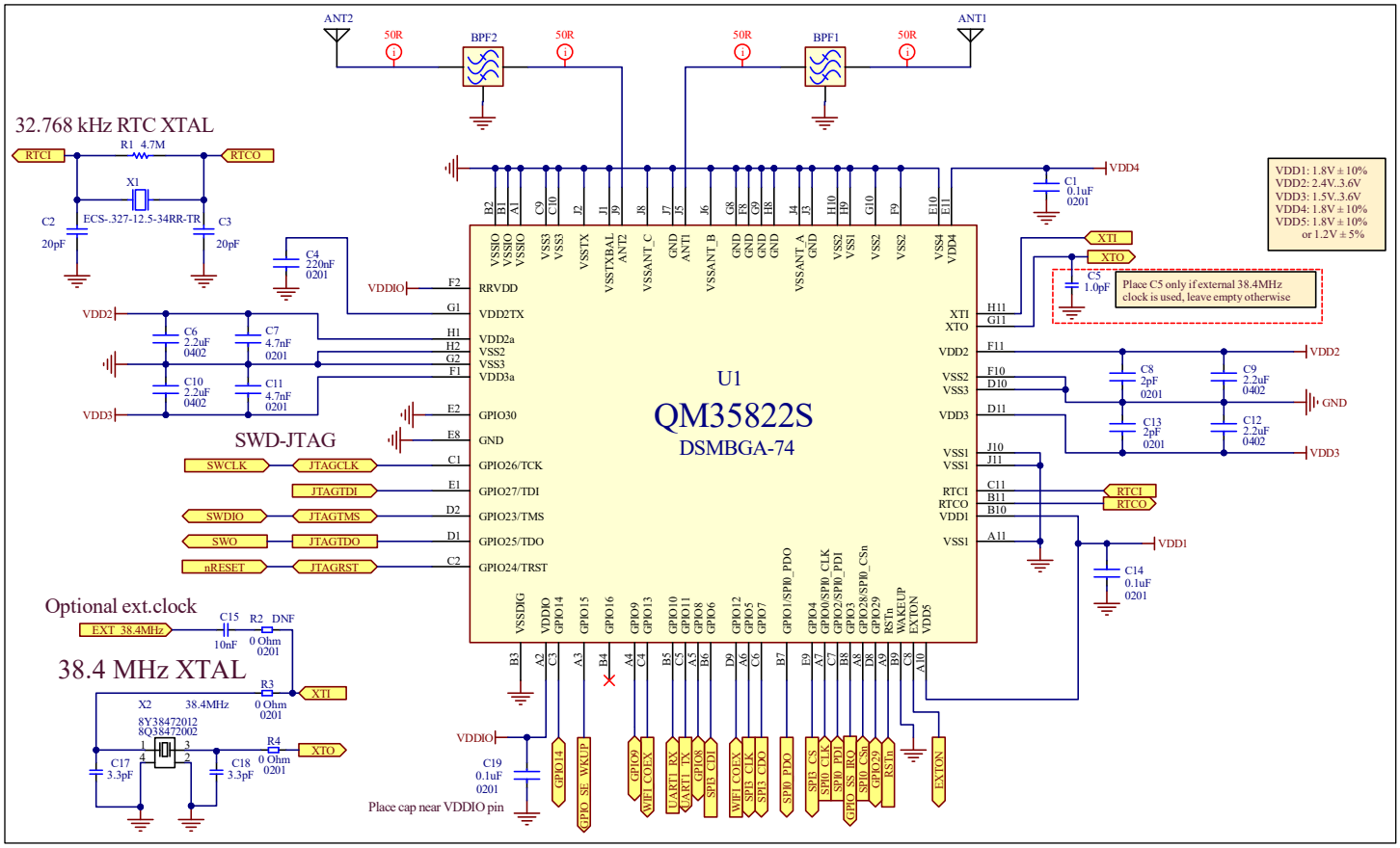


Figure 5: QM35822S Application Circuit (1.8V IO)

2.2 QM35822S Application Circuit (1.2V IO)

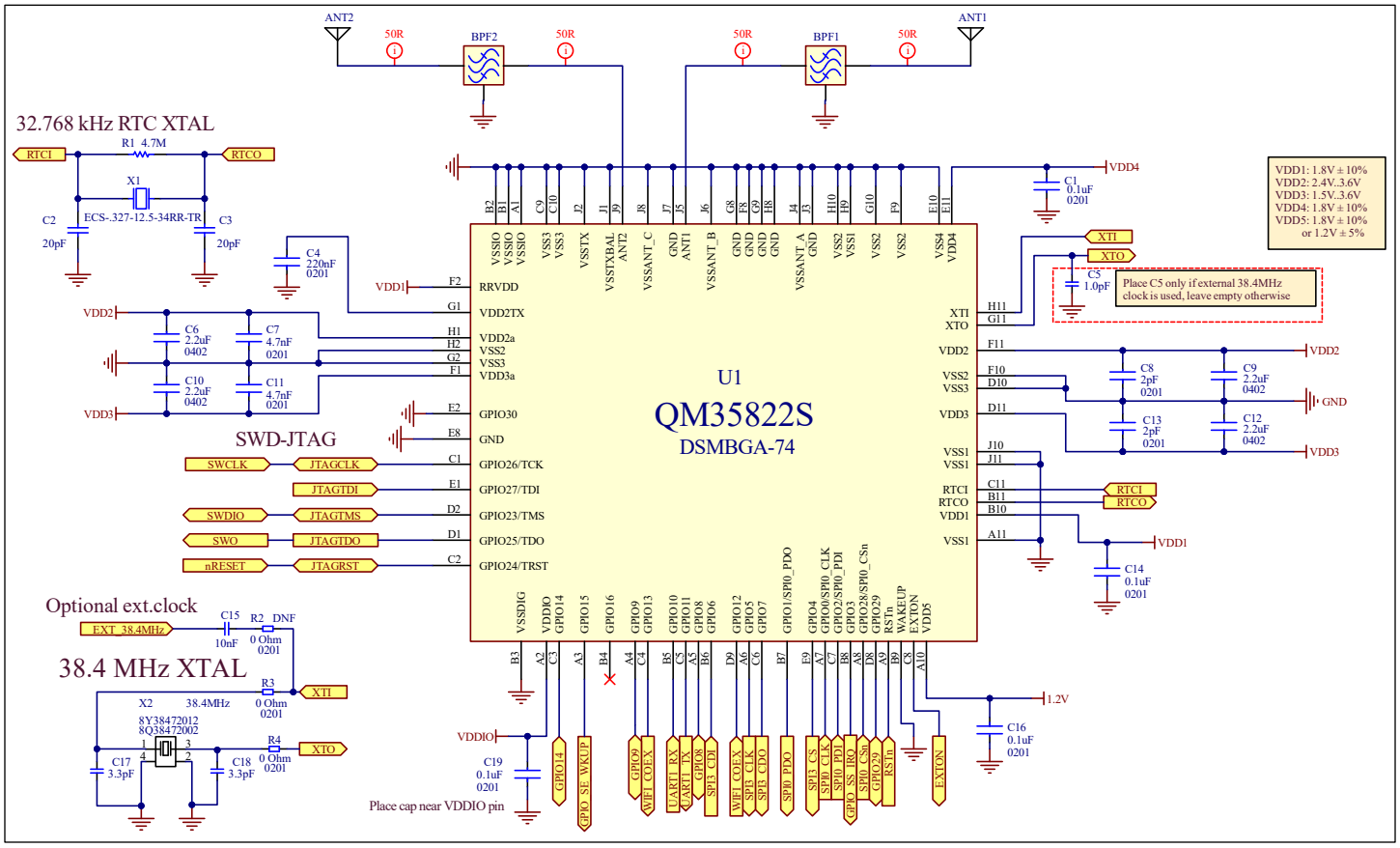


Figure 6: QM35822S Application Circuit (1.2V IO)

2.3 QM35825 Application Circuit

Same as QM35822S application circuit where just the antenna pins/connections are as below:

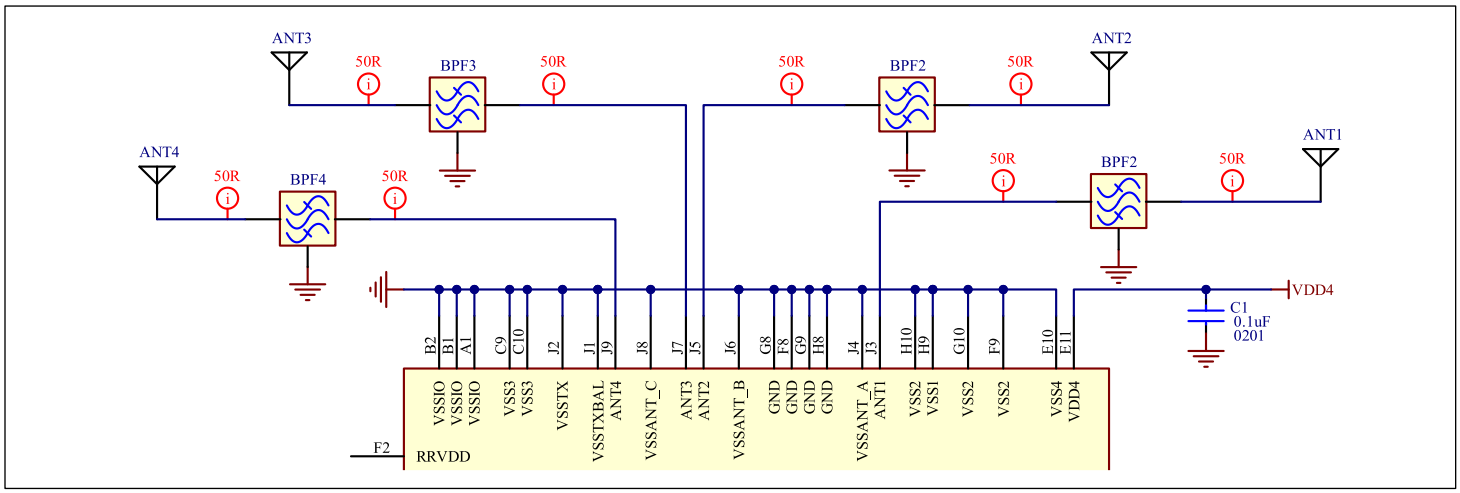


Figure 7: QM35825 Application Circuit

2.4 Recommended Pin Assignment

Pin Name	Function		Alternate 1		Comments
GPIO0	HSSPI0_CLK	I			
GPIO1	HSSPI0_PDO	O			This pin will float in SLEEP and DEEPSLEEP preventing the host from receiving a predictive message when trying to communicate with the QM3582x
GPIO2	HSSPI0_PDI	I			
GPIO3	SS_IRQ	O			Notification to Host in HSSPI0 mode. This pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low.
GPIO4	SPI3_CS	O			SPI3: to be connected to a Secure Element UART0: can be used to log debug info
GPIO5	SPI3_CLK	O			
GPIO6	SPI3_CDI	I	UART0_TX (debug)	O	
GPIO7	SPI3_CDO	O	UART0_RX (debug)	I	
GPIO8	GPIO	I/O	LED	O	
GPIO9	GPIO	I/O	LED	O	
GPIO10	UART1_RX	I			
GPIO11	UART1_TX	O			
GPIO12	WIFI COEX IN	I	LED	O	
GPIO13	WIFI COEX OUT	O	LED	O	
GPIO14	GPIO	O			
GPIO15	SE_WAKEUP	O			
GPIO16	GPIO	I/O			Reserved – Do not connect
GPIO17	RFUBUS0	I/O			For QM35725, RFUBUSx and RF_CTRLx are internal signals that manage LNA, PA and RF switches of the RF Front End
GPIO18	RFUBUS1	I/O			
GPIO19	RF_CTRL0	O			
GPIO20	RF_CTRL1	O			
GPIO21	RF_CTRL2	O			
GPIO22	RF_CTRL2	O			
GPIO23	JTAG_TMS/SWDIO	I/O			
GPIO24	JTAG_RST	I			
GPIO25	JTAG_TDO/SWO	O			
GPIO26	JTAG_TCK/SWCLK	I			
GPIO27	JTAG_TDI	I			
GPIO28	HSSPI0_CSn	I			When GPIO28 is low at start-up, the MCU enters in Rom Code Command Mode
GPIO29	GPIO	O			

Table 1: Recommended Pin Allocation

2.5 High Speed SPI0 interface

HS SPI0 is strictly required. This interface allows communication to the boot ROM code and the main application.

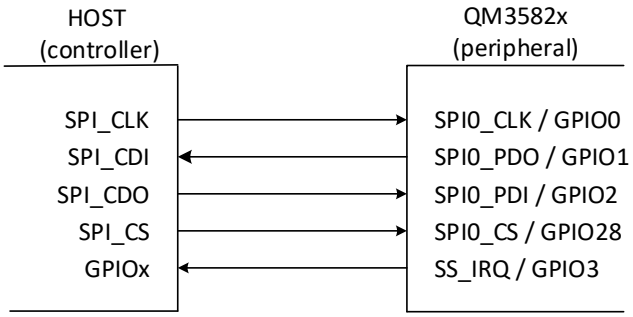


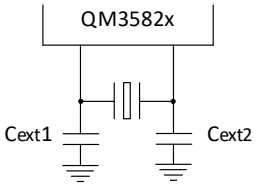
Figure 8: High Speed SPI0 interface

SS_IRQ: this pin will float in SLEEP and DEEPSLEEP states and may cause spurious interrupts unless pulled low. Either the host processor can configure its GPIO as an input with pull-down or a 100K pull-down can be added to this signal.

SPI0_PDO: this pin will float in SLEEP and DEEPSLEEP states. To avoid the host receiving an unpredictive message when attempting to communicate with the QM3582x, it is recommended that either the host processor configures its GPIO as an input with pull-down or that a 100K pull-down be added to this signal.

2.6 Clock source

2.6.1 On-chip RF oscillator (e.g. 38.4MHz):



See the QM3582x datasheet for calculation of external capacitors C_{EXT}.

C_{EXT} value should be chosen to have no clock offset when the crystal trim register of the QM3582x is set to its middle value. Thus, the trim facility can provide a variation of XTI/XT0 connection capacitance from 0 to 8pF allowing the adjustment of the clock frequency of each unit during production stage.

A good starting estimate for C_{EXT} is approximately 3.3pF. The value can be adjusted by measuring the UWB carrier frequency using the QM3582x Continuous Wave mode.

2.6.2 External RF oscillator (e.g. 38.4MHz):

When an external oscillator is connected to XTI input, a 10nF AC coupling capacitor should be added.

In addition, a 1pF capacitor should be connected between XTO pin and ground.

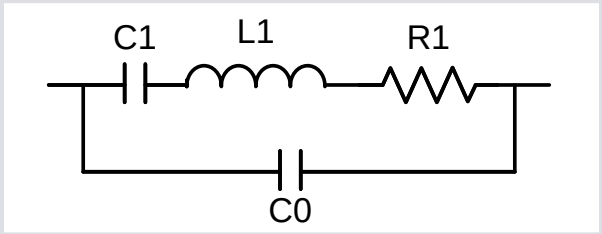
2.6.3 Real Time Clock (RTC)

If low power mode during TWR is not required, the RTC crystal can be omitted. In this case RTCI and RTCO pins should be connected to ground through a 1pF capacitor.

Note that while it is theoretically possible to omit the RTC crystal, the current Qorvo SDK is not compatible with a platform without an RTC clock.

Crystal procurement specification:

Crystal specifications are defined according to the following crystal representation:



Specification	Value
Nominal frequency	32.768 kHz
Oscillation mode	Fundamental
Load capacitance (CL) crystal	12.5 pF For external load capacitors, please refer to the application circuit section
Resistance (R1)	See the table below. The maximum R1 should take into consideration: temperature dependency, drive level dependency and aging effects.
Shunt Capacitance (C0)	See the table below.
Drive Level	0.1 µW
Operating temperature range	-40 … +85 °C (depending on application) -40 … +90 °C (extended range)
Frequency Tolerance	If using Qorvo software, initial frequency offsets are automatically compensated during startup of the application SW.
Initial offset at 25 °C	+/- 200 ppm
Aging 1st year	+/- 3 ppm
Parabolic Curvature Constant	≥ -0.04 [ppm/°C^2]
Turnover Temperature	25 +/- 5 °C

Table 2: RTC Crystal Specifications

Shunt Capacitance (C0) / Resistance (R1) Combinations							Unit
C0	0.5	0.7	1.0	1.2	1.8	2.5	pF
Max. R1	56.3	54.5	52	50.5	46	42.3	kΩ

Table 3: Allowed Shunt Capacitance / Resistance Combinations

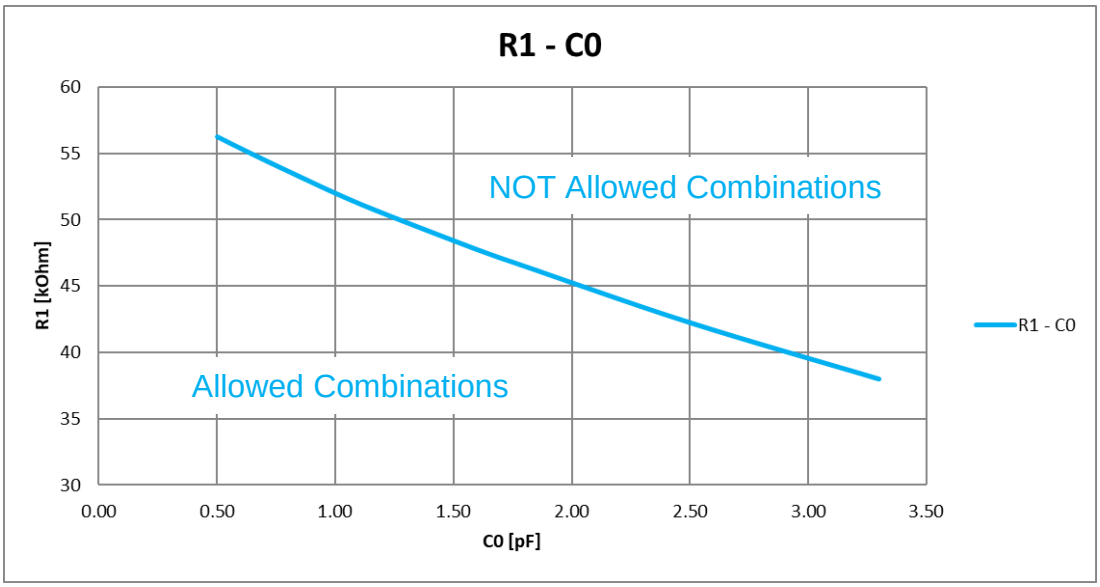


Figure 9: Allowed C0 / R1 Combinations

Examples of suitable crystals:

- ECS Inc. ECS-.327-12.5-34RR-TR
- TXC 9H03270092

2.7 Debug interface

It is highly recommended to make the JTAG/SWD port accessible to facilitate hardware and firmware debugging at least on the initial versions of the PCB.

Pinout of JTAG / SWD debug connector

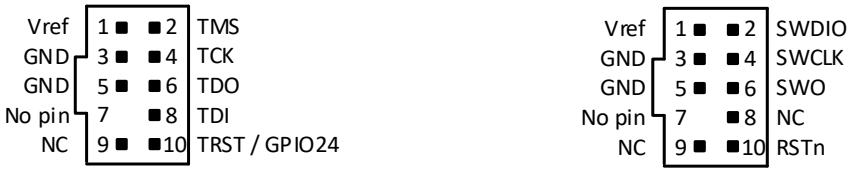


Figure 10: Pinout of JTAG / SWD connector

Vref is the target reference voltage. It is used to check that the target is powered and to control the output logic level to the target. It should be connected to VDD1 (that internally powers VDDIO rail of the QM3572x)

Reference of 9-pin header: FTSH-105-01-L-DV-007-K

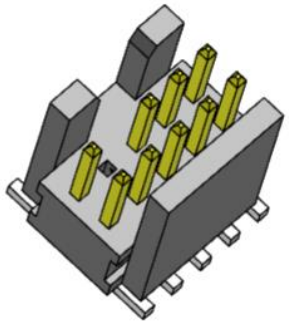


Figure 11: 3D View of Debug Connector

2.8 Test Points

It is highly recommended to add test points to the following signals particularly on the initial version of the PCB. This will facilitate hardware and firmware debugging.

- GPIO0/HSSPI0_CLK
- GPIO1/HSSPI0_PDO
- GPIO2/HSSPI0_PDI
- GPIO28/HSSPI0_CSn
- GPIO3/SS_IRQ,
- GPIO12/WIFI COEX IN (optional)
- GPIO13/WIFI COEX OUT (optional)
- RSTn
- EXTON

3 PCB Layout Considerations

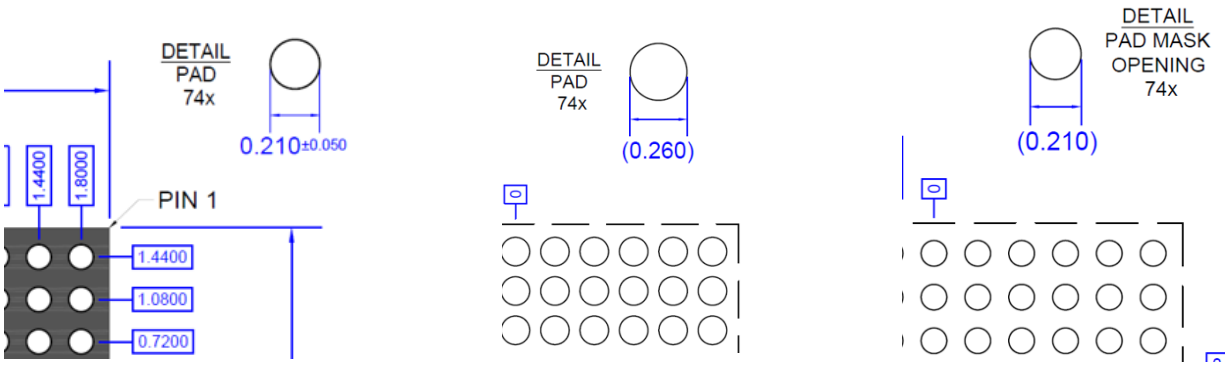
3.1 PCB Technology

The following technology has been implemented in the QM3582x Radio Boards:

Parameter	Notes
Number of layers	6 layers
Substrate material	FR4
Stack-up	See the figure below
Minimum trace width	0.125 mm
Minimum line spacing	0.125 mm
QM3582x pad geometry	SMD (Solder Mask Defined - the solder mask opening is smaller than the metal pad) See dimensions in the Pad Geometry section
Via	L1 to L6 Drill hole diameter: 0.254 mm - Pad diameter: 0.61 mm
Micro via	L1 to L2, L2 to L3 (see figure below) Drill hole diameter: 0.1 mm - Pad diameter: 0.2 mm Via in pad and via filling under the BGA
Pad finish	ENIG (Electroless Ni Immersion Gold)

Table 4: PCB Technology

3.2 QM3582x Pad Geometry



Solder Bump | Copper Pad | Solder Mask opening

Figure 12: QM3582x Pad Geometry

3.3 Stack-up

Stack-up and via structure of the QM3582x Radio Board are shown in the figures below.

#	Name	Type	Thickness
	Top Overlay	Overlay	
	Top Solder	Solder Mask	0.02mm
1	L1-Top	Signal	0.035mm
	ISO-1	Prepreg	0.094mm
2	L2	Signal	0.035mm
	ISO-2	Prepreg	0.092mm
3	L3-SignalNS	Signal	0.035mm
	ISO-3	Core	1.03mm
4	L4-Ground	Signal	0.035mm
	ISO-4	Prepreg	0.094mm
5	L5-Power	Signal	0.035mm
	ISO-5	Prepreg	0.094mm
6	L6-Bottom	Signal	0.035mm
	Bottom Solder	Solder Mask	0.02mm
	Bottom Overlay	Overlay	

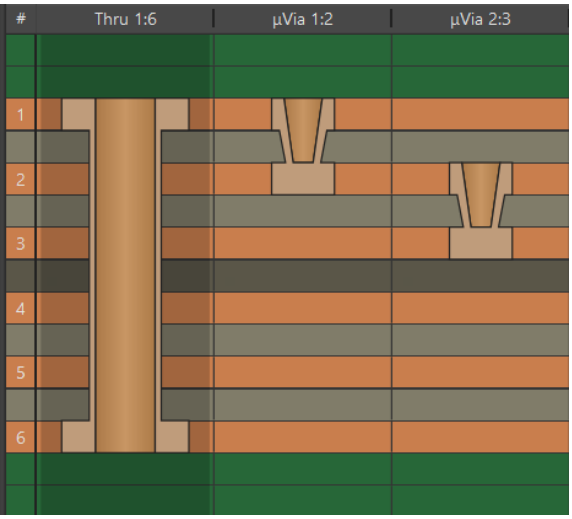


Figure 13: QM3582x Radio Board Via Structure

#	Name	Type	Material	Thickness	Dk	Weight
	Top Overlay	Overlay				
	Top Solder	Solder Mask	Solder Resist	0.02mm	3.7	
1	L1-Top	Signal		0.035mm		1oz
	ISO-1	Prepreg	S1000HB (3313)	0.094mm	4.48	
2	L2	Signal		0.035mm		1/2oz
	ISO-2	Prepreg	S1000HB (3313)	0.092mm	4.48	
3	L3-SignalNS	Signal		0.035mm		1/2oz
	ISO-3	Core	S1000H	1.03mm	4.74	
4	L4-Ground	Signal		0.035mm		1/2oz
	ISO-4	Prepreg	S1000HB (3313)	0.094mm	4.48	
5	L5-Power	Signal		0.035mm		1/2oz
	ISO-5	Prepreg	S1000HB (3313)	0.094mm	4.48	
6	L6-Bottom	Signal		0.035mm		1/2oz
	Bottom Solder	Solder Mask	Solder Resist	0.02mm	3.7	
	Bottom Overlay	Overlay				

Figure 14: QM3582x Radio Board Stack-up

3.4 Cutout in QM3582x PCB layout

In the areas shown below, copper, tracks and via's should be removed to a depth of 100 µm from the bottom of the chip once soldered. In most of the case, this means removing copper from the top layer in the area in question.

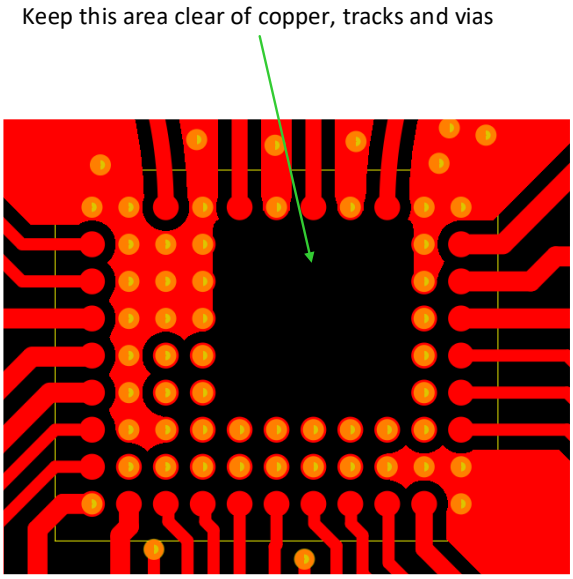


Figure 15: Cutout in QM3582x Layout

An opening should also be created in the solder mask as indicated in the image below.

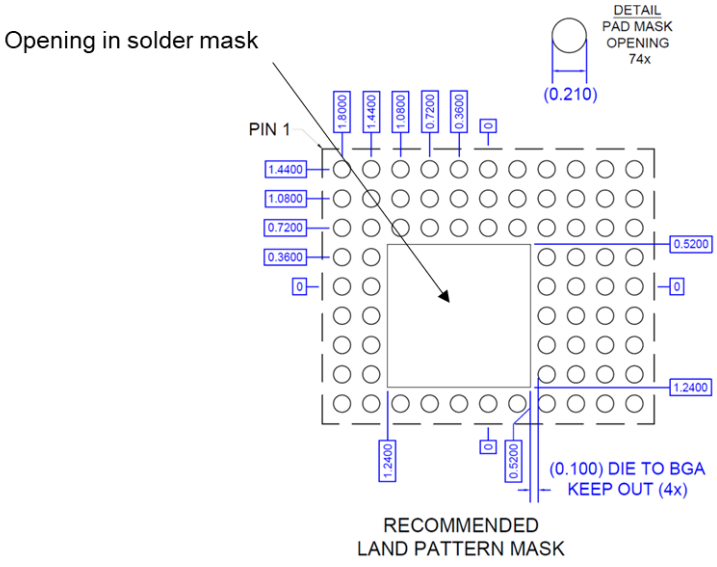


Figure 16: Opening in QM3582x Solder Mask

3.5 BGA Escape Routing

An example of escape routing scheme for each BGA is shown below.

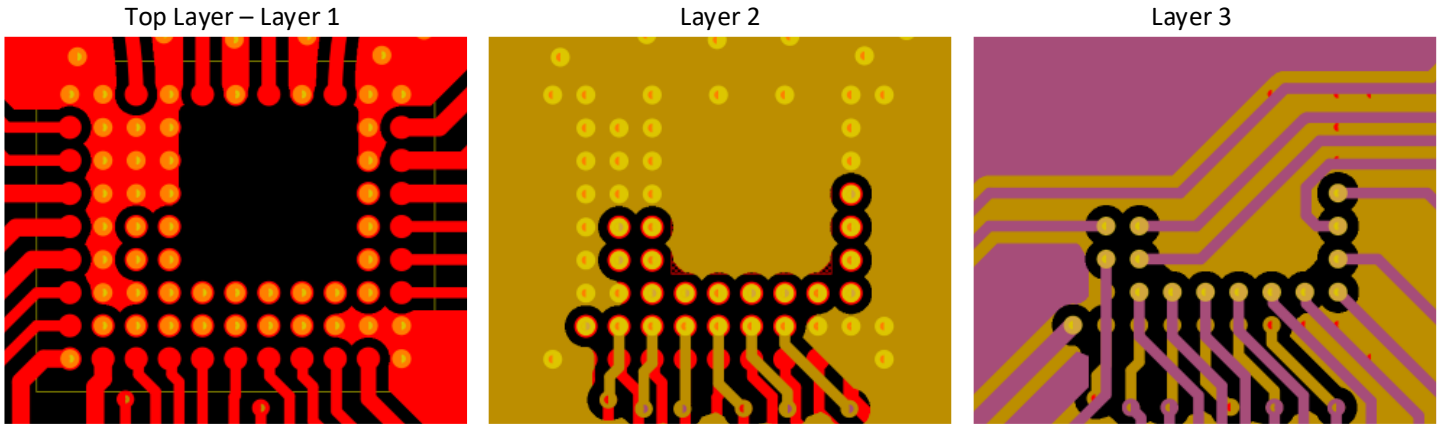


Figure 17: QM3582x - BGA Escape Routing

3.6 RF Transmission Lines

- RF track impedance must be matched to 50 ohms single ended.
- Keep RF tracks as short as possible to minimize insertion loss.
- Keep the RF track as straight as possible as bends can introduce impedance discontinuities.
- If a bend must be used, avoid angles and make the bend radius as large as possible (see screenshot below).
- Never split the ground plane beneath RF tracks
- Remove solder mask above RF tracks.
- Place vias joining ground planes on adjacent layers around the border of transmission lines to shield the RF signal. This technique is sometimes called ‘via shielding’ or ‘via fencing’. The distance between adjacent vias should be small relative to the wavelength (λ) of the highest frequency signal on the RF trace. The recommended distance is λ/20.

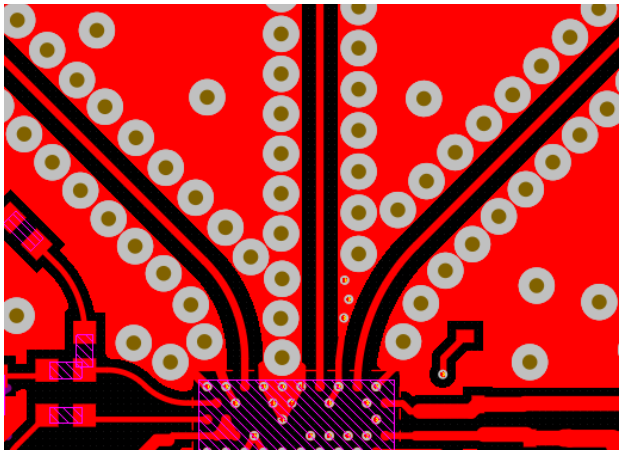


Figure 18: Via Fencing

3.7 High Speed SPI Interface

The QM3572x provides two Hi Speed SPI peripheral. Particular attention should be paid to the routing of these digital signals.

- Keep all SPI layout traces as short as possible.
- Run the trace as straight as possible and avoid using serpentine routing
- Select materials to aid signal integrity. For high-speed design, your material selection is important as the dielectric constant will impact impedances and signal propagation.
- Run the clock signal at least 3x of the trace width away from all other signal traces. This helps to keep clock signal clean from noise (see the figure below).
- Keep a continuous ground in the next layer as reference plane.
- It should be avoided to route the traces with 90° angle corner. The recommendation is to cut the corner and smooth the trace when trace route needs to change direction (see the figure below).

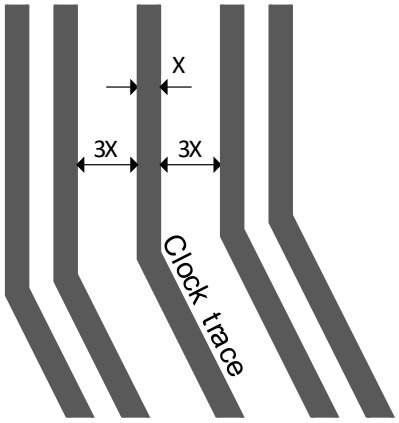


Figure 19: Clock Trace Routing

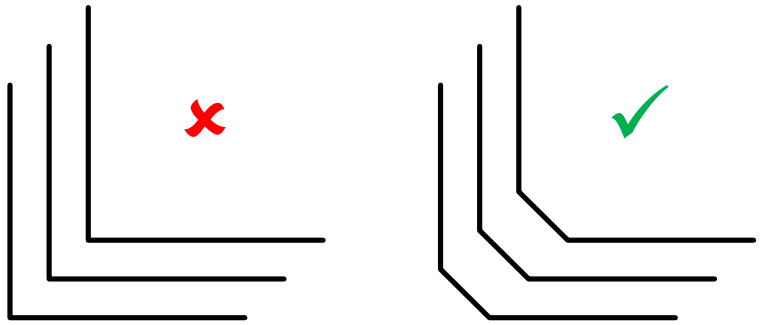


Figure 20: Avoid 90 Degree Trace Angles

4 Power Management

4.1 Power Rails

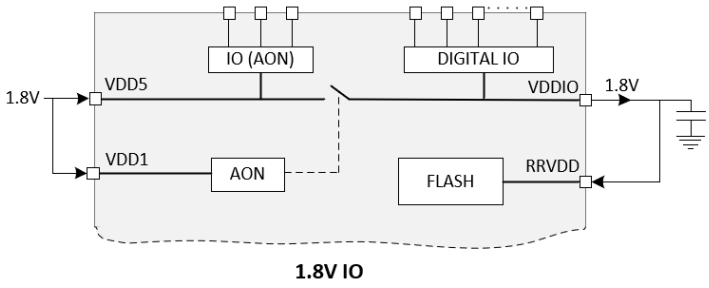
Parameter	Min – Max (V)	Suggested Voltage (V)	Notes
VDD1	1.62 – 1.98	1.8	AON (Always On)
VDD2 **VDD2a**	2.4 – 3.6	2.5	
VDD3 **VDD3a**	1.5 – 3.6	1.8	
VDD4	1.62 – 1.98	1.8	RF Front End power supply
VDD5	1.14 – 1.26	1.2	1.8V / 1.2V based on the application IO voltage
	1.62 – 1.98	1.8	

Table 5: QM3582x Power Supply Rails

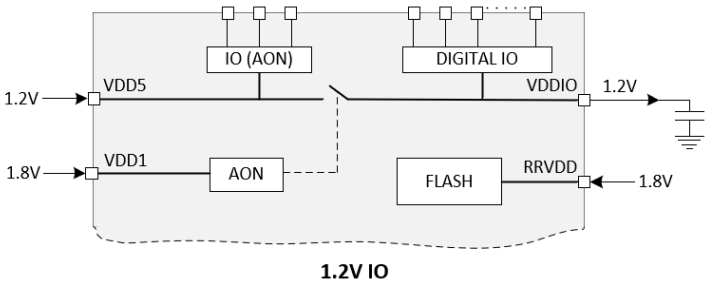
- VDDIO is an internal power rail for GPIOs that is powered by VDD1. So, VDD1 voltage value must be chosen in accordance with host and peripherals interface power rail voltage.

  VDDIO output pin requires a 100nF decoupling capacitor.

  VDDIO rail is not intended to power some other components of the design except external GPIO pull-ups or ultra-low current consumption components such a logic gate.



1.8V IO



1.2V IO

- RRVDD input pin shall be connected to:
  - VDDIO in 1.8V IO config
  - 1.8V power rail in 1.2V IO config
- VDD2TX output pin requires a 220nF decoupling capacitor.

4.2 Placement of components

- It's important to follow DCDC manufacturer's layout guidelines carefully, for control of EMI, and to avoid placing DCDC converters close to sensitive RF circuitry, such as crystals and RF traces.
- Decoupling capacitors should be placed as close as possible to the power pin, with lower value capacitors closer than higher ones.
- The width of power tracks should be as wide as possible to decrease the effective series resistance (ESR) of the track.

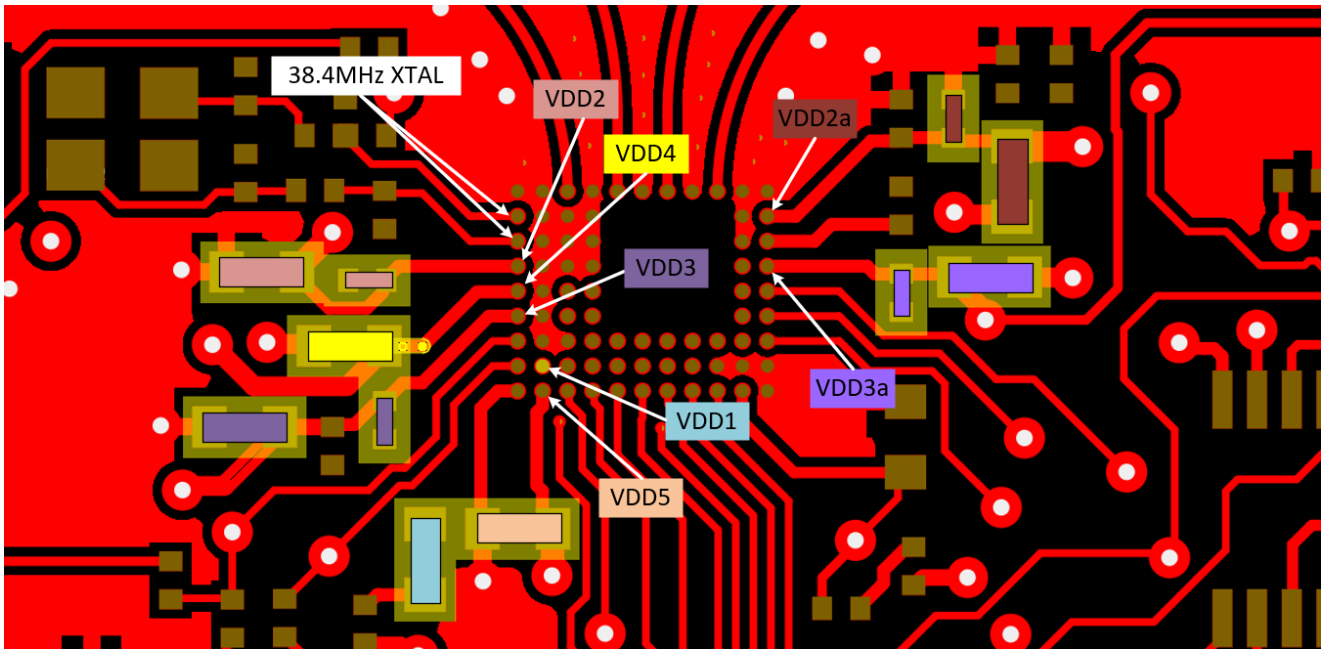


Figure 21: QM3582x - Power Pins and Decoupling Capacitors

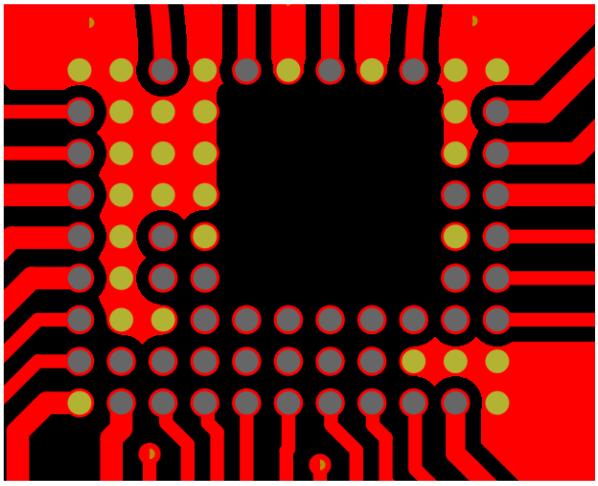


Figure 22: QM3582x Ground Pins

4.3 ACT88329 Power Solution

Qorvo recommends the ACT88329 Power Management Integrated Circuit (PMIC) for all QM3852x power applications.

The ACT88329 PMIC is a power management integrated circuit designed to support a wide range of applications. Its high flexibility, programmability and reconfigurability via the I2C interface allow for seamless adaptation to multiple applications without requiring PCB modifications make it an ideal QM3582x power solution.

The ACT88329 contains three integrated buck converters and two LDOs. It is highly configurable to allow optimization of output voltages, sequencing, GPIO configuration, switching frequency, and low power modes. It operates from standard 3.3V and 5V input voltages. The scalability and configurability feature significantly reduces time to market. The ACT88329 PMIC provides the following benefits when powering the QM3582x UWB:

- Single chip power solution.
- High integration results in an extremely small PCB footprint and low BOM count.
- Low noise outputs result in high system receiver sensitivity and low package error rate.
- Configurability allows easy output voltage changes to optimize system level power

Refer to Qorvo ACT88329 Web Page for additional information including:

- Datasheet with startup sequencing, GPIO configurations, etc.
- EVK User's Guide
- GUI
- Register Map Definition App Note
- Altium PCB schematic, footprint and layout

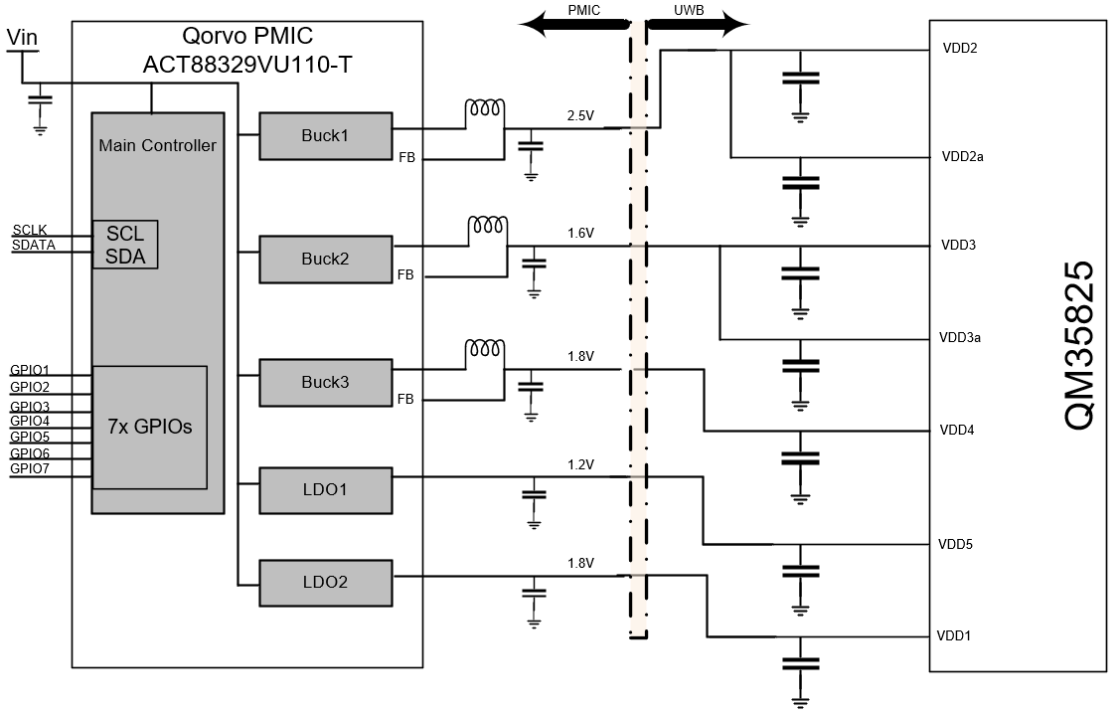


Figure 23: ACT88329VU110 PMIC + QM3582x Block Diagram (1.2V IO configuration)

4.4 ACT88329 Power Rail Default Configuration Details

The ACT88329 default configuration was optimized to support the QM3582x requirements. The ACT88329 output voltage mapping was chosen to meet the following QM3582x requirements.

- VDD1 and VDD5 should be powered by low Iq LDOs if the system uses the QM3582x low power modes.
- VDD2, VDD3, and VDD4 should be powered with low noise DC/DC converters with good load transient performance.
- Ferrite beads such as BLM15AG601SN1D can be used as power rail filters as an option if required.
- Additional filtering for the VDD2a and VDD3a power rails is optional some case Ferrite beads such as BLM15AG601SN1D can be used as power rail filters if required.

The orderable part number for the customized power design is **ACT88329VU110-T**. The table below shows how the ACT88329 output rails are mapped to the QM3582x voltage requirements.

QM3582x Power Rails	QM3582x Voltage Requirement (V)	ACT88329 Voltage Rail	ACT88329 Output Voltage (V)	QM3582x Input Current (mA)	ACT88329 Current Limit (A)	Fsw (kHz)	On/Off Control (Note 1)
VDD1	1.62 - 1.98	LDO2	1.8	1	0.4	-	GPIO1
VDD5	1.2 +/- 5%	LDO1	1.2	1	0.4	-	GPIO2
	1.8 +/- 5%	LDO2	1.8	1	0.4	-	GPIO1
VDD2	2.40 - 3.60	Buck1	2.5	110	3.8	2250	GPIO3
VDD2a							
VDD3	1.50 - 3.60	Buck2	1.6	225	3.8	2500	GPIO4
VDD3a							
VDD4	1.80 +/-10%	Buck3	1.8	225	2	2500	GPIO6

Table 6: ACT88329VU110 to QM3582x Power Rail Mapping

Note 1: The GPIOs specified in the table above are configured as active high inputs to enable/disable each ACT88329 output voltage.

4.5 ACT88329 Detailed Design

Output Voltages: the **ACT88329VU110-T** default settings are configured to meet the QM3582x voltage requirements. Each output voltage rail is set to the required voltage at startup with the IC's internal register settings. The default output voltages are factory programmed but can easily be modified up or down via I2C to optimize the QM3582x transmit power or low power modes. Note that any voltage changes via I2C are volatile, and the IC restarts at the default voltage settings when input power is cycled.

Startup Sequencing: the QM3582x controls the ACT88329 output voltage startup sequencing by pulling the ACT88329 GPIO inputs high. This gives the system full control over startup sequencing. It also allows each rail to be turned on and off independently to minimize power consumption in low power modes. Table 2 Shows how each GPIO is mapped to each output.

I2C Address: the ACT88329 output voltages and configuration settings can be modified via I2C. See the ACT88329 datasheet for more details. The ACT88329VU110 7-bit I2C address is 0x25h. This results in 0x4Ah for a write address and 0x4Bh for a read address.

System Voltage: the ACT88329VU110 is configured for a standard 5V input. The QM3582x can turn on the output voltages when the input voltage goes above the SYSMON threshold (3.6V). The outputs automatically turn off if the voltage increases above the VIN_OV threshold (5.81V) or decreases below the UVLO threshold (2.6V). Refer to IC datasheet for details about how to change these and other system level voltage thresholds.

GPIO Configuration: the table in previous section shows which GPIOs are configured to enable each output rail. Note that GPIO5 and GPIO7 are unused. GPIO5 is connected to the J2 1x6 pin header and only used when connected to Qorvo's ActiveCiPS Programming Dongle. Refer to the IC datasheet for additional GPIO configuration options.

Component Selection: the components for this hardware design are optimized for size. The capacitor requirements are defined in the ACT88329 datasheet and are realized with 0603 sized capacitors in this reference design. Standard X5R or X7R capacitors are acceptable. The ACT88329 datasheet also includes guidance on inductor selection. This design uses 0.47uH inductors with 3.1A saturation current to accommodate the QM3582x maximum output currents as well as the inductor ripple current. The inductor requirements can be realized with a 0603 size and 64mOhm DCR rating such as the DFE18SANR47. This provides a reasonable tradeoff between efficiency and size. The user can make additional tradeoffs between size and efficiency with smaller or larger inductors as long as the inductor value is unchanged, and the saturation current is higher than 2A

4.6 ACT88329 - PCB Schematic and Layout Considerations

The Qorvo ACT88329 PMIC (Power Management Integrated Circuit) supports Printed Circuit Board (PCB) technology with four or more PCB layers. It is compatible with both standard FR4 or Rogers 3xxx dielectric materials. The PMC layout is insensitive to the dielectric constant. The copper thickness can be 1 oz or 1.4 mil, depending on the application's total current requirements for the Buck Switcher or LDO outputs.

This QM3582x hardware is designed with a 6-layer PCB stack-up. The ACT88329 EVK uses a 4-layer stack-up. Both options result in a very small, compact layout. Figure13 Shows the 6-layer stack-up which is identical to the rest of the PCB Note that proper power supply component placement and routing is critical to ensure proper operation. Qorvo recommends following this hardware design placement and routing. The ACT88329 datasheet gives specific placement and routing guidance, and the EVK provides an additional example.

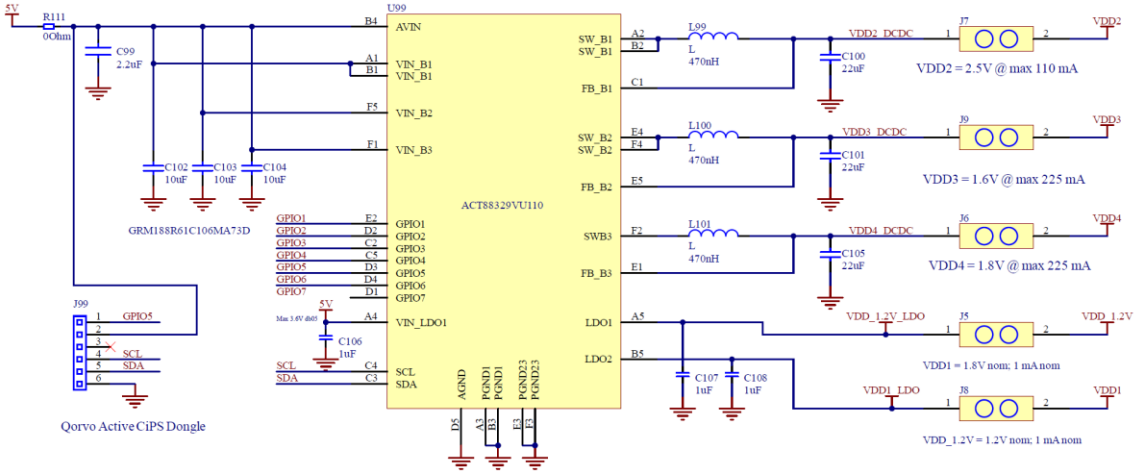


Figure 24: Qorvo's ACT88329 PMIC Detailed Schematic

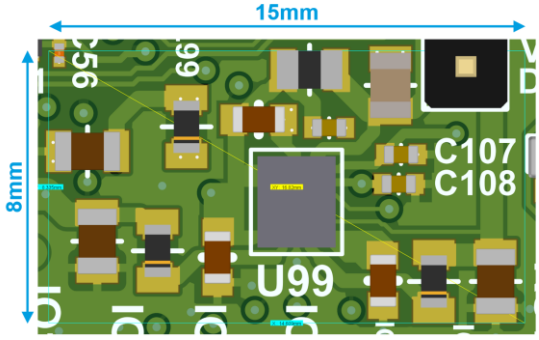


Figure 25: ACT88329 PMIC Component Placement (dimension 15mm x 8mm)

4.7 ACT88329 PMIC PCB detailed layout

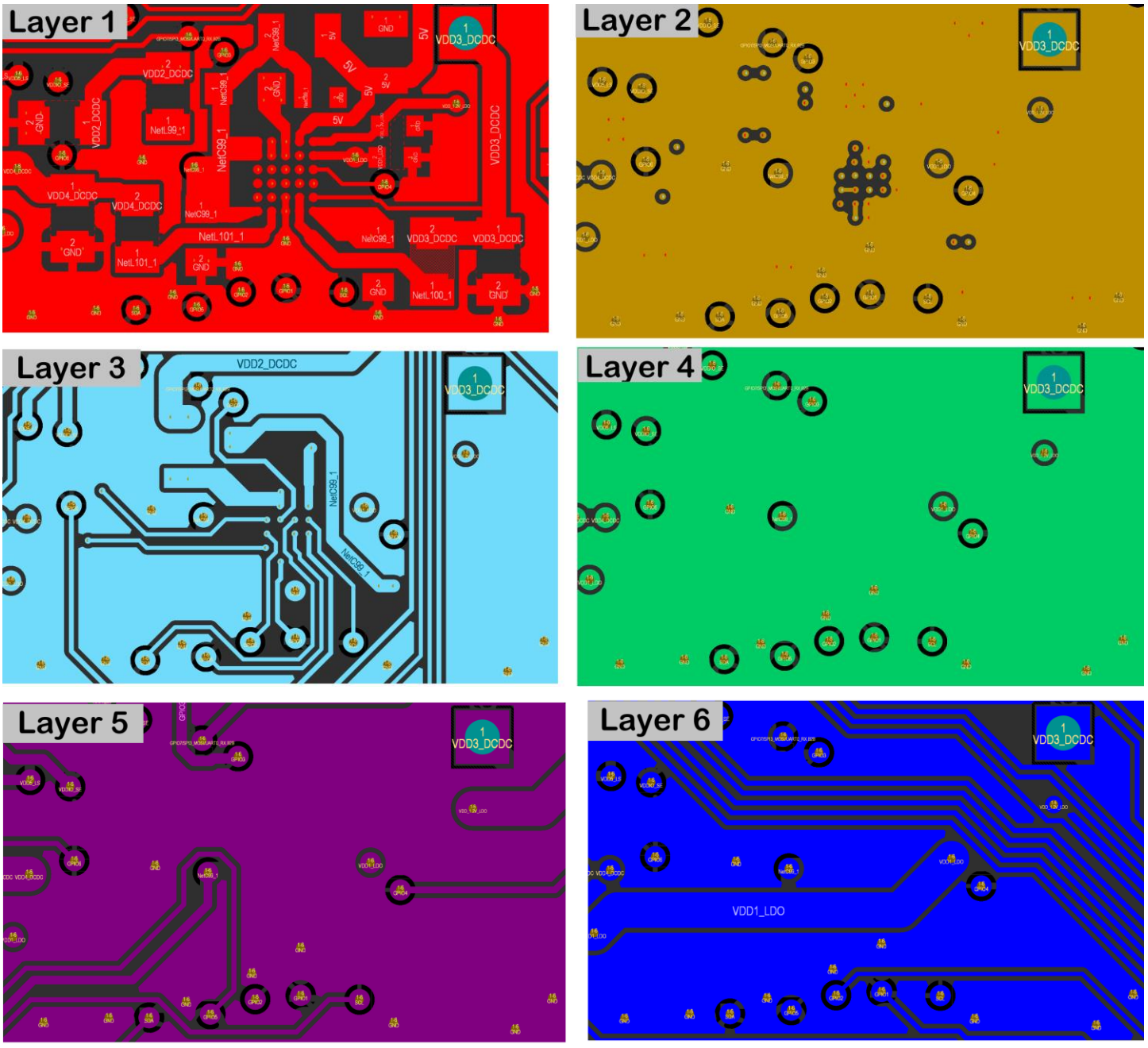


Figure 26: ACT88329 PMIC PCB layout details: Layer 1 to 6

4.8 Alternate Power Scheme

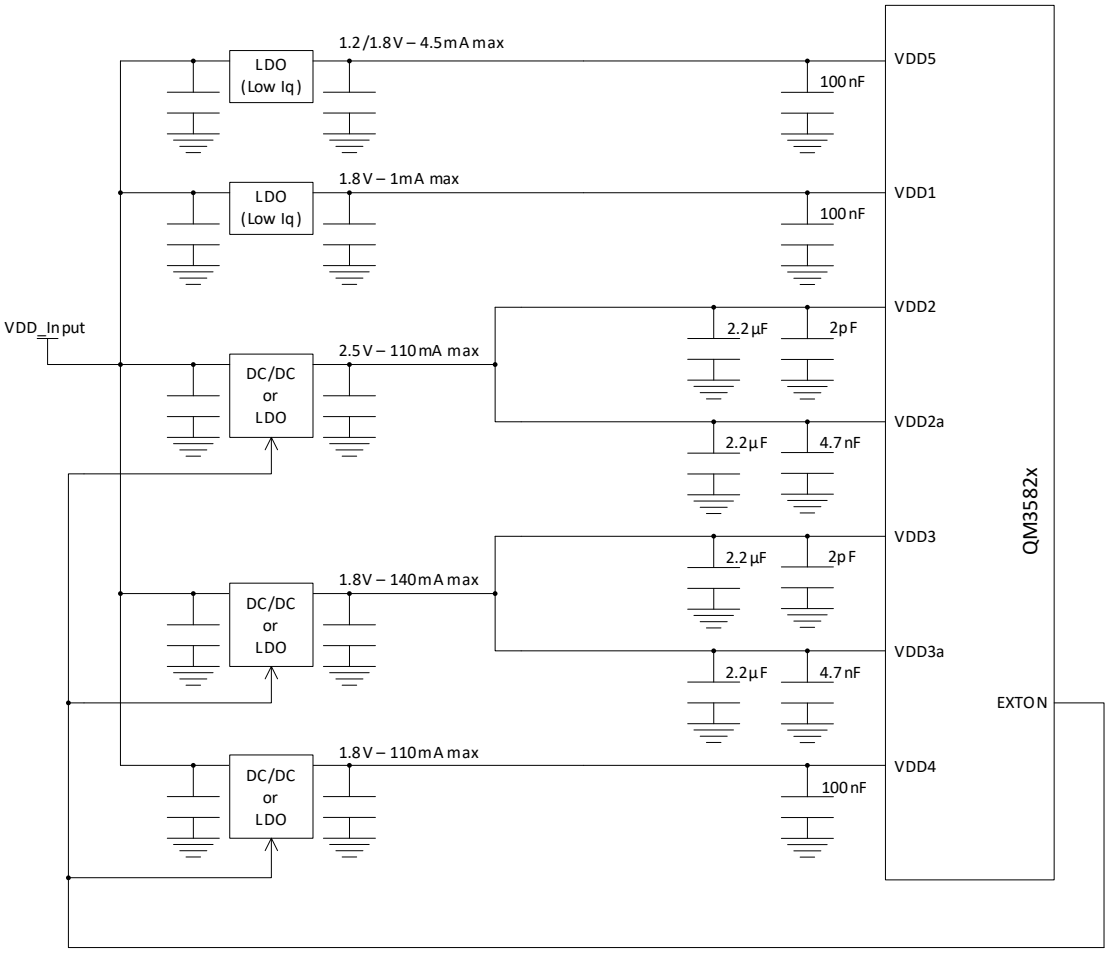


Figure 27: Power Distribution – 1.2V IO Configuration

- It is recommended to select:
  - a low Iq LDO to power VDD1 & VDD5 rail if low power modes are used
  - low noise DC/DC with an excellent transient response to power VDD2, VDD3, & VDD4 rails
- Ferrite beads such as BLM15AG601SN1D can be used as power rail filter
- Filters of VDD2a and VDD3a power rails are highly recommended. The others are optional and depend on the power scheme of the design.

5 Document History

Revision	Date	Description
A	October 2024	Initial version
B	November 2024	Including notes regarding the SS_IRQ and SPI0_PD0 signals
C	February 2025	Update of Application Circuit (modification of RTC crystal reference) Addition of Qorvo PMIC section Addition of information in RTC Oscillator section Addition of a Test Points section

Table 7: Document History

6 Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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7 Important Notice

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