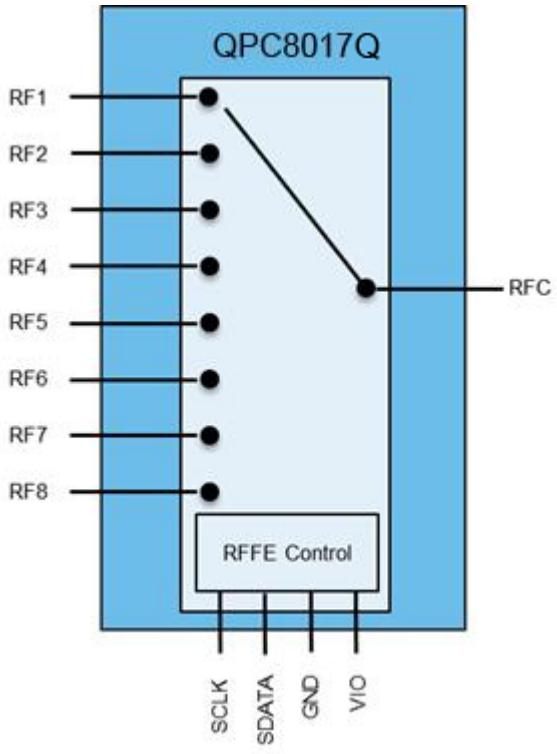
QPC8017Q

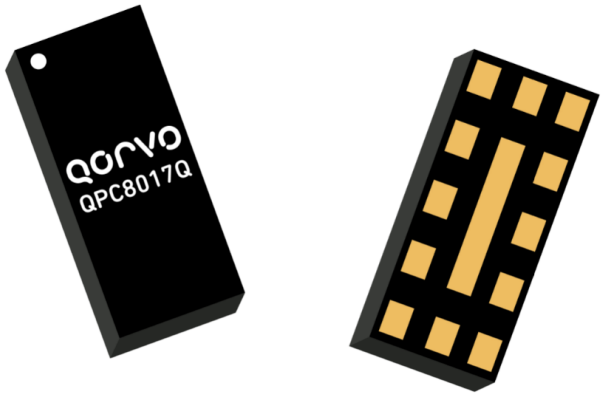
SP8T Switch for LTE Applications

Product Description

The QPC8017Q is a low loss, high isolation SP8T switch with performance optimized for LTE and diversity applications. The QPC8017Q is packaged in an ultra compact 1.1mm x 1.9mm x 0.44mm, 13-pin, Module package which allows for the smallest solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Functional Block Diagram





13 Pin 1.1 x 1.9 x 0.44 mm Module Package

Feature Overview

- Qualified to AEC-Q100 Grade 3
- Excellent insertion loss and isolation performance
  - 0.4dB Typ IL, Band 5
  - 45dB Typ Isolation, Band 5
- Multi-Band operation from 617 MHz to 6000MHz
- RFFE 2.0 compatible
- DC blocking capacitors are not required in typical applications

Applications

- Automotive Telematics Modules
- LTE and Diversity Applications

Ordering Information

PART NO.	DESCRIPTION
QPC8017QSB	5-pc Sample Bag
QPC8017QSR	100-pc, 7” Reel
QPC8017QTR13	10000-pc, 13” Reel
QPC8017QEVB	EVB
QPC8017QDK	Design Kit

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-45 to +125 °C
V_{IO}	2.5 V
SDATA, SCLK	2.5 V
Maximum Input Power (Electrical point of view)	37 dBm, 1:1 VSWR. 100% Duty Cycle, CW, +85C 34 dBm, 3:1 VSWR, 100% Duty Cycle, CW, +85C
Maximum Input Power (Thermal point of view)	34.5 dBm , 1:1 VSWR. 100% Duty Cycle, CW, +85C, Tj=125C
Maximum Input Power (Thermal point of view)	31.5 dBm , 3:1 VSWR. 100% Duty Cycle, CW, +85C, Tj=125C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	MIN.	TYP.	MAX.	UNITS
Operating Ambient Temperature(1)	-40	+25	+85	˚C
V_{IO} Supply Voltage	1.65	1.8	1.95	V
V_{IO} Supply Current (Active Mode)		26	40	µA
V_{IO} Supply Current (Low Power Mode)		4	6	µA
SDATA, SCLK Logic Low (Input)	0.00	0.00	0.3 x VIO	V
SDATA, SCLK Logic High (Input)	0.7 x VIO	1.8	VIO	V
SDATA Logic Low (Output)	0.00	0.00	0.2 x VIO	V
SDATA Logic High (Output)	0.8 x VIO	1.8	VIO	V
SDATA, SCLK Logic High Current		0.1	5	µA
Turn-On Time			20	µs
Switching Speed		3	5	µs

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

1)Case temperature allows 10˚C max rise over Ambient.

Electrical Specifications[1]

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss					
RFx to RFC	617MHz to 960MHz		0.45	0.6	dB
RFx to RFC	1710MHz to 2170MHz		0.55	0.7	dB
RFx to RFC	2300MHz to 2690MHz		0.65	0.8	dB
RFx to RFC	3300MHz to 4200MHz		0.98		dB
RFx to RFC	4400MHz to 5000MHz		1.0		dB
RFx to RFC*	5100MHz to 6000MHz		1.2		dB
Isolation					
RFx to RFx	See Isolation Matrix				dB
RFx to RFC	See Isolation Matrix				dB
Harmonics					
Low Band, 2fo	Pin = +26dBm, 50Ω, f_o= 824MHz		-75	-70	dBm
Low Band, 3fo	Pin = +26dBm, 50Ω, f_o= 824MHz		-63	-60	dBm
Mid Band, 2fo	Pin = +26dBm, 50Ω, f_o= 1980MHz		-79	-65	dBm
Mid Band, 3fo	Pin = +26dBm, 50Ω, f_o= 1980MHz		-63	-56	dBm
High Band, 2fo	Pin = +26dBm, 50Ω, f_o= 2570MHz		-73	-61	dBm
High Band, 3fo	Pin = +26dBm, 50Ω, f_o= 2570MHz		-66	-62	dBm
IMD2					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 1840 MHz at -15dBm Measured RX frequency @ 942.5MHz		-114		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 3840 MHz at -15dBm Measured RX frequency @ 1960MHz		-115		dBm
IMD3					
Low Band	TX Carrier @ 897.5MHz at +21dBm CW Blocker @ 852.5MHz at -15dBm Measured RX frequency @ 942.5MHz		-109		dBm
High Band	TX Carrier @ 1880MHz at +21dBm CW Blocker @ 1800MHz at -15dBm Measured RX frequency @ 1960MHz		-108		dBm
VSWR					
	698 MHz to 960 MHz		1.14		:1
	1700 MHz to 2700 MHz		1.4		:1

* See tuning schematic for 5000MHz to 6000MHz insertion loss
[1] Recommended EVB schematic / layout / BOM / PCB should be followed in order to achieve specified performance.

Isolation Matrix Low Band (617MHz – 960MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		43	39	53	51	47	37	36
RF2	RF2	43		53	39	49	50	37	38
RF3	RF3	38	50		53	42	46	39	37
RF4	RF4	49	38	55		49	40	37	40
RF5	RF5	44	53	37	53		48	41	38
RF6	RF6	53	42	55	36	50		38	40
RF7	RF7	51	54	46	54	36	51		42
RF8	RF8	54	49	55	44	52	35	42	
RF1	RFC		50	44	50	44	41	34	34
RF2	RFC	49		52	44	42	44	34	35
RF3	RFC	44	53		47	49	41	36	34
RF4	RFC	55	42	50		42	48	34	36
RF5	RFC	50	49	41	47		41	43	35
RF6	RFC	51	47	49	40	42		35	43
RF7	RFC	51	49	52	48	42	43		38
RF8	RFC	51	52	50	49	45	41	38	

Isolation Matrix Mid Band (1710MHz – 2170MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		33	30	39	37	38	30	30
RF2	RF2	33		39	29	39	36	30	31
RF3	RF3	29	37		40	31	37	31	30
RF4	RF4	37	28	40		38	30	30	32
RF5	RF5	34	39	29	40		37	34	31
RF6	RF6	39	33	41	28	38		31	28
RF7	RF7	39	40	36	40	27	37		33
RF8	RF8	40	37	41	34	38	26	33	
RF1	RFC		40	36	38	34	32	26	26
RF2	RFC	39		40	36	33	34	26	26
RF3	RFC	35	40		37	36	32	26	26
RF4	RFC	41	34	39		33	34	26	27
RF5	RFC	37	38	34	37		32	29	26
RF6	RFC	39	36	38	32	33		27	29
RF7	RFC	37	38	38	38	32	34		28
RF8	RFC	39	37	39	37	34	31	28	

Isolation Matrix High Band (2300MHz – 2690MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		30	27	35	34	34	28	28
RF2	RF2	30		35	26	35	32	28	28
RF3	RF3	26	34		36	27	34	29	28
RF4	RF4	33	25	36		35	26	28	29
RF5	RF5	30	35	25	36		34	33	29
RF6	RF6	35	29	37	25	35		29	24
RF7	RF7	35	35	32	36	24	33		29
RF8	RF8	36	34	36	31	34	23	30	
RF1	RFC		37	34	35	31	29	23	23
RF2	RFC	37		36	34	30	30	23	23
RF3	RFC	33	37		34	32	29	23	23
RF4	RFC	37	32	35		30	30	23	24
RF5	RFC	33	35	31	34		29	25	24
RF6	RFC	35	33	35	30	30		24	25
RF7	RFC	33	34	34	34	29	30		25
RF8	RFC	35	33	35	33	31	28	25	

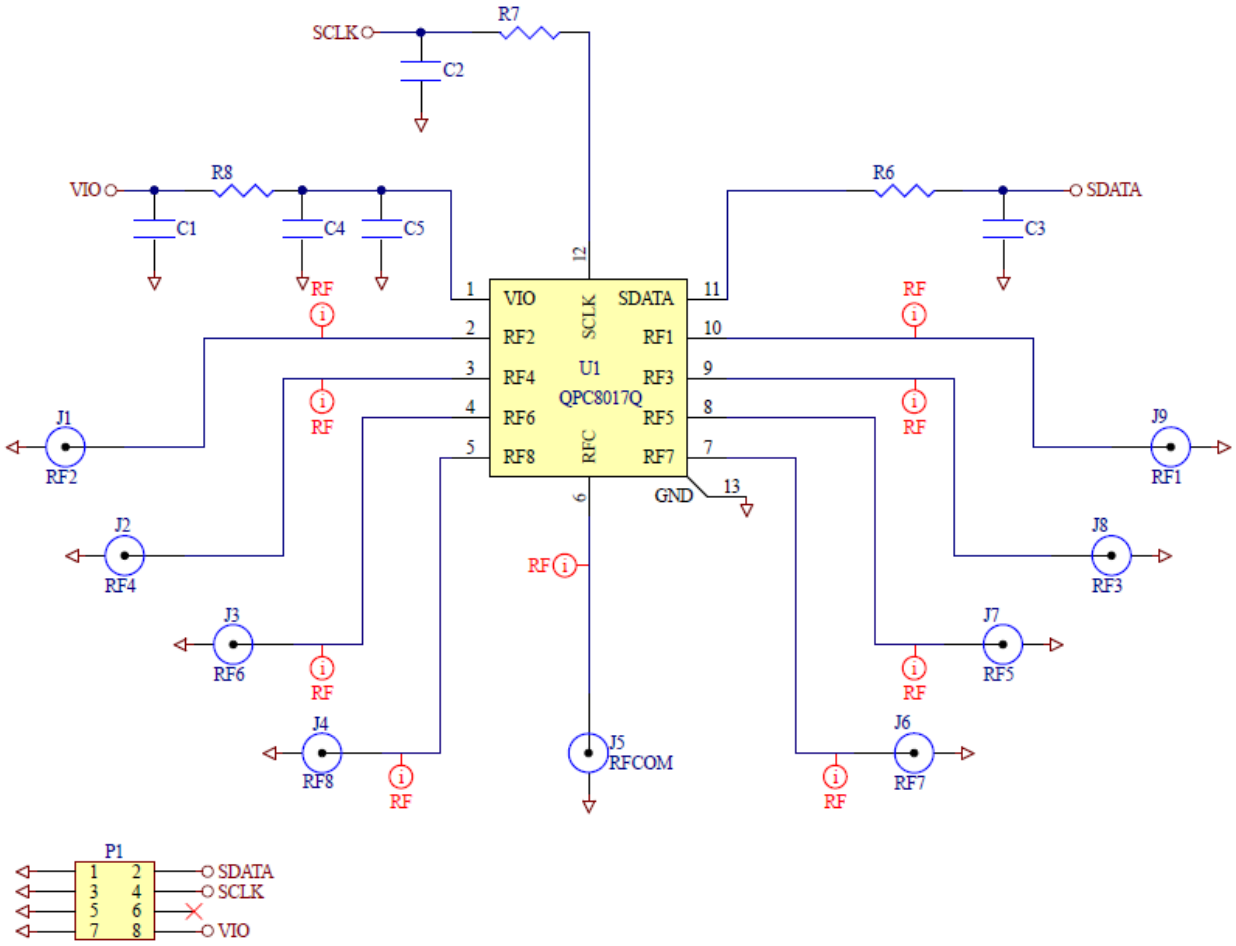
Isolation Matrix Ultra High Band (3200MHz – 3800MHz)

STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		25	22	30	28	30	26	25
RF2	RF2	25		30	22	31	27	26	26
RF3	RF3	21	28		31	22	30	26	26
RF4	RF4	28	21	31		31	21	26	25
RF5	RF5	26	30	21	32		30	30	26
RF6	RF6	30	25	32	20	30		26	19
RF7	RF7	30	30	27	31	19	28		25
RF8	RF8	30	29	31	26	29	19	25	
RF1	RFC		33	31	30	26	25	20	19
RF2	RFC	33		31	31	26	26	20	19
RF3	RFC	28	32		30	26	25	19	19
RF4	RFC	32	28	31		26	26	20	19
RF5	RFC	28	30	28	29		25	20	20
RF6	RFC	31	28	30	27	26		20	20
RF7	RFC	28	30	29	29	25	25		20
RF8	RFC	30	28	30	28	26	24	21	

Isolation Matrix LTE-U Band (5000MHz – 6000MHz)

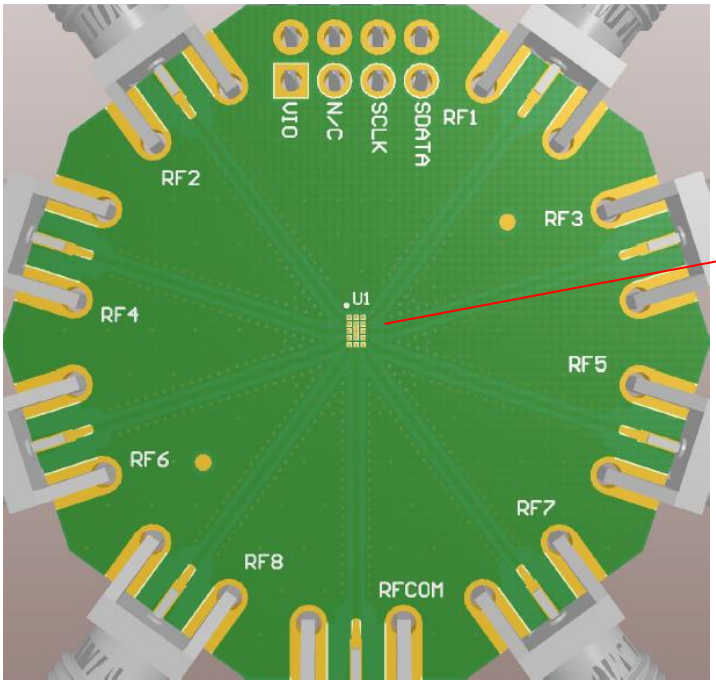
STATE	INSERTION PORT	ISOLATION, TYPICAL (dB)							
		RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
RF1	RF1		20	18	25	23	26	23	24
RF2	RF2	20		26	17	26	22	23	23
RF3	RF3	17	24		27	18	26	22	23
RF4	RF4	23	16	27		26	17	23	21
RF5	RF5	21	25	17	27		25	29	23
RF6	RF6	25	20	27	16	25		23	14
RF7	RF7	25	25	22	25	14	23		20
RF8	RF8	25	23	26	21	23	14	20	
RF1	RFC		27	27	25	21	21	15	15
RF2	RFC	28		27	27	21	21	15	15
RF3	RFC	24	27		25	21	21	15	15
RF4	RFC	28	24	27		22	20	15	15
RF5	RFC	24	26	25	25		21	14	15
RF6	RFC	26	23	26	24	22		15	14
RF7	RFC	23	25	24	25	19	21		15
RF8	RFC	25	22	26	23	21	18	15	

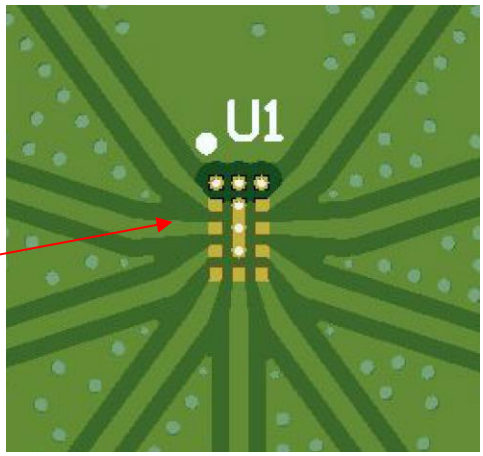
Application Circuit Schematic & BOM



Ref Des	Qty	UOM	Material #	Alt Grp	Usage Prob %	Description	Manufacturer	Manufacturer Part #
PCB	1	EA	291882			PCB, QPC8017Q	TTM TECHNOLOGIES INC	QPC8017Q-4000
C4	1	EA	273180			CAP, 100pF, 5%, 25V, C0G, 0201	MURATA ELECTRONICS SINGAPORE PTE LT	GRM0335C1E101JA01D
R6,R7,R8	3	EA	21253			RES, 0 OHM, 5%, 1/20W, 0201	Kamaya, Inc	RMC1/20JPPA15
U1	1	EA	QPC8017QSR			SP8T Switch, LTE, RFFE		
RF1,RF2,RF3,RF4, RF5,RF6,RF7,RF8, RFCOM	9	EA	262452			CONN, SMA, EL MINI FLT 0.068" SPE-000303	Aliner Industries, Inc.	20-001CF-T
P1	1	EA	272100			CONN, HDR, SHRD, RT-AN, 2x4, 0.100", T/H	MOLEX	90130-3108
C1,C2,C3,C5	5	EA	4XXX1			NOT POPULATED ITEM-1		DUMMY PART

Evaluation Board





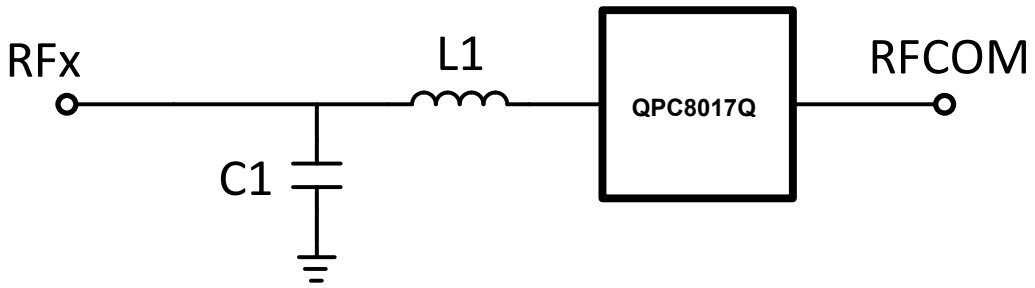
3 Vias under DUT for thermal transfer

Evaluation Board PCB Information

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	0.70mil		
4	Dielectric1	Rogers 4003	8.00mil	3.55	
5	Signal Layer 1	Copper	0.70mil		
6	Dielectric 3	FR4	8.00mil	4.2	
7	Signal Layer 2	Copper	0.70mil		
8	Dielectric 4	FR4	24.00mil	4.2	
9	Signal Layer 3	Copper	0.70mil		
10	Dielectric 5	FR4	8.00mil	4.2	
11	Signal Layer 4	Copper	0.70mil		
12	Dielectric 2	FR4	8.00mil	4.2	
13	Bottom Layer	Copper	1.40mil		
14	Bottom Solder	Solder Resist	0.40mil	3.5	
15	Bottom Overlay				

Total Thickness: 62mil +/- 10%

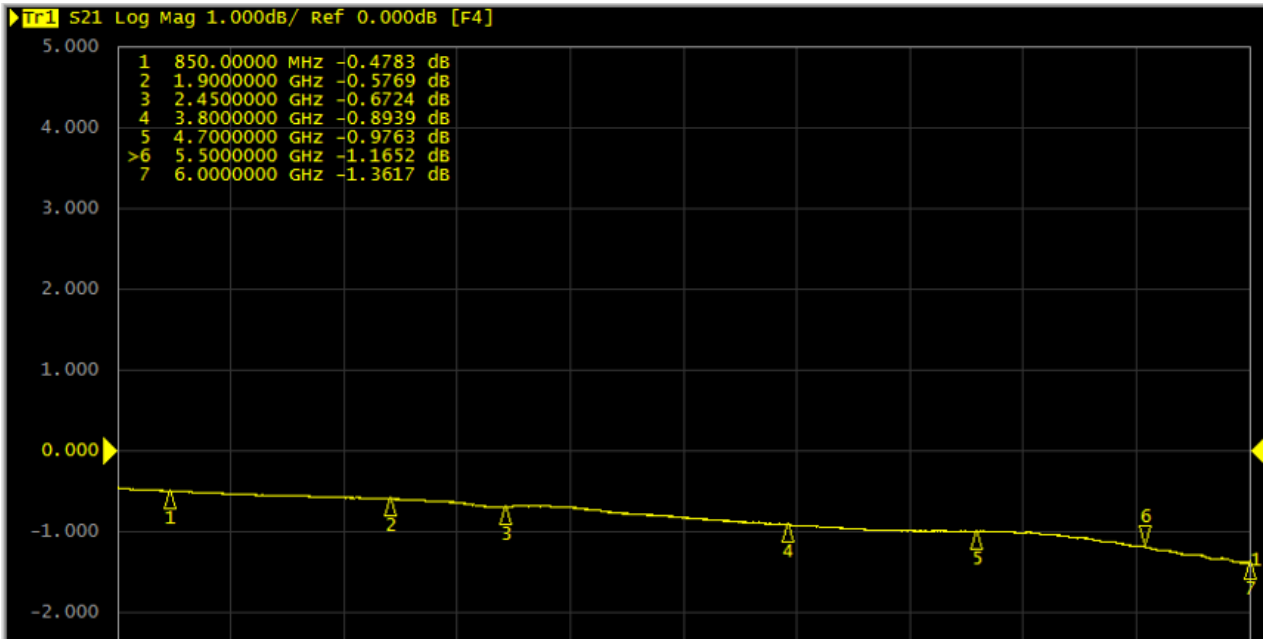
Tuning Schematic for 5000MHz – 6000MHz



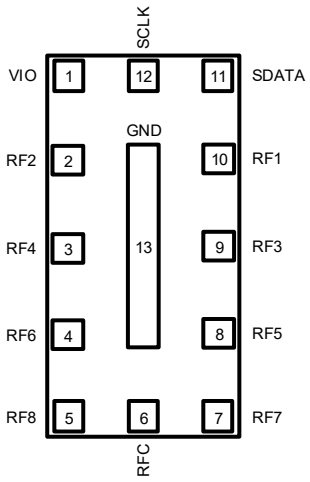
NAME	VALUE	PACKAGE	DESCRIPTION
C1	0.4pF	0201	Matching for optimized RF performance*
L1	1.1nH	0201	Matching for optimized RF performance*

* Matching Elements are subject to change based on specific system application

Note: For High Frequency application, 10pF caps placed on control signals and VIO close to device pins can improve insertion loss



Pin Configuration and Description



Top View

PIN NO.	LABEL	DESCRIPTION
1	VIO	Voltage Supply
2	RF2	RF Port
3	RF4	RF Port
4	RF6	RF Port
5	RF8	RF Port
6	RFC	RF Common Port
7	RF7	RF Port
8	RF5	RF Port
9	RF3	RF Port
10	RF1	RF Port
11	SDATA	RFFE Data Signal
12	SCLK	RFFE Data Signal
13	GND	Ground

RFFE Register Map

Register 0x0000 — SW_CTRL0

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	0 - 2	R/W
6:0	SW_CTRL	0x00: Isolation 0x01: RF1 - RFC 0x02: RF2 - RFC 0x04: RF3 - RFC 0x08: RF4 - RFC 0x10: RF5 - RFC 0x20: RF6 - RFC 0x40: RF7 - RFC 0x41: RF8 - RFC	0x00	No	0 - 2	R/W

Register 0x0001 — SPARE

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	SPARE	Reserved for future use	0x00	No	0 - 2	R/W

Register 0x001A — RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B — GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C — PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	PWR_MODE[1:0]	00: ACTIVE - Normal Operation 01: STARTUP - Reset all registers to default settings 10: ACTIVE - Low Power - Antenna in isolation 11: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0b10	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D — PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x19	No	No	R

Register 0x001E — MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x34	No	No	R

Register 0x001F — MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	RESERVED	Reserved for future use	0b00	No	No	R
5:4	MFG_ID[9:8]	Upper two bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0b01	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x9	No	No	R/W

Register 0x0020 — EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Register 0x0021 — REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Register 0x0022 — GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 – ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x002C – TEST_PATT

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see figure 1)

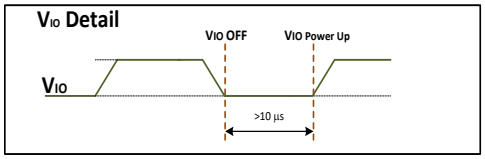


Figure 1 Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see figure 2)
3. VIO must be applied for a minimum of 15 µs before applying RF power. (see figure 2)
4. Wait a minimum of 5 µs after RFFE bus is idle to apply an RF signal. (see figure 2)

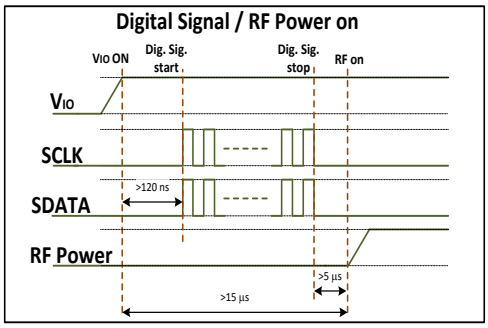


Figure 2 Digital Signal/RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see figure 3)

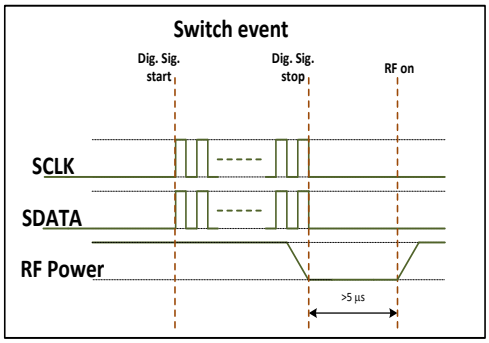


Figure 3 Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 µs before exiting “Low Power Mode”. (see figure 4)

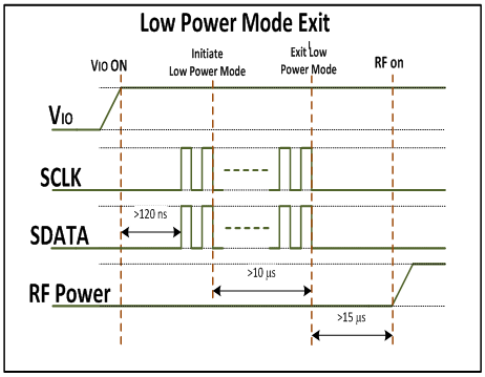
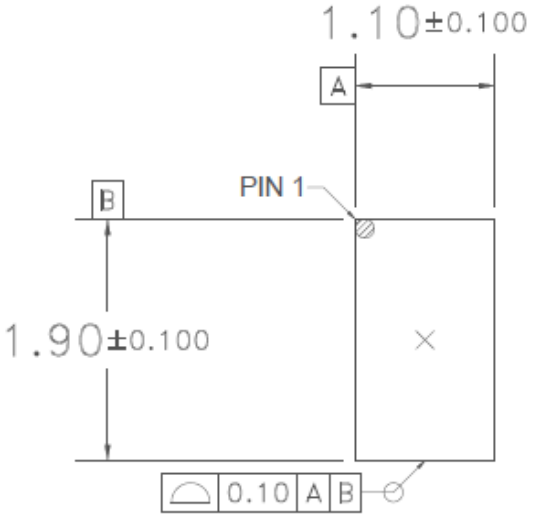


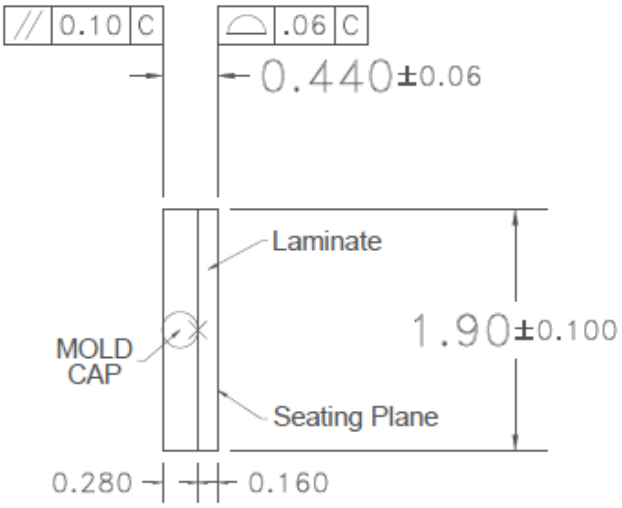
Figure 4 Low Power Mode Exit Timing

Mechanical Information

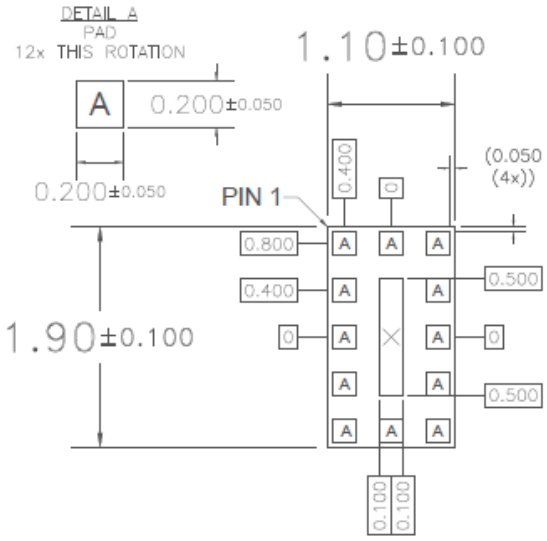
Package Drawing

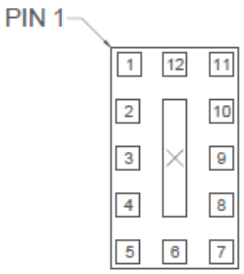


Top View



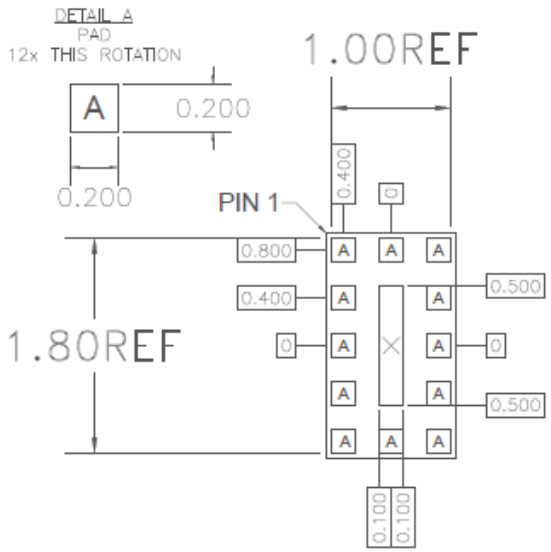
Side View



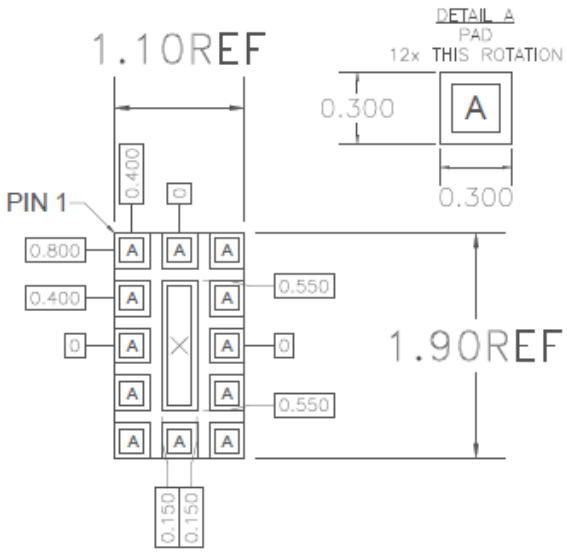


Top View X-Ray

PCB Design Requirements



Recommended Land Pattern



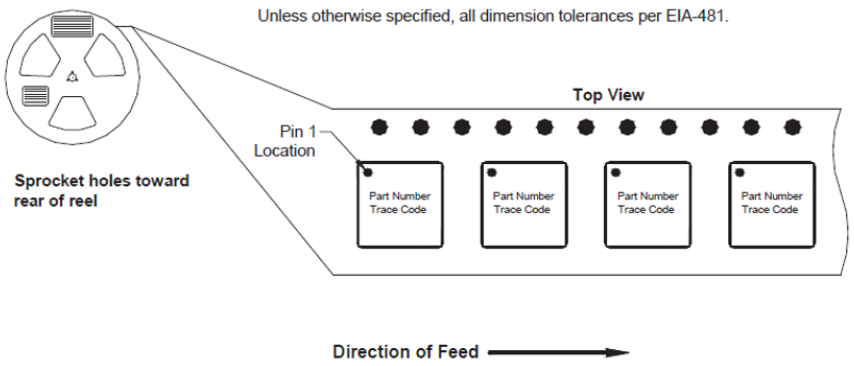
Recommended Land Pattern Mask

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Tape and Reel Information

Table 1. Tape and Reel

Qorvo Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units Per Reel
QPC8017QTR13	13 (330)	4 (102)	8	4	Single	10000
QPC8017QSR	7 (178)	2.5 (63)	8	4	Single	100



1.10 mm x 1.90 mm (Carrier Tape Drawing with Part Orientation).

Handling Precautions

PARAMETER	RATING	STANDARD
ESD – Human Body Model (HBM)	Class 2 2000V	ESDA/JEDEC JS-001-2012
ESD – Charge Device Model (CDM)	Class C3 1000V	ESDA/JEDEC JS-002-2012
MSL – Moisture Sensitivity Level	MSL3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: ENEPIG

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free
- PFOS Free

Revision History

Revision Code	Date	Comments
Rev 1.0	October 19, 2018	Initial Datasheet Release
Rev 1.1	8/6/19	Update 380 min/max limits and automotive requirements
Rev 1.2	10/9/19	Updated image and added 2.7GHz GBD
	4/28/20	Updated page 1 freq range
A	11/16/20	Updated format
B	2/17/22	Updated for production release; Replaced TBDs with production run data. Added vias shot under DUT on EVB. Updated EVB schematic and BOM; Added matched EVB Trace Data Shot with Note; Added ESD ratings
C	8/14/25	Updated page1 EVB orderable part, modified part number of TR13 on page17

Contact Information

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