APPLICATION NOTE

QPF4259

Wi-Fi 7 Front End Module

Product Overview

The purpose of this application note is to help customers translate the layout and design guidelines for the Qorvo® QPF4259 front end module.

The Qorvo® QPF4259 is an integrated front end module (FEM) designed for Wi-Fi 7 (802.11be) systems. The compact form factor and integrated matching minimizes layout area in the application.

Performance is focused on optimizing the PA for a 5V supply voltage that conserves power consumption while maintaining the highest linear output power and leading-edge throughput.

Integrated die level filtering for 2nd and 3rd harmonics as well as 5 GHz rejection for DBDC operation are included. A coupler with RF output as well as a broad range, constant slope voltage logarithmic power detector is provided for application feedback.

The QPF4259 integrates a 2.4 GHz power amplifier (PA), single pole two throw switch (SP2T) and bypassable low noise amplifier (LNA) into a single device.

Product Details

Figure 1a. Device Packaging Detail

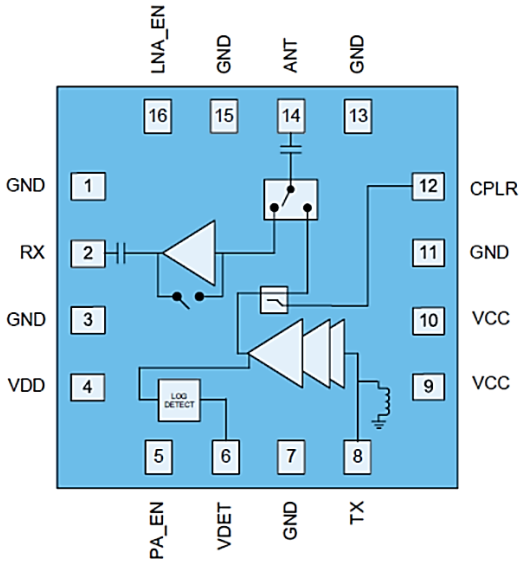


Figure 1b. Functional Block Diagram & Pin-Out Detail

Pin Configuration and Description

Table 1. QPF4259 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1	GND	Ground connection.
2	RX	RF output from the low noise amplifier. Internally matched to 50 Ω and DC blocked. (1)
3	GND	Ground connection.
4	VDD	DC Supply voltage.
5	PA_EN	Control pin.
6	VDET	DC power detector. Provides an output voltage proportional to the RFoutput power level.
7	GND	Not internally connected. Recommend connecting to ground or leave floating.
8	TX	RF input. Internally matched to 50 Ω and DC blocked. (1)
9	VCC	DC Supply voltage.
10	VCC	DC Supply voltage.
11	GND	Ground connection.
12	CPLR	RF power detector. Provides a coupled RF output power proportional to the RF output power level.
13	GND	Ground connection.
14	ANT	RF bi-directional antenna port. Internally matched to 50 Ω and DC blocked. (1)
15	GND	Ground connection.
16	LNA_EN	Control pin.
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Notes:

1. Pin is DC blocked internally. There is no DC present on these ports. If connected to an external component with DC present, Qorvo® recommends using a blocking capacitor.

Evaluation Board Information

The Qorvo® QPF4259 evaluation board is designed to provide performance representative of that obtainable in an actual application. The EVB is designed to operate with 50 Ω load impedances at all RF ports, which are provided with SMA connector interface.

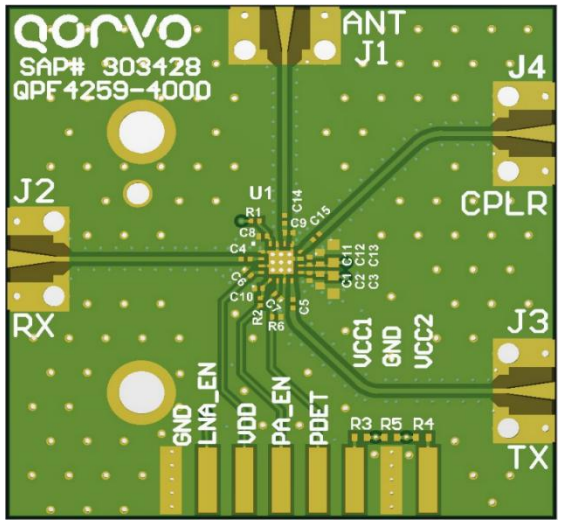


Figure 2a. QPF4259 Evaluation Board PCB

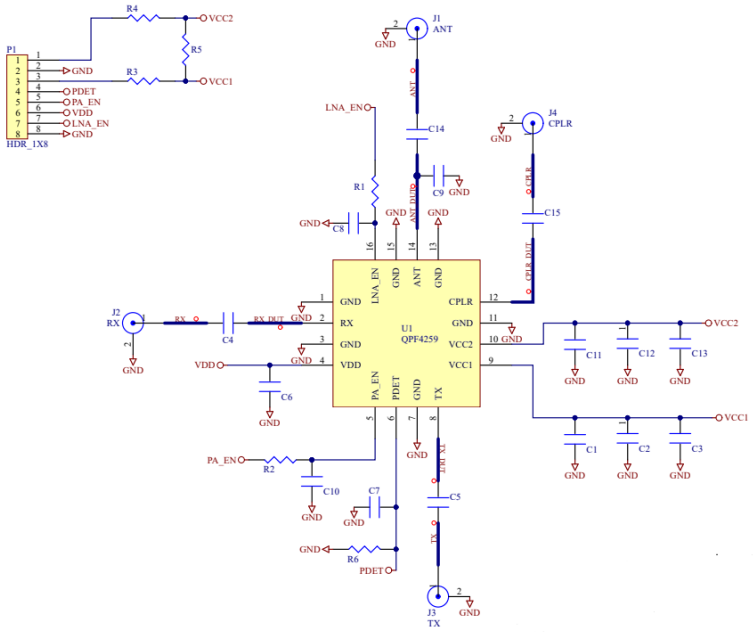


Figure 2b. QPF4259 Evaluation Board Schematic

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3.5	
1	Top Layer	Copper	1.40mil		
	Dielectric1	RO4003	8.00mil	3.55	
2	Mid-Layer 1	Copper	1.40mil		
	Dielectric2	FR-4	10.20mil	4.26	
3	Mid-Layer 2	Copper	1.40mil		
	Dielectric3	FR-4	8.00mil	4.26	
4	Bottom Layer	Copper	1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3.5	
	Bottom Overlay				

Total Thickness: 0.034 +/- 10%

Figure 2c. QPF4259 Evaluation Board PCB Stack-Up

Table 2. QPF4259 Evaluation Board Bill of Materials

REF. DES.	VALUE	DESCRIPTION	MANUF.	PART NUMBER
-	-	Printed Circuit Board	-	-
U1	-	2.4GHz Wi-Fi 7 Front End Module	Qorvo®	QPF4259
C3, 13	4.7 µF	Capacitor, Chip, 20%, 16V, X7R, 0603	Murata	GRM188Z71C475ME21D
C1, C11	1000pF	Capacitor, Chip, 10%, 16V, X7R, 0201	-	-
C6	1 µF	Capacitor, Chip, 0201	-	-
C4, C5, C8, C10, C14, C15	100 pF	Capacitor, Chip, 5%, 25V, C0G, 0201	-	-
C2, C12	1 µF	Capacitor, Chip, 10%, 25V, X6S, 0402	Murata	GRM155C81E105KE11D
R3, R4	0 Ω	Res, Chip, 1/10W, 0402	Kamaya	RMC1/16SJPTH
R1, R2	0 Ω	Res, Chip, 1/20W, 0201	Kamaya	RMC1/20JPPA15
R6	27 kΩ	Res, Chip, 5%, 1/16W, 0201	Kamaya	RMC1/20-273JPA15
C7, C9, R5	-	Not Populated Item	-	-

Logic Truth Table

Table 3. QPF4259 Logic Truth Table

Mode	PA_EN	LNA_EN
Transmit	High	Low
LNA On	Low	High
Bypass	Low	Low
Not Supported	All Other States	

Notes:

1. The QPF4259 logic control and RF input is required to ensure optimal performance and reliable operation. See the turn on/off procedure below.

Transmit Power-On Procedure:

1. Connect Power Supplies in OFF mode (0V) to VCC, VDD, and PA_EN pins.
2. Apply +5V to VCC and VDD pins.
3. Apply control voltages (0V to LNA_EN, +1.8V to PA_EN).
4. Apply RF input signal to J3 (TX, pin 8), transmit RF; measure RF output on J1 (ANT, pin 14).
5. DC Power detector voltage can be monitored on VDET, pin 6.
6. RF Power detector can be monitored on J4 (CPLR, pin 12).

Transmit Power-Off Procedure:

1. Remove RF input signal.
2. Set all control signals (PA_EN, LNA_EN) to 0V.
3. Set the Power Supply Voltages on VCC and VDD to 0V.

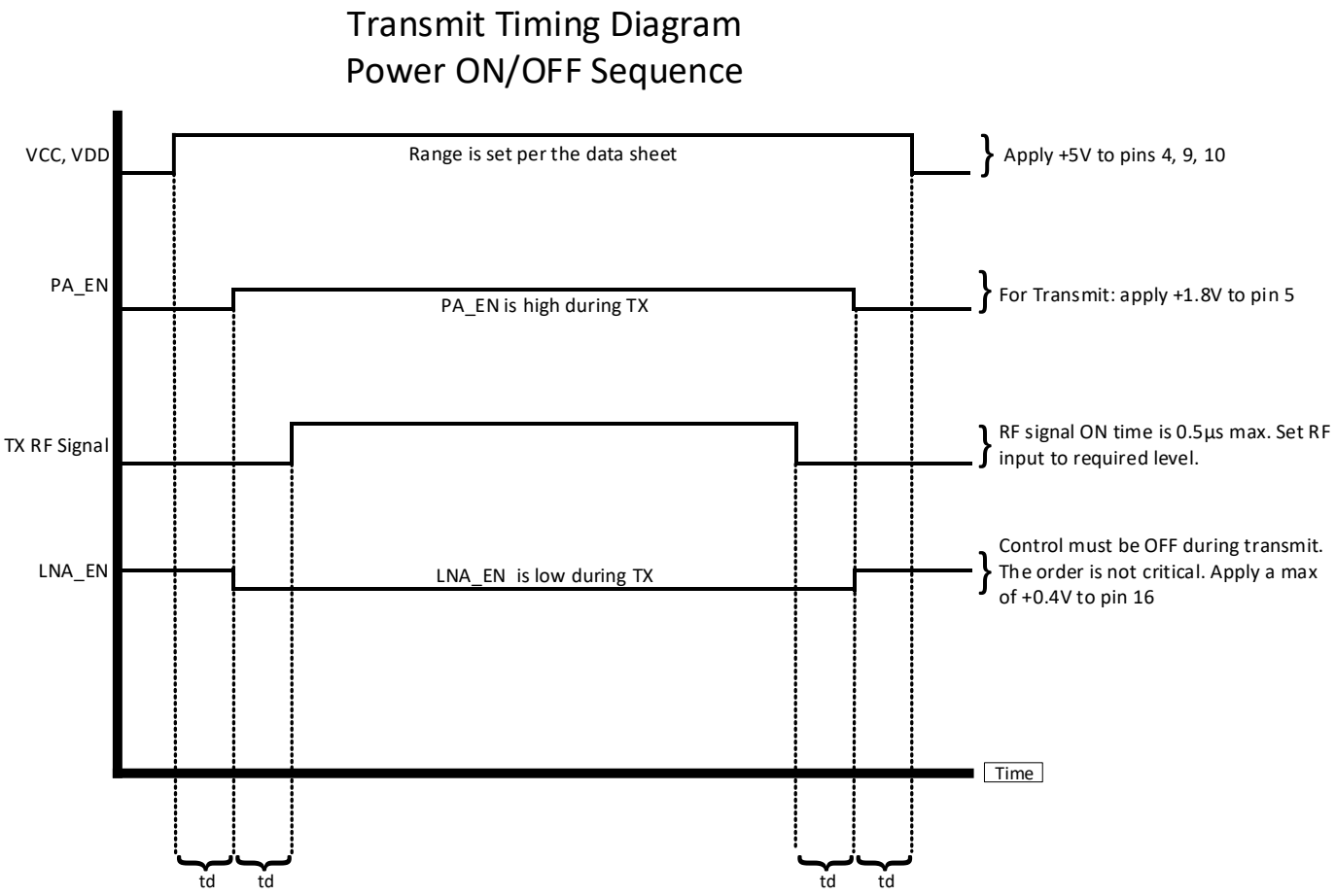


Figure 3a. QPF4259 Transmit Timing Diagram

Notes:

1. RF Signal for each specific mode is applied after the DC bias is applied.
2. For “td” value, please refer to the turn ON/OFF switching time shown in the QPF4259 datasheet specification table.

System Architecture Application Circuit Recommendations

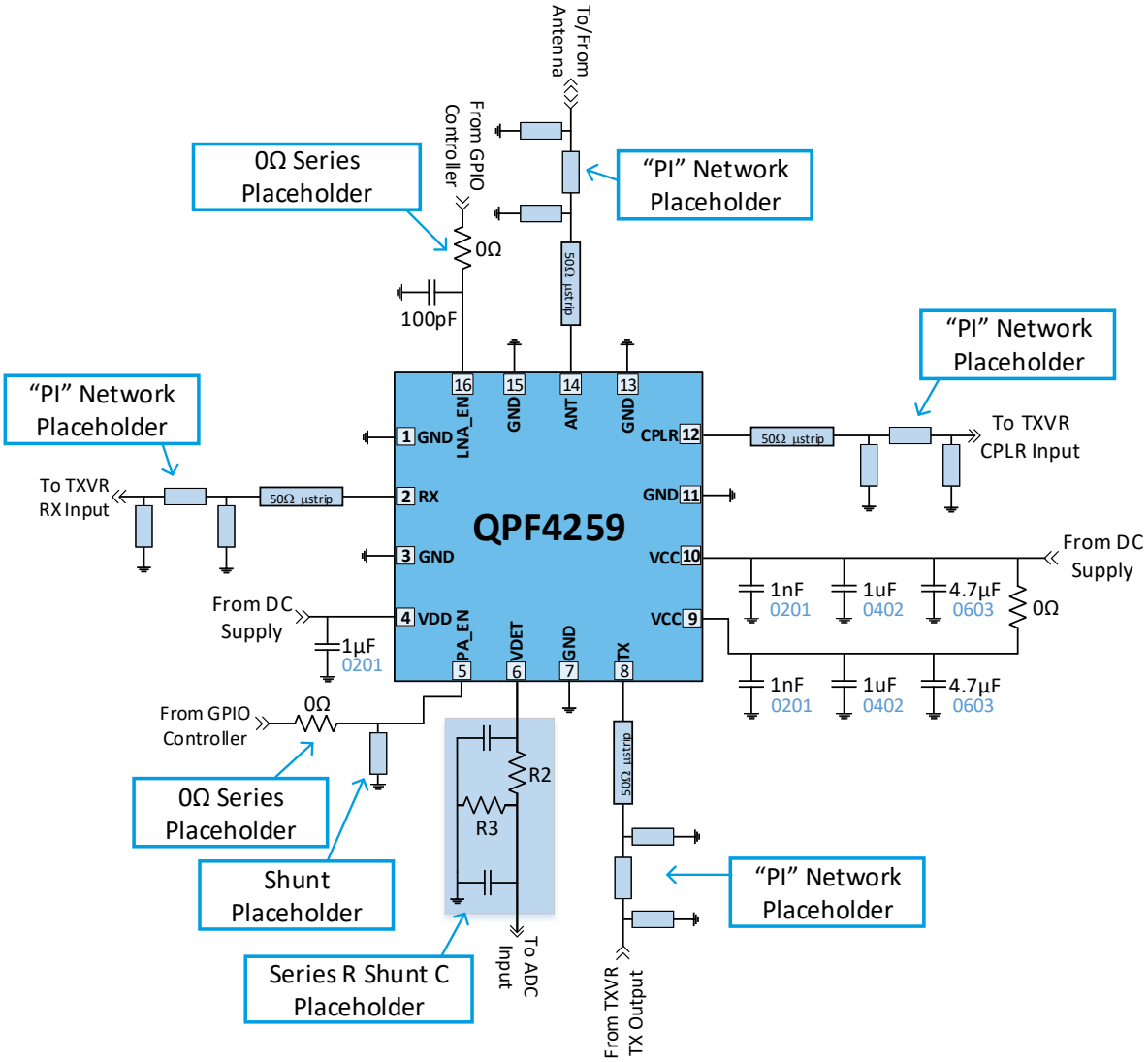


Figure 4a. Recommended Application Circuit in a System

1. The above schematic shows recommended bypassing values based on the QPF4259 evaluation board. The customer should ensure that sufficient bypassing is provided based on their PCB layout. In addition, one should ensure all bypass capacitors are placed as close as possible to respective FEM pins, with the lowest values placed closest to the part pin. It is also recommended that at least one ground via be placed right next to each bypass capacitor ground pad to minimize ground return inductance between the capacitor and the FEM ground.

2. In case there is DC present on the lines connecting RF paths on the board, we recommend using DC block per the recommended values in the schematic. There is no DC present on RF ports of FEM internally. Low value external DC blocking capacitors, however, can be beneficial for improving ESD immunity and overall ruggedness in the presence of transients. The capacitor values should be chosen to be series resonant at approximately mid band per the component manufacturer datasheet.

3. VDET (pin 6) should not be left floating and should be terminated with 100 pF capacitors if this pin is not being used.

4. Qorvo® suggests having a series element to customer layout at the output of VDET (pin 6) to have a flexibility of low pass filter, if required. R2 can be replaced as 0 Ω. Since output of detector goes into ADC that acts as high impedance, therefore, external shunt R3 may not be needed for pin 6. Qorvo recommends using a 27 kΩ shunt as a starting point.

5. Qorvo® recommends placing a "pi" network placeholder at FEM TX, RX, ANT, and CPLR ports for tuning flexibility. In addition, try to place tuning placeholder closer to FEM. Transceiver (TXVR) matching components should be placed closer to TXVR with 50 Ω trace connecting the network placeholder near FEM port.

6. Route control lines on a separate layer, other than the signal layer, whenever possible and isolate control line traces from RF and VCC traces. Keep a minimum distance of 150 µm between TX and RX control lines to minimize coupling.

7. Having a placeholder for a series component on PA_EN, LNA_EN control lines provides a way to improve isolation.

8. Qorvo® recommends to fully populate the ground slug with as many thermal vias as possible and to add ground vias around RF traces.

9. Qorvo® recommends following the evaluation board layout guidelines as close as possible. QPF4259 evaluation board uses 12 mil vias under the FEM. Gerber files are available upon request.

10. When in operating mode, ensure ANT port on system board is always terminated and Wi-Fi chipset drive going into FEM input does not exceed FEM recommended operating range to avoid any damage.

PCB Layout Considerations

Board layout must be carefully considered to achieve optimal performance from any FEM, including the QPF4259. In addition to providing connectivity between the FEM and external components, the PCB layout is a part of the overall circuit. The RF and DC parasitic of the traces, along with coupling between traces, must be evaluated. The QPF4259 Evaluation Board PCB layout guidelines provides a good starting point for designing the layout in the actual application.

RF Traces

All the PCB traces between the RF pins and matching networks (where applicable) should be 50 Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. The RF traces should be routed on the top layer to minimize coupling with other RF, control input, and DC traces. If it is not possible for some reason to route RF traces on top layer, we suggest making sure there is proper isolation between traces on the layout to avoid any coupling issues. RF lines should be isolated from other RF and DC signals by adding solid ground planes (with vias) between them to minimize coupling or cross-talking. In addition, we also recommend reducing RF trace lengths, wherever possible as shown in **Figure 5a.**

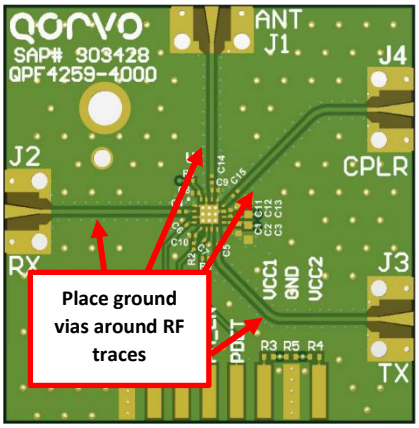


Figure 5a. Recommended PCB layout Considerations

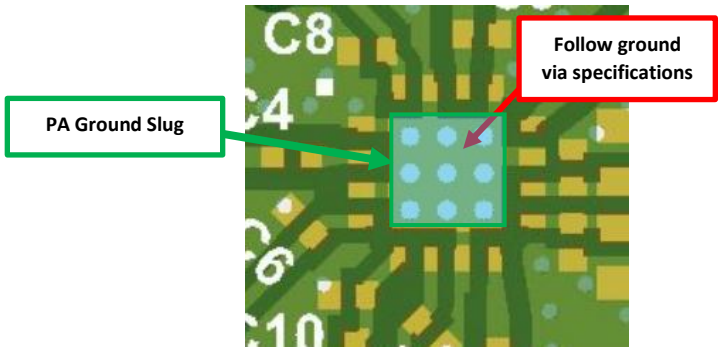


Figure 5b. Ground via placement on module ground slug

Grounding Considerations

Connect the module center ground pad directly to the main ground plane layer using as many vias as possible. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible. This ground layer also provides the reference layer for microstrip lines.

Particular attention should be paid to the grounding of the PA ground slug, the solid metalized area on the bottom side of the package. This serves as the primary RF and DC ground return for the entire PA, as well as the primary path for heat removal. A larger number of via holes should be distributed over the entire ground area below the PA to provide good RF and DC ground returns, as shown in **Figure 5b** below. Additionally, the vias will serve as a low resistance thermal path between the PA and the PCB. Vias passing through multiple copper layers provide the best overall RF, DC, and thermal performance.

Ensure proper vias on ground slug / paddle for better thermal consideration. QPF4259 ground slug / paddle has special electrical and thermal grounding requirements. This pad is the main RF ground and main thermal conduct path for heat dissipation. The GND pad and vias pattern and size used on the Qorvo® evaluation board should be replicated. The Qorvo® layout files in Gerber format can be provided upon request.

DC Layout Considerations

The most important layout consideration for the VCC DC traces is that they provide low impedances back to their main supply rail. Where possible, power planes should be used to route these traces. Where this is not possible due to space constraints, the traces should be made as wide as possible, using multiple copper layers if necessary, to achieve an equivalent width of 2 mm or more.

There should be at least one ground layer between these traces and any RF traces even though both are running diagonal to each other on different layers to minimize coupling.

When connecting all VCC pins on the board together, we recommend connecting VCC and VDD pins (pin 4, 9, 10) before bypass capacitors as shown in **Figure 5c**. In addition, we suggest running a longer trace for better isolation.

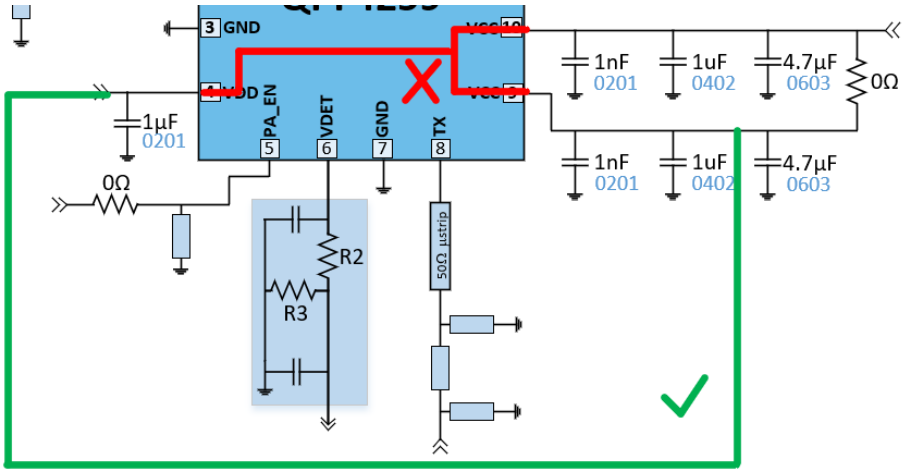


Figure 5c. Recommended PCB layout Considerations – Connecting VCC and VDD Pins

PCB Footprint Recommendations

See **Figures 6a and 6b** below for the Qorvo® recommended package outline drawing and solder mask patterns.

Land Pattern Recommendation

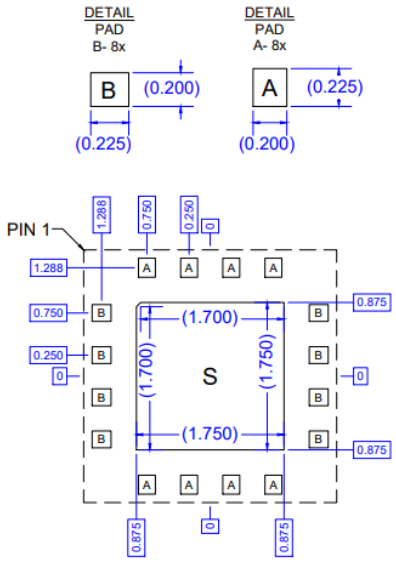


Figure 6a. PCB Footprint Recommended Landing Pattern

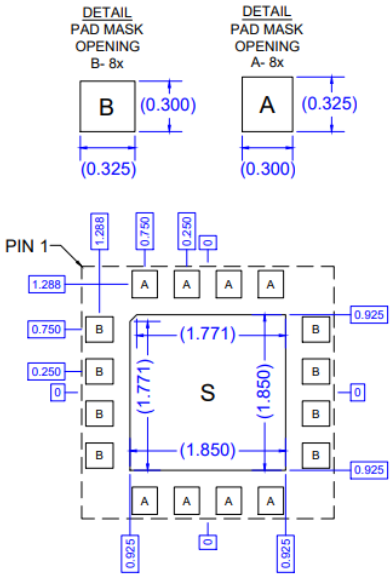


Figure 6b. PCB Footprint Recommended Solder Mask Pattern

Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Package Information

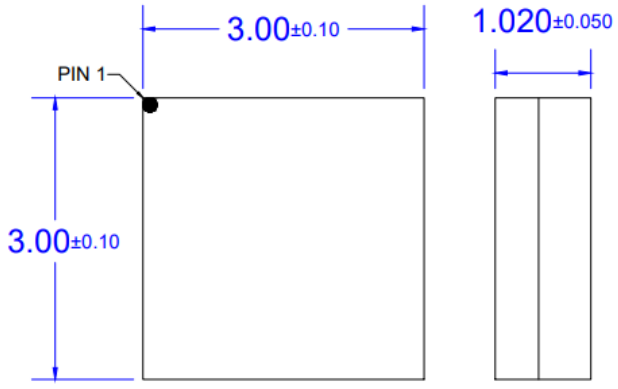


Figure 6c. QPF4259 Marking Diagram

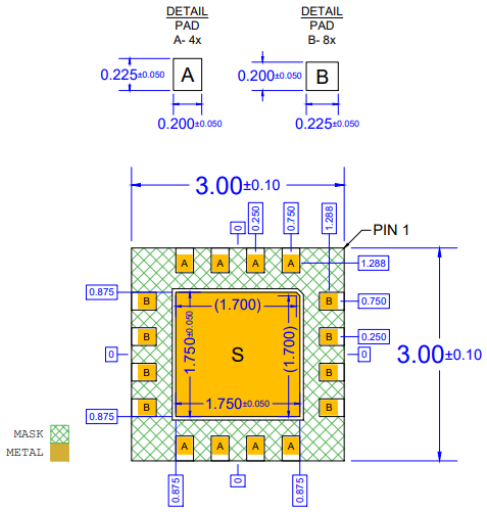


Figure 6d. QPF4259 Package Outline Drawing

Package Style: Laminate
Dimensions: 3.00 x 3.00 x 1.020 mm

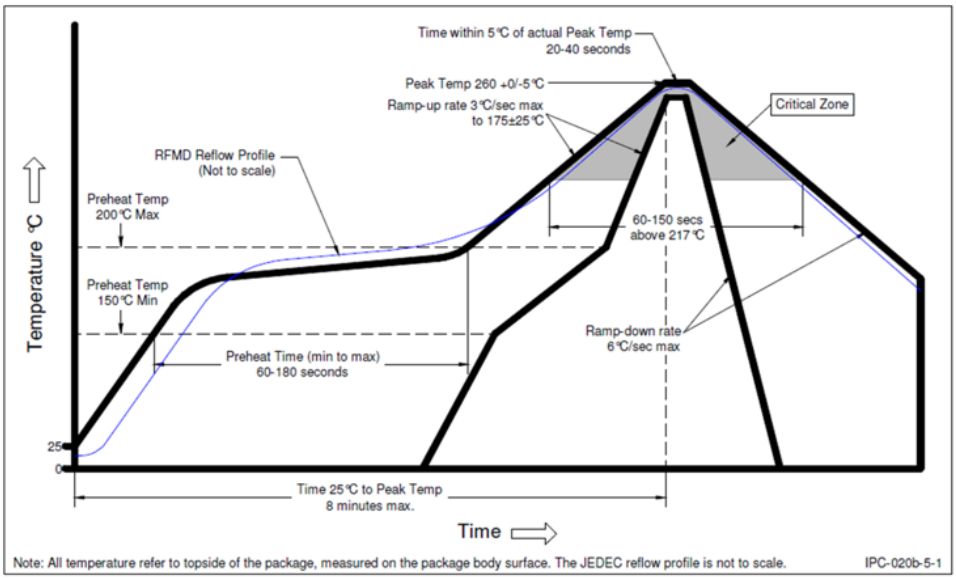
Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo® evaluation board for this product.
3. Some modifications may necessary to suit end user assembly materials and processes.

Shielding

To prevent any external electromagnetic interference (EMI) from affecting the sensitivity, follow the chipset partner shielding recommendation.

Reflow Profile & Solder Paste



Solder Reflow Recommendation

This information is provided as a guideline to facilitate the successful implementation of a surface mount process customized to the user's requirements.

Solder Reflow Equipment

Recommendations provided are based on a 100% convection reflow oven capable of maintaining temperatures specified in Joint Industry Standard IPC/JEDEC J-STD-020.

Reflow Profile Notes

An optimized reflow profile depends on several factors such as the solder paste, board density and type of reflow equipment used. Additional reflow information can be obtained from solder paste vendor data sheets.

It is recommended that any reflow profile be characterized with a fully populated production PCB. Thermocouples can be used to record temperatures across the surface and any sensitive components on the PCB. Ensure that a thermocouple is placed in contact with the top surface of any moisture sensitive component to ensure maximum temperature is not exceeded.

High Temperature Reflow Profile

Maximum reflow temperature is 260 °C. The temperature used to classify the MSL level appears on the MSL label on each shipping bag. Qorvo® uses reflow profiles in accordance with IPC/JEDEC J-STD-020 for qualification with the exception of the maximum reflow temperature of 260 °C.

Table 4. Qorvo® Recommended Reflow Profile & Conditions

CONDITIONS	
Ramp-up rate	3 °C/second max.
Preheat temperature 175 (±25) °C	180 seconds max.
Temperature maintained above 217 °C	60-150 seconds
Time within 5 °C of actual peak temperature	20-40 seconds
Peak temperature range	260 +0/-5 °C
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
Maximum number of reflow cycles	≤3
Pre-baking requirements	Refer to JEDEC J-STD-033 if original device package is unsealed.
Maximum reflow temperature	260 °C

Table 5. Qorvo® Recommended Low Temperature Solder Paste Specifications

SPECIFICATIONS	
Solder paste	Multicore RP11
Alloy type	Sn62/Pb36/Ag2
Metal content	89.5%
Solder particle size	45 µm to 20 µm

Table 6. Qorvo® Recommended High Temperature Solder Paste Specifications

SPECIFICATIONS	
Solder paste	Multicore 96SCAGS89 (CR39)
Alloy type	Sn95.5/Ag3.8/Cu0.7
Metal content	88.5%
Solder particle size	45 µm to 20 µm

A no-clean solder paste is recommended since it is difficult to completely clean residues under low profile components after they have been soldered to the PCB. Eliminating residues reduces the possibility of solder bridging between non-connected pads. This condition is affected by time, temperature, and humidity and will not be visible during initial inspection after reflowing.

Inspection

It is recommended that x-ray inspection be performed for any solder joints that are not visible after assembly. The following analysis and inspection criteria have been shown to result in component attachments that pass all Qorvo® package qualification procedures:

- Evaluate solder paste printing process. Measure print height, and paste slump.
- Perform visual inspection for excess solder on terminal pads before and after reflow.
- Perform x-ray to inspect for proper alignment, solder voids, solder balls, and solder bridging after reflow.
- Check for a minimum of 90% solder coverage on pad.
- There should be sufficient solder coverage on ground pads and I/O.

- Inspect for solder bridging or splatter between I/O pads.

Support Data

For any further data on the QPF4259, please request Qorvo® point of contact such as marketing, sales or a representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo® for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

Important Notice