APPLICATION NOTE

QPQ5200

Wi-Fi CH1-11 Edge Boost BAW Filter

Product Overview

The purpose of this application note is to help customers translate the layout and design guidelines for the Qorvo® QPQ5200 Bulk Acoustic Wave (BAW) band-pass filter.

The Qorvo® QPQ5200 is a high-performance, high power, Bulk Acoustic Wave (BAW) band-pass filter with extremely steep roll-offs, simultaneously exhibiting low loss in the Wi-Fi channels 1 – 11, and high near-in rejection in the 2.4 GHz band-edge and adjacent LTE/TD_LTE bands.

The filter module is specifically designed to enable industry's leading capacity performance in Wi-Fi applications that result in higher power capacity in more Wi-Fi channels.

This application note serves the purpose of component integration while using advanced laminate module packaging techniques to achieve high integration in an industry leading compact footprint. And at the same time negating as many external passive component placements to assist end users ease of integration into their circuits.

Product Details

Figure 1a. Device Packaging Detail

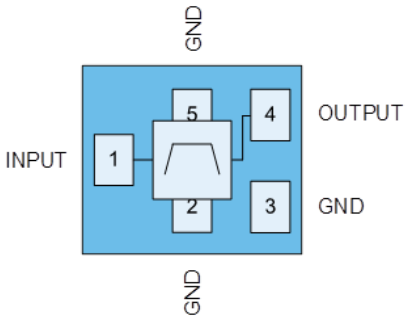


Figure 1b. Functional Block Diagram & Pin-Out Detail

Table 1. QPQ5200 Pin Description

PIN NUMBER	LABEL	DESCRIPTION
1	INPUT	RF input.
2	GND	Ground connection.
3	GND	Ground connection.
4	OUTPUT	RF antenna port.
5	GND	RF Ground connection. Use recommended via pattern to minimize inductance and thermal resistance.

Notes:

1. The Transmit (Pin 1) and Antenna (Pin 4) ports are both bidirectional for small signals only.
2. It's recommended not to exceed the max power handling conditions specified on the data sheet or permanent damage may occur.

Evaluation Board Information

The Qorvo® QPQ5200 evaluation board is designed to provide performance representative of that obtainable in an actual application. The evaluation board is designed to operate with 50Ω load impedances at all RF ports, which are provided with SMA connector interfaces.

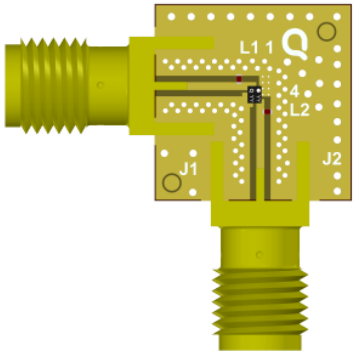


Figure 2a. QPQ5200 Evaluation Board PCB

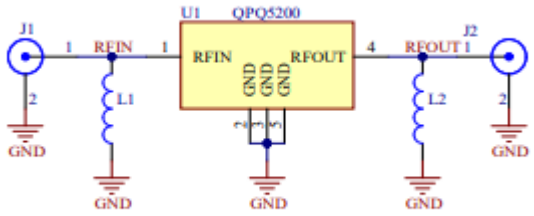
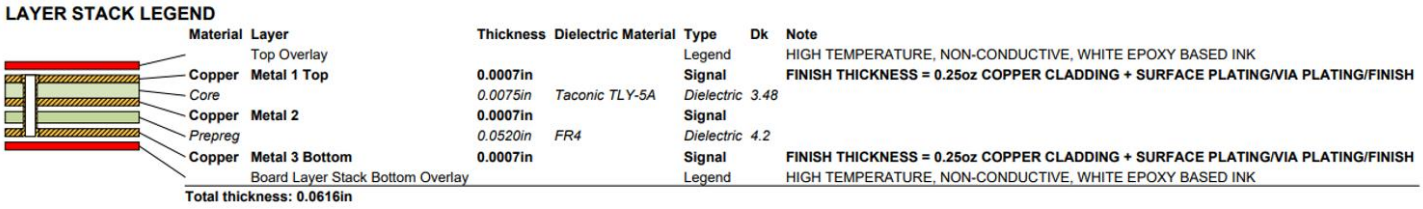


Figure 2b. QPQ5200 Evaluation Board Schematic

QPQ5200 PCB Stack-Up



LAYER STACK LEGEND

Material	Layer	Thickness	Dielectric Material	Type	Dk	Note
	Top Overlay			Legend		HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK
Copper	Metal 1 Top	0.0007in		Signal		FINISH THICKNESS = 0.25oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH
Core		*0.0075in*	*Taconic TLY-5A*	*Dielectric*	*3.48*	
Copper	Metal 2	0.0007in		Signal		
Prepreg		*0.0520in*	*FR4*	*Dielectric*	*4.2*	
Copper	Metal 3 Bottom	0.0007in		Signal		FINISH THICKNESS = 0.25oz COPPER CLADDING + SURFACE PLATING/VIA PLATING/FINISH
	Board Layer Stack Bottom Overlay			Legend		HIGH TEMPERATURE, NON-CONDUCTIVE, WHITE EPOXY BASED INK

Total thickness: 0.0616in

Note:

Total PCB Thickness: 0.0616in

Table 3. QPQ5200 Evaluation Board Bill of Materials

REF. DES.	VALUE	DESCRIPTION	MANUF.	PART NUMBER
-	-	Printed Circuit Board		
U1	-	Wi-Fi Band edge BAW Filter	Qorvo	QPQ5200
L1	10 nH	0201 chip inductor, ± 3%	Murata	LQP03TN10NH02
L2	10 nH	0201 chip inductor, ± 3%	Murata	LQP03TN10NH02
SMA	-	SMA connector	Radiall	9602-1111-018

System Architecture Application Circuit Recommendations

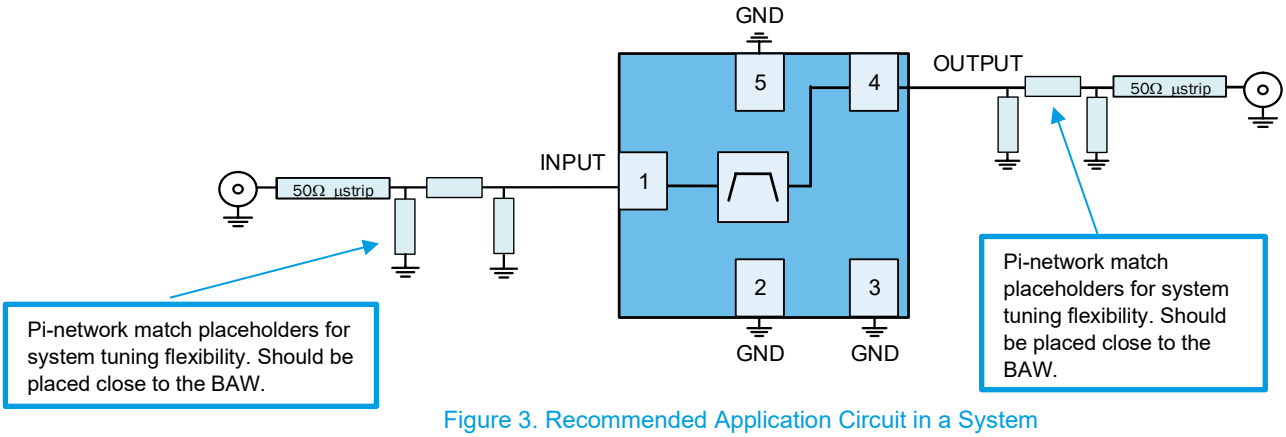


Figure 3. Recommended Application Circuit in a System

RF Matching Considerations

The above schematic shows Qorvo® recommended Pi-network match placeholders for system tuning flexibility based on the QPQ5200 evaluation board and should be placed close to the BAW.

- The customer should ensure that sufficient Pi-matching is provided based on their PCB layout.
- If additional out-of-band rejections/ attenuations are needed the matching at the output port will help to improve the filtering.
- Matching at the Input port side of the BAW will help in improving the in-band ripple and insertion loss.

PCB Layout Considerations

The board layout must be carefully considered to achieve optimal performance from any BAW filter, including the QPQ5200. In addition to providing connectivity between the BAW and external components, the PCB layout is a part of the overall circuit. The PCB parasitics of the RF traces, along with coupling between traces, must be evaluated. The QPQ5200 evaluation board PCB layout guidelines provide a good starting point for designing the layout in the actual application.

RF and DC Trace Routing

All PCB traces between the RF pins and matching networks (where applicable) should be 50Ω controlled impedance lines, as should the traces between the matching networks and the next component in the chain. RF traces should be isolated from other RF and DC signals from other components by adding solid ground planes (with vias) between them to minimize coupling or cross-talking. All DC traces routed near the BAW must be isolated from the BAW with a GND in between the BAW and the DC trace. Qorvo® recommends to avoid routing traces/ tracks underneath the BAW.

In addition, Qorvo® also recommends reducing RF trace lengths, wherever possible. Fenced or shielding vias are recommended around RF traces to help maintain a low impedance or short return current path.

Grounding Considerations

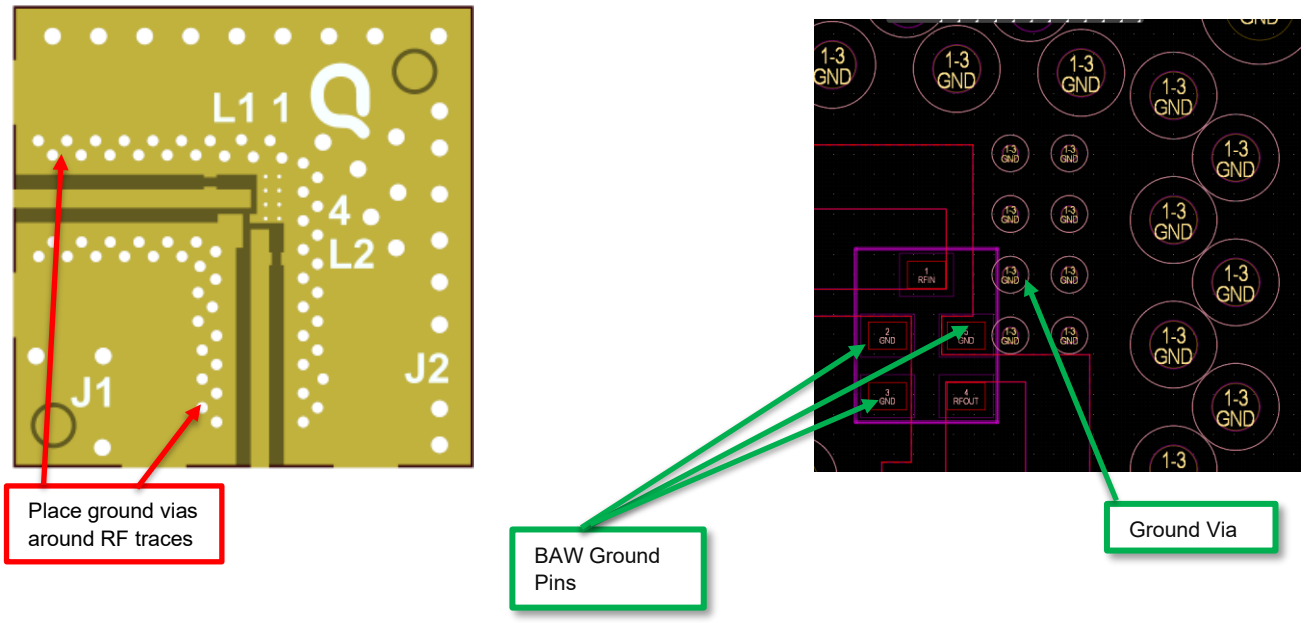
Grounding of BAW GND pad – The ground pad serves as the primary RF ground reference for the entire BAW. Connect the BAW filter ground pins directly to the main ground plane layer of the PCB. The PCB ground layer should be close to the component layer, preferably the next layer down to minimize the lengths of via connections between the component and ground layers. Ground paths (under device) should be made as short as possible to reduce inductance.

Reference Plane Ground – Qorvo® recommends distributing a large number of via holes over the entire area below/around the BAW to provide good RF ground reference ground plane, as shown in the thermal via array pattern in **Figure 4**. The GND planes on the rest of the PCB should have vias on them which route from the top layer through to the bottom GND layer.

GND Vias for Thermal Considerations – The BAW GND pins serve as the primary path for heat removal, additionally, the PCB ground vias will serve as a low resistance thermal path between the BAW and the PCB. Vias passing through multiple copper layers provide the best overall RF and thermal performance. The QPQ5200 ground pins have special electrical and thermal grounding requirements. These pins are the main RF ground and main thermal conduction path for heat dissipation. The GND pins, vias pattern, size, and type used on the Qorvo® evaluation board should be replicated on the final product. The Qorvo® layout files in Gerber format can be provided to the reader upon request.

- The QPQ5200 evaluation board uses through-hole GND vias with a 4mil hole and 8mil diameter beneath the BAW on the BAW GND Pins and it uses 12mil hole and 22mil diameter GND vias along RF traces.
- Qorvo recommends using GND vias between 4mil and 9.5mil hole size and to follow the thermal via array patterns similar to what's shown in **Figure 4.**
- Qorvo® recommends using a **Direct Connect** ground connection underneath the QPQ5200 rather than use the Thermal Relief style ground connection.
- The Qorvo® QPQ5200 Evaluation Board uses Filled Vias on the GND pad. It is recommended to have GND vias on all GND pins.

Figure 4. Recommended PCB layout Consideration



Land Pattern Recommendation

PCB Footprint Recommendations

See **Figures 5a and 5b** below for the Qorvo® recommended package outline drawing and solder mask patterns.

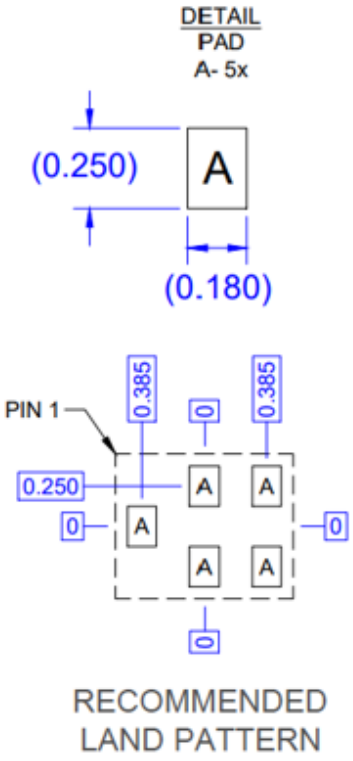


Figure 5a. PCB Footprint Recommended Landing Pattern

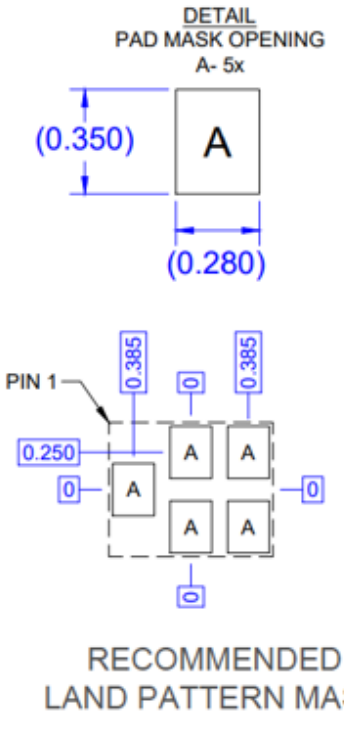


Figure 5b. PCB Footprint Recommended Solder Mask Pattern

Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
4. Qorvo® recommends to use a 2mil e-FAB stencil.

Package Information

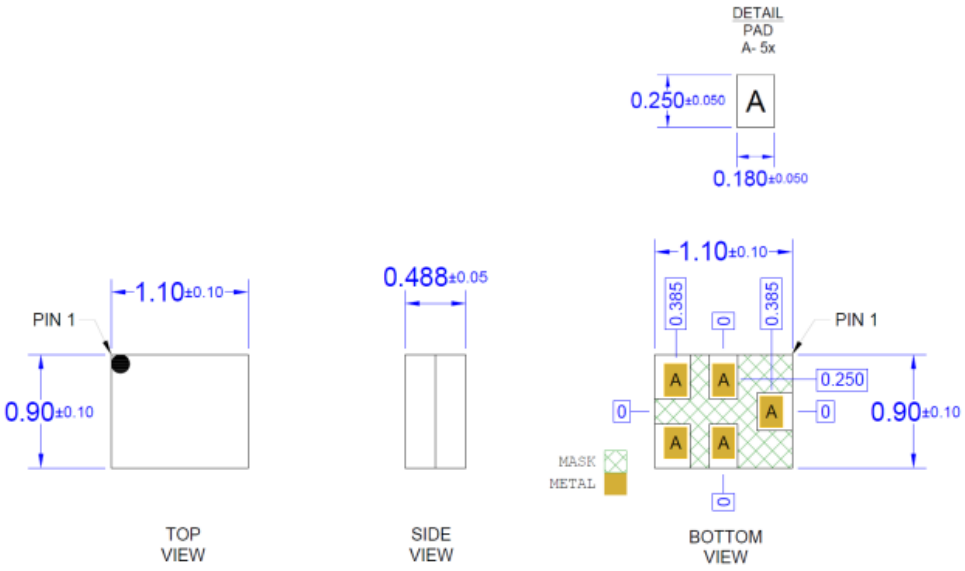


Figure 6a. Marking Diagram

Figure 6b. QPQ5200 Package Outline Drawing

Package Style: Laminate
Dimensions: 1.1 x 0.9 x 0.488 mm

Notes:

1. All dimensions shown are in millimeters. Angles are in degrees.
2. This drawing specifies the mounting pattern used on the Qorvo® evaluation board for this product.
3. Some modifications may be necessary to suit end user assembly materials and processes.

Support Data

For any further data on QPQ5200, please request Qorvo® point of contact such as marketing, sales or a representative in your region.

Additional Information

For information on ESD, Soldering Profiles, Packaging Standards, Handling and Assembly, please contact Qorvo® for general guidelines.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
Web: www.qorvo.com
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Email: customer.support@qorvo.com

Important Notice