PAC Battery Management System Guide

Abstract

This document outlines Qorvo's Power Application Controller® (PAC) battery management systems for higher voltage battery powered equipment, including lawn & garden tools, construction tools, e-bikes, e-scooters, energy storage, recreational vehicles, robots, drones, uninterruptible power supplies, golf carts, and industrial applications. It describes the PAC BMS product series, functions, and high-level operation. Further implementation details are contained in the corresponding product-specific datasheets, application notes, and user guides.

1. Introduction

This application note covers Power Application Controller® (PAC) battery management systems (BMS) that monitor battery parameters, including cell voltages, interrupt battery current, manage power, and actively balance cells with balancing transistors and resistors (not a switching power converter). This document supplements datasheets and user guides by describing operation of main functions and summarizing features.

Table 1-1. PAC BMS series features at a glance

Feature	PAC25140
Package	QFN 10x10 mm, 68-pin
Variants	**PAC25140N** offset pad **PAC25141N** same as PAC25140N but 16S maximum
Cell count	10S – 20S (PAC25141N supports 10S – 16S)
Power management	19 to 145 V input buck, regulators
CHG/DSG gate drivers	High-side
FUSE driver	Low-side
Source follower mode	Yes
Current sense ADC	16-bit sigma-delta
Battery voltage sense ADC	16-bit sigma-delta
Comparators	SCP, OCD, OCC
MCU core	150 MHz Arm® Cortex®-M4F with floating point unit
MCU FLASH / SRAM	128 KB code protection / 32 KB
MCU ADC	12-bit SAR, 2.5 MSPS
ADC sequencer	DTSE with pseudo-DMA, 24 channels
Debug interface	SWD, JTAG, Embedded Trace Module
UART	3x
SPI, I2C/SMBus	Yes
CAN	Yes (CAN 2.0B)
Hibernate current	3 µA
Wake sources	PB, PACK+, timer
Watch-dog timer	2x windowed with independent clock
Low-speed independent clock	Yes

Each BMS is highly integrated thanks to a high voltage fabrication process. Precision amplifiers, comparators, bias circuitry, isolated gate drivers, power supplies, PWM controller with associated feedback and compensation components, voltage regulators, and voltage supervisors are all included in the BMS, greatly reducing board space and cost as well as design time and risk.

The PAC2xxxx BMS works with relatively high-power battery packs, such as lawn & garden power tools, e-bikes, scooters, and other outdoor power equipment. High power requires high series cell count, designated with suffix S. Common battery pack configurations range from 10S to 20S corresponding to nominal voltages of 32 to 80 V depending on chemistry. Qorvo PAC battery management systems are configurable and accurately measure cell voltages ranging from 1.8 to 4.7 V and so can work with any battery chemistry.

2. Safety

Fig. 2-1 shows a portion of the PAC2xxxx block diagram including battery disconnect and secondary fuse protection circuitry. The PAC2xxxx BMS includes all necessary protection features to safely and fully utilize lithium-based batteries. The BMS drives two external MOSFETs that are connected back-to-back (common drain) to enable bidirectional battery current blocking. A third MOSFET can activate a Self Control Fuse (SCF), also called Self Controlled Protector. Note that MOSFET gate-source pull-down resistors and optional transorbs (back-to-back Zeners) are omitted for clarity. Please refer to datasheets, user guides, and application note [1] for a detailed design example, recommended component values, and implementation details.

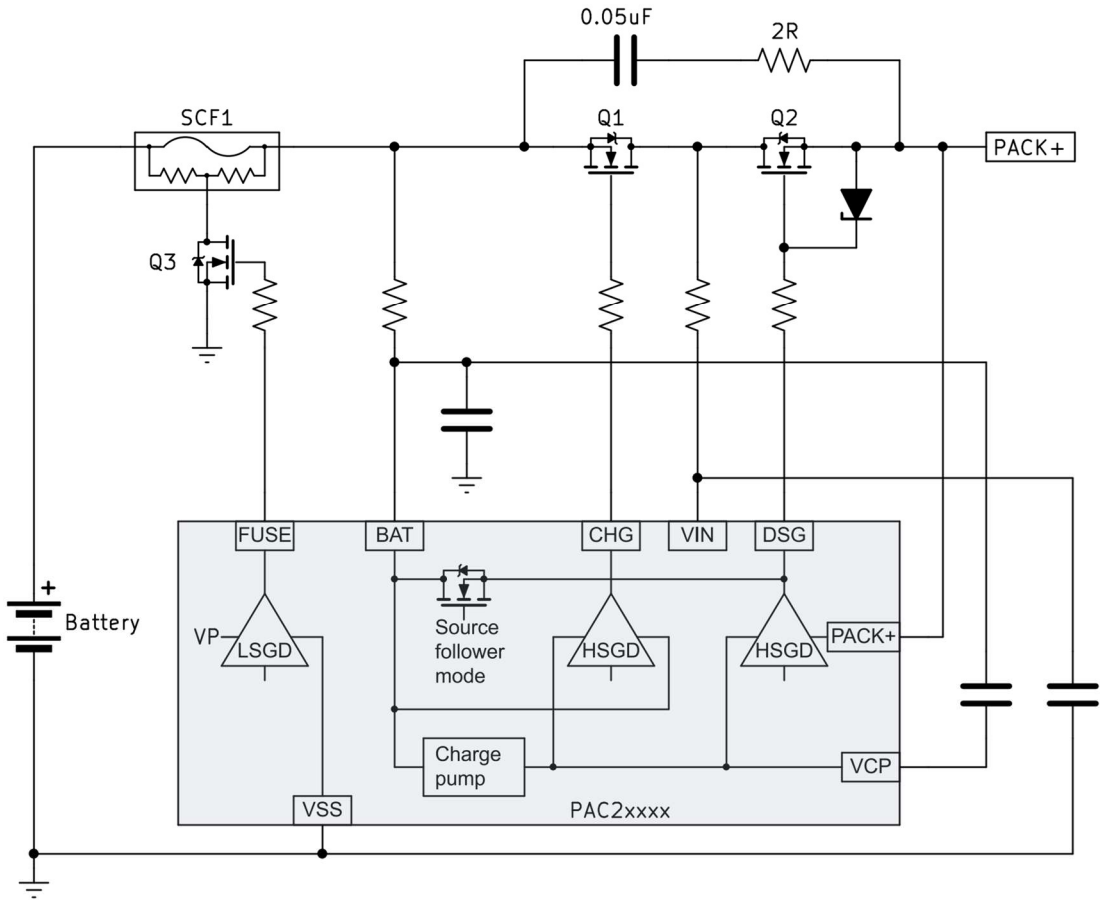

Fig. 2-1. PAC2xxxx battery disconnect with internal drivers for external MOSFETs

The MOSFETs Q1 and Q2 in Fig. 2-1 are connected by their drains so that they can operate independently [2]. The battery can charge only if Q1 is on, and discharge (power a tool) if Q2 is on. The battery pack is disconnected from the load or charger when Q1 and Q2 are off. Therefore, Q1 and Q2 in combination with the PAC2xxxx function as a solid-state circuit breaker and battery disconnect.

Source follower mode is an option for low discharge current operation. In this mode, the charge pump and Q1 drive are off, and Q2 is driven by an internal pull-up MOSFET to BAT, hence a source follower configuration. Note that a Zener diode or transorb is required for source follower mode and the usual gate resistor.

When Q1 and Q2 switch on, such as when a battery is plugged into the tool, an inrush current spike into the tool's DC link capacitors could cause a glitch pulling VCP below its undervoltage lockout threshold, which sends a fault indication to the firmware. If this happens, consider using a pre-charge mode (resistor + small relay for example) or use source follower mode to pull the load capacitor up. Using high gate resistance is discussed in application note [1]. During normal operation the charge and discharge MOSFETs are on and the internal pull-up MOSFET is off to minimize power loss. A resistor-capacitor snubber across Q1 and Q2 is recommended to limit the voltage slew rate when Q2 or Q1 switch on or off. Again, see [1] for details.

In the Configurable Analog Front End (CAFE™), there is a current sense differential programmable-gain amplifier and three protection comparators: one for short circuit discharge protection, one for over-current discharge protection, and one for over-current charge protection. When one of the comparators trips, the PAC2xxxx sends a signal to the driver manager, which can be programmed in various ways to switch off the charge and discharge MOSFETs, as well as interrupt the MCU. Each of the comparators has an 8-bit digital-to-analog converter (DAC) to set the comparator reference. Once configured, the CAFE in combination with the charge and discharge MOSFETs protect from overcurrent or short circuit conditions independent of MCU code execution. In addition to automatic overcurrent and short circuit protection functionality, the CAFE has a dedicated, high resolution 16-bit current sense ADC that enables Coulomb counting for battery state of charge and health calculations. This ADC has an input multiplexor for safety checks of the overcurrent charge and discharge DACs.

The CAFE also features a battery overvoltage comparator and DAC. If the comparator trips, the CAFE can be configured to automatically switch off Q1 and/or Q2 and generate an MCU interrupt. In addition to automatic battery overvoltage protection functionality, the CAFE has a dedicated 16-bit battery voltage ADC with an input multiplexor for battery cell voltage measurements and safety checks of the battery overvoltage DAC and short circuit protection DAC. The high resolution of the 16-bit ADC enables precise cell voltage measurements despite a high cell count of up to 20 series-connected battery cells.

For a second level of protection, there is an external fuse MOSFET, which is Q3 in Fig. 2-1. This works in conjunction with the Self Control Fuse (SCF), labeled SCF1 in Fig. 2-1. The SCF provides two-in-one protection. First, it is a fuse, and it will blow if an abnormally high current persists too long. Second, when the fuse MOSFET Q3 switches on, current flows through a heater in the SCF, causing the SCF fuse to quickly blow. Switching the fuse MOSFET requires MCU code, such as in a battery overvoltage fault interrupt service routine. The SCF is not resettable, so if it blows, the battery pack cannot be used until the SCF is replaced. If the system design omits the SCF, then the FUSE output can be used for another purpose such as driving an LED or relay.

A 12-bit ADC and input multiplexer can sense the internal temperature, all internal and pin-accessible voltages, DAC voltages, and other internal parameters. Additionally, up to 7 external analog signals are multiplexed to the ADC. There are two internal temperature warning thresholds, the first at 120 °C and the second at 140 °C, and an automatic shutdown threshold at 155 °C that causes Q1 and Q2 to switch off, among other things. Some or all the external analog signals can be from battery temperature sensors thus providing protection from battery overheating.

If any internal voltage falls below its respective power good threshold voltage, a fault event is detected and the MCU is reset. The MCU stays in the reset state until the internal supply rails are all good again and the reset time has expired.

PAC2xxxx BMS include an independent, low-speed clock as needed by UL or IEC60730 Class B safety standards. This clock has an output that can be connected on the circuit board to a digital input so that the MCU firmware can detect any issues with the clock such as failure or frequency drift. These PACs also include a windowed watchdog timer with independent clock.

3. Cell Balancing

The probability of cell mismatch increases with cell count. Therefore, in many large cell-count battery applications (>10 cells in series), cells should be balanced to achieve maximum runtime and battery service life as well as ensure safe operation. The PAC2xxxx devices support passive cell balancing, meaning no power conversion is used. Cells are alternately partially discharged with energy dissipated in internal or external transistors, and in external resistors. Internal PAC2xxxx cell balancing is limited to less than 50 mA due to heating. When internal cell balancing cannot support the desired balancing current, external transistors can increase the current to more than 200 mA. The PAC2xxxx firmware controls cell balancing regardless of internal or external transistor use. Cell balancing is described in detail in datasheets and in application notes [1] and [3].

4. Power Management

All Qorvo PACs have integrated power management. All have voltage regulators to generate various required internal voltages. Each PAC2xxxx includes a gate driver for an external power transistor and a switch-mode controller with an internally compensated (stabilized) feedback loop, making it easy to power the PAC. See Fig. 4-1. Recommended component values are listed in datasheets and/or user guides.

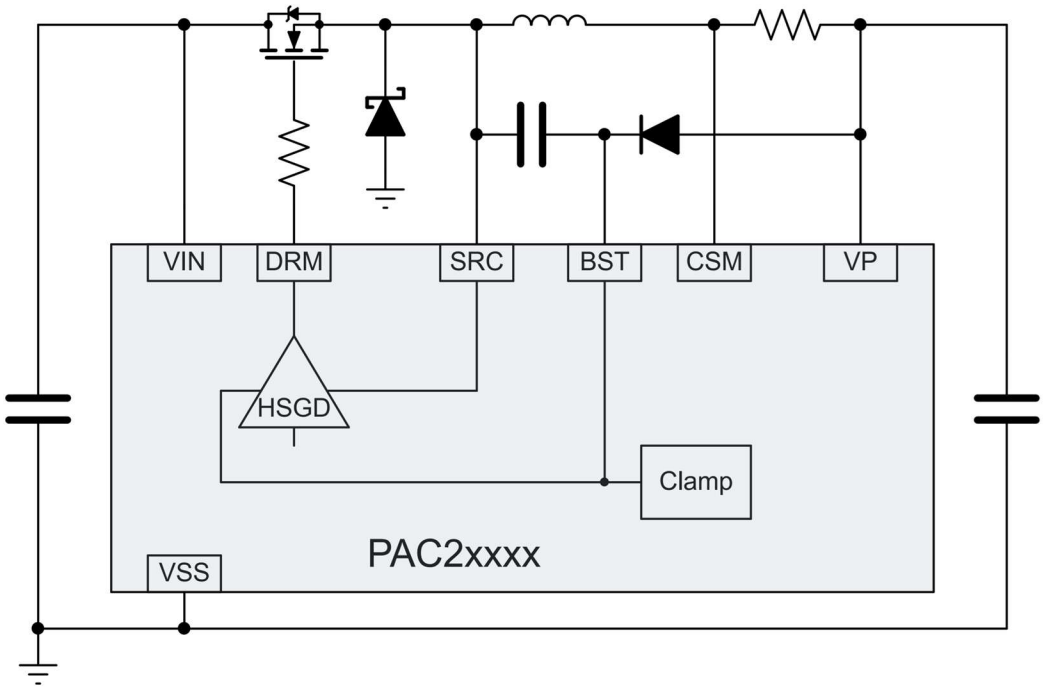

Fig. 4-1. PAC2xxxx buck converter

The buck converter utilizes an external MOSFET, diodes, inductor, current sense resistor, and capacitors. Its function is to produce a regulated power supply for internal use with a voltage lower than the battery pack voltage. Note that the internal buck controller, gate driver, and bootstrap supply eliminate from the circuit board assembly a buck controller IC, feedback compensation components, an isolated gate driver, and a voltage supervisor. The design and test time for the buck converter are greatly reduced.

Technical tip: A bootstrap gate drive power supply requires continuous switching to maintain sufficiently steady voltage. Continuous switching is certainly the case with a buck converter, so the PAC2xxxx buck converter uses a bootstrap power supply. The advantages of bootstrap power supply are low cost, low component count, and simple open-loop operation. On the other hand, the charge and discharge (circuit breaker) MOSFETs Q1 and Q2 in Fig. 2-1 must remain on or off indefinitely, which is why their gate drive power is from a charge pump, which operates continuously whenever enabled.

5. Processing

Each PAC25xxx BMS contains a 150 MHz Arm® Cortex®-M4F 32-bit microcontroller core with floating point unit (FPU), 128 KB of FLASH, and 32 KB of SRAM. Peripherals include pulse width modulation (PWM) and other timers, analog-to-digital converters (ADC) with associated state machine, various serial communications, and security. See Table 1-1

Each BMS has an industry leading low-power mode called sleep or hibernate mode. This important feature keeps a battery pack ready for use with full charge even after months of storage. There are various ways to exit sleep mode including a button press, timer, and battery pack or charger detection.

6. Communication

There are multiple options for a PAC BMS to communicate with other ICs or externally. Table 6-1 lists communication peripherals included in each Qorvo PAC BMS. Note that SWD is used for both debugging and programming. JTAG can also be used for programming if included.

Table 6-1. Communication and debug/program interfaces

Series	Communication and Debug Peripherals	Notes

PAC25xxx	• 3 x USART (Either SPI or UART)
	  ○ SPI Master/Slave up to 25 MHz
	  ○ UART up to 1 Mbps
	• I2C/SMBus Master/Slave
	• CAN 2.0B Controller
	• SWD
	• JTAG
	• Embedded Trace Macrocell (ETM)
		• SMBus is a variant of I2C.
		• JTAG (Joint Test Action Group) is also known as boundary scan and is covered by IEEE 1149.x standards.

References

[1] J. Dodge, “Outdoor Power Equipment Design Guide,” Qorvo. [Online]. Available: https://www.qorvo.com/products/d/da009838
[2] Application note, “PAC2xxxx BMS Parallel FET Operation,” Qorvo. [Online]. Available: https://www.qorvo.com/products/d/da009026
[3] Application note, “PAC2xxxx External Cell Balancing,” Qorvo. [Online]. Available: https://www.qorvo.com/products/d/da009029

Revision History

Revision	Author	Date	Description
A	Jonathan Dodge, P.E.	12 September 2025	Initial draft
B	Jonathan Dodge, P.E.	20 October 2025	Changed battery monitoring to PAC battery management
C	Jonathan Dodge, P.E.	26 February 2026	Focused on PAC25140

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