Qorvo Motor Control & Drive System Guide

Abstract

This document outlines Qorvo's Power Application Controller® (PAC) intelligent motor controller & drive (MCD) solutions for higher voltage battery powered equipment, including lawn & garden tools, construction tools, e-bikes, e-scooters, energy storage, recreational vehicles, robots, drones, uninterruptible power supplies, golf carts, and industrial applications. It describes the PAC MCD product series, functions, and high-level operation. Further implementation details are contained in corresponding product-specific datasheets, application notes, user guides, and evaluation kits.

1. Introduction

This application note covers Power Application Controller® (PAC) intelligent motor control and drive (MCD) solutions that drive external sets of half-bridge MOSFETs, monitor current and voltages, and manage power. This document supplements datasheets and user guides by describing operation of main functions and summarizing features and differences of each MCD. The intent is to facilitate part selection and application.

2. Part Number Decoder

The wide range of intelligent motor controllers from Qorvo can cause confusion when choosing one for an application. Also, as is often the case, there are multiple correct answers. This section provides an overview of all PAC motor controllers and the main differences. It also includes the ACT72350, which is derived from PAC5x32 without the MCU core and uses a Serial Peripheral Interface (SPI) port for register configuration and status. These are referred to collectively as MCD.

Qorvo MCDs have internal gate drivers for at least six external MOSFETs or IGBTs in a triple half-bridge arrangement. There are two exceptions to this. First, the PAC5285 has six internal drivers and six *internal* MOSFETs. Second, the PAC5210 has three open-drain drivers because it is intended for use with an intelligent power module (IPM) with integrated gate drivers, deadtime generator (interlock), and power transistors. All the remaining PAC5xxx controllers are designed to drive low and high-side MOSFETs or IGBTs, henceforth referred to only as MOSFETs.

Table 2-1 below lists all MCD products to date. Highlighted items are newly released with added features preferable for new designs. Definitions of abbreviations and terms are:

- TP: Totem-Pole driver, drives high and low
- OD: Open-Drain driver that only drives low
- HV Buck: Internal controller, external transistor, diode, inductor, and bootstrap power
- MV buck: Internal controller, transistor, and diode; external inductor
- Buck: Internal controller and optional clamp, external transistor, diode, inductor,
- SEPIC: Single-ended primary-inductor converter with overlapping input and output voltage ranges
- CBC: cycle-by-cycle overcurrent protection by truncating conduction duration
- WWDT: Windowed watchdog timer with separate clock configurable for reset within a certain time window
- V_{DS} sense: Drain-source voltage sense to detect desaturation of external power transistors
- nBRAKE/nDRVDIS: Redundant microcontroller overrides control of motor drive power transistors with nBRAKE and nDRVDIS signals
- Diff-PGA: Precision differential programmable amplifier
- PGA: Precision programmable amplifier
- Simultaneous-SH: Multiple simultaneous sample-and-hold, for example simultaneously samples each phase current
- M0 and M4F: Arm® Cortex®-M0 and -M4F microcontroller core

Table 2-1. Motor controller and driver part numbers and differentiating features

Part # \ Feature	MCU	600 V	160 V	72 V	40 – 52 V	AC-DC Flyback	AC Input	HV + MV Buck	Buck	SEPIC	Simultaneous-SH	CBC	WWDT	V_{DS} Sense	nBRAKE/nDRVDIS	Diff-PGA	PGA	Notes
PAC5256	M0	•					•	•				•				3	4	
PAC5556[A]	M4F	•					•	•				•	•			3	4	PAC5556A is more recent
PAC5250/5 [1]	M0	•				•			•		•					3	4	6 low, 3 high, 2 low OD drivers 5 ≤ Vin ≤ 52 but high-side driver 600 V PAC5255 adds a clock out
PAC5253 [2]	M0	•				•			•		•					3	4	4 low, 3 high, 2 low OD drivers 5 ≤ Vin ≤ 52 but high-side driver 600 V
PAC5232[A]	M0		•					•				•				3	4	[A] eliminates buck restart delay
PAC5532[A,B]	M4F		•					•				•	•			3	4	[A,B] eliminate buck restart delay
ACT72350	–		•					•				•			•	3	4	No integrated MCU
PAC5223/5	M0			•		•			•	•	•					3	4	PAC5225 adds a clock out
PAC52700	M0			•							•					1	4	5 ≤ Vin ≤ 20 but high-side 72 V
PAC52723	M0			•					•	•	•	•				3	4	
PAC52710	M0			•					•	•	•	•		•		3	4	
PAC52711	M0			•					•	•	•	•		•	•	1	4	
PAC5523/4[A]	M4F			•					•	•			•			3	4	PAC5524[A] 64- vs. 48-pin pkg [A] versions use v2 vs. v1 MCU
PAC55723/4[L]	M4F			•					•	•	•	•	•			3	4	PAC55724 64- vs. 48-pin pkg [L] wider pitch, larger package
PAC55710/12	M4F			•					•	•	•	•	•	•		3	4	PAC55712 64- vs. 48-pin pkg
PAC55711/13	M4F			•					•	•	•	•	•	•	•	1	4	PAC55713 64- vs. 48-pin pkg
PAC5210	M0				•	•			•		•					3	4	3 low-side OD drivers
PAC5220	M0				•	•			•		•					3	4	3 low, 3 high, 2 low OD drivers
PAC52400	M0				•						•					1	4	5 ≤ Vin ≤ 20 but high-side driver 44 V
PAC52410	M0				•				•	•	•	•		•		3	4	
PAC52411	M0				•				•	•	•	•		•	•	1	4	
PAC52422	M0				•				•	•	•	•				3	4	
PAC5222	M0				•				•	•	•					3	4	
PAC5285	M0				•											1	0	Charge pump, internal MOSFETs
PAC5526[A]	M4F				•							•	•			1	5	Charge pump, MV buck-boost [A] versions use v2 vs. v1 MCU
PAC5527[A]	M4F				•							•	•			3	7	

Notes:

1. PAC5250 and PAC5255 have 6 low-side drivers and 3 high-side drivers plus 2 low-side open-drain drivers. Both have input voltage range of 5 to 52 V, but the high-side drivers can withstand 600 V. PAC5255 includes 2nd clock source for IEC-60730 Class B, alternate with ENHS2 output, but it is otherwise identical to PAC5250.
2. PAC5253 has 4 low-side drivers and 3 high-side drivers. Input voltage range is 5 to 52 V, but the high-side drivers can withstand 600 V.

A high voltage fabrication process allows integration of power management operating within a certain voltage range. All controllers support a DC power source, and nine additionally support 120 to 240 VAC. For this reason, the first question when selecting a part number is “What type of power source supplies the equipment, AC or DC?” The second question is “What is the DC link voltage?” The recommended maximum DC voltage is two-thirds of maximum input voltage, but using a transient voltage suppression method, up to three-fourths. For example, the PAC5532x maximum input voltage is 160 V, so it could operate with a maximum battery voltage of $0.75 \cdot 160$ V = 120 V with a transient voltage suppression clamp, or $0.66 \cdot 160$ V = 107 V without one. Finally, focusing on newly released parts, when possible, quickly narrows the selection to a few parts.

3. Sensing and Comparing

All MCDs have internal temperature sensing and protection and at least one differential PGA and two corresponding overcurrent comparators and digital-to-analog converters (DACs) as part of the Configurable Analog Front End (CAFE™) module. One comparator is high-speed for detecting high-peak current spikes. The other comparator limits current, and its threshold is lower than that of the high-speed comparator, so its input can have more noise filtering because it need not respond as quickly. Once configured, response to overcurrent or internal overtemperature is independent of MCU code execution.

If any internal voltage falls below its respective power good threshold voltage, a fault event is detected and the MCU resets. The MCU stays in the reset state until the internal supply rails are all good again and the reset time expires.

3.1. V_{DS} Sensing (DESAT Detection)

Table 2-1 lists some MCDs that include drain-source voltage sensing (V_{DS} sensing) of both high and low side external MOSFETs. The purpose of V_{DS} sensing is to provide additional current surge protection on a switching cycle basis. It works by comparing conducting MOSFET V_{DS} with one of eight selectable trip threshold voltages. If V_{DS} exceeds the selected trip voltage and one of 16 selected blanking times (ranging from 250 ns to 4 µs) expires since MOSFET switch-on, then an internal V_{DS} fault comparator trips. This works on the same principle as DESAT detection, a common feature of many off-the-shelf gate drivers. Excessive current causes abnormally high V_{DS}. It is not so much a measurement of MOSFET on resistance ($R_{DS(on)}$), especially because MOSFET $R_{DS(on)}$ increases with its temperature, but rather a detection of when the conducting MOSFET begins to leave its Ohmic region and enter active mode where current is determined more by gate-source voltage V_{GS} and less by V_{DS}. In this area of operation, V_{DS} rises sharply with any increase in current.

The overcurrent protection comparators inside the PAC should trip at much lower current compared to V_{DS} sense trip current. This is important to remember when selecting trip voltage and blanking time. The purpose of V_{DS} sensing is not overcurrent protection, but rather to protect the motor drive from further malfunction when an overcurrent trip should have already happened. It is thus a parallel protection method. It is tempting to set the trip voltage and/or blanking time short enough to trip at a certain, relatively low current level. This, however, can cause false V_{DS} trips due to normal changes in real operating conditions such as MOSFET temperature and electro-magnetic interference (EMI). During a very high current surge or short circuit event, V_{DS} quickly surpasses the threshold voltage, so there is no need to set the trip voltage too low and blanking time too short. There is a tradeoff between trip voltage and blanking time: A lower trip voltage is usable with a longer blanking time, and vice versa.

Although V_{DS} sensing works on the same principle as DESAT detection in a typical MOSFET or IGBT gate driver, there are some differences. There is no external blocking diode nor blanking time capacitor. There is an RC noise filter on the VBUS pin, as shown in datasheets.

4. Safety

MCDs have a watchdog timer (WDT), and the PAC55xx motor controllers also include a windowed watchdog timer (WWDT) with an independent clock source. The WWDT has upper and lower time limits, so it must be reset within a certain time window. Instead of a WWDT, the following parts have an independent clock as needed by UL / IEC60730 Class B safety standards: PAC5222, PAC5225, PAC52400, PAC52422, PAC5250, PAC5255, PAC5256, PAC52700. This is a low-speed clock with an output that can connect on the circuit board to a digital input so that the MCU firmware can detect any issues with the clock such as failure or frequency drift.

4.1. Safety MCU

The following parts include brake and driver disable features: PAC55713, PAC55711, PAC52723, PAC52711, PAC52411, and ACT72350. A redundant safety microcontroller can drive two signals, nBRAKE and nDRVDIS, to override control of the motor drive. Note that in the ACT72350 datasheet, the nDRVDIS signal is called EN, but it functions the same. The outputs of the internal high-side drivers are named DRHx, where x represents the phase designation U, V, or W. Similarly, the low-side driver outputs are named DRLx. For the purposes of discussion, the inputs to the high-side and low-side gate drivers are PWMHx and PWMLx respectively, or simply PWM when referring to all of them.

When both nDRVDIS and nBRAKE are high (de-asserted), the internal gate drivers are enabled and follow their PWM inputs, which is normal operation. Whenever nDRVDIS is driven low, the PWM and nBRAKE signals are ignored, and DRHx and DRLx driven low so all external MOSFETs are switched off.

Braking mode is entered when nDRVDIS is kept high and nBRAKE is driven low for at least the blanking time, which is 80 µs maximum. See Fig. 4-1. In braking mode, all PWM signals are ignored, DRHx are all driven low (high-side MOSFETs are switched off), and DRLx follow the inverse of nBRAKE. While in braking mode, the safety controller drives nBRAKE low to switch on all low-side MOSFETs, which when driving a permanent magnet motor causes high braking torque. This is because the motor windings are shorted, but the motor's rotation maintains voltage (back EMF), so winding current is high, limited by winding resistance. In other words, the motor acts as a generator with resistance in its own windings as the load. The rotational energy is dumped as heat into the motor, so braking mode cannot be used consistently. This is why the safety controller can pulse nBRAKE during braking mode. When nBRAKE is high, the low-side MOSFETs switch off, so both high-side and low-side MOSFETs are off. Current can only flow through the MOSFET body diodes into the battery pack, which has a high voltage relative to the motor's back EMF, so the braking torque drops off because the motor current drops off. Thus, by pulsing nBRAKE, the safety controller can regulate the winding current and braking torque.

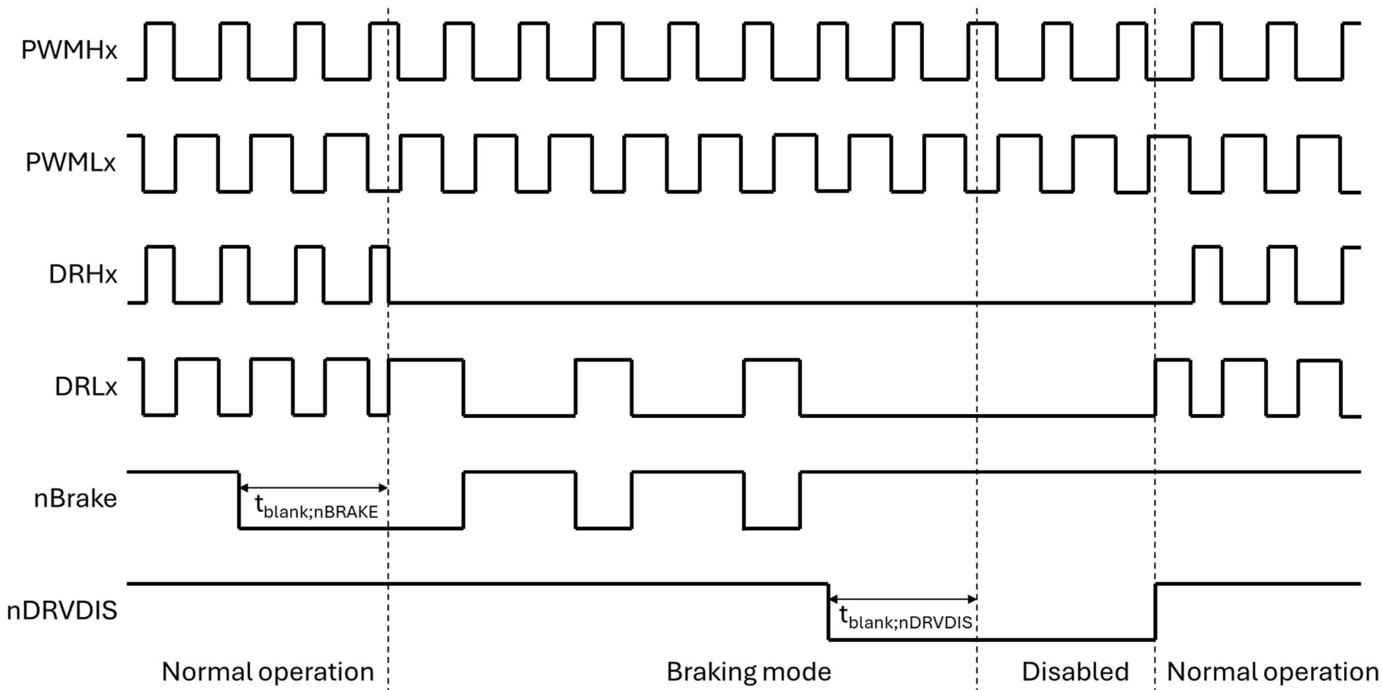

Fig. 4-1. Braking mode operation

Fig. 4-1 shows the timing of entering and exiting braking mode. Braking mode ends after nDRVDIS is asserted (driven low) for at least the blanking time, which is 80 µs maximum. After the blanking time, with nDRVDIS asserted, the PWM and nBRAKE signals are ignored as previously described. Only after nDRVDIS is subsequently de-asserted can normal PWM operation resume. Firmware in the PAC5xxxx cannot enable or disable the gate drivers.

5. Power Management

MCDs integrate optimized power management that power the MCD from a variety of input power sources. Dedicated multimode switching supply (MMSS) controllers operate as a buck, SEPIC or AC/DC flyback converter. Linear regulators provide the required internal voltages. The power manager also handles system functions including internal reference generation, timers, hibernate mode management, and power and temperature monitoring.

Table 2-1 indicates the type of power manager included in the MCD. PAC5x56 allows AC input, meaning rectified 120 to 240 VAC can connect directly to the HV buck input. This is because the PAC5x56 maximum input voltage is 605 V. The PAC5x56, PAC5x32, and ACT72350 have a high-voltage buck and a medium-voltage buck. HV buck uses external MOSFET, diode, inductor, and a bootstrap to power the internal high-side gate driver. MV buck has internal buck MOSFET and diode and requires no bootstrap; it requires only an external inductor and usual capacitors. Circuit examples are included in corresponding datasheets, user guides, and EVKs.

Many PACs support buck or SEPIC as the power source converter. SEPIC means Single-Ended Primary-Inductor Converter. The SEPIC input and output voltages can overlap and have the same polarity. A SEPIC uses a series capacitor to transfer energy from its input to output, allowing graceful short circuit response. Another advantage is its output current drops to zero after the SEPIC shuts down (stops switching). This helps minimize hibernation mode leakage current. Control of a SEPIC can be tricky with two inductors and two capacitors affecting its transfer characteristics. This, however, is handled by the MMPM in the PAC, including feedback compensation.

The buck converter (not HV or MV) needs further explanation. The DC input to the buck converter connects through a resistor from the battery pack to VHM pin, which connects internally to a clamp that is enabled or disabled by firmware. The clamp limits the high-side gate driver supply to about 15 V above VSS.

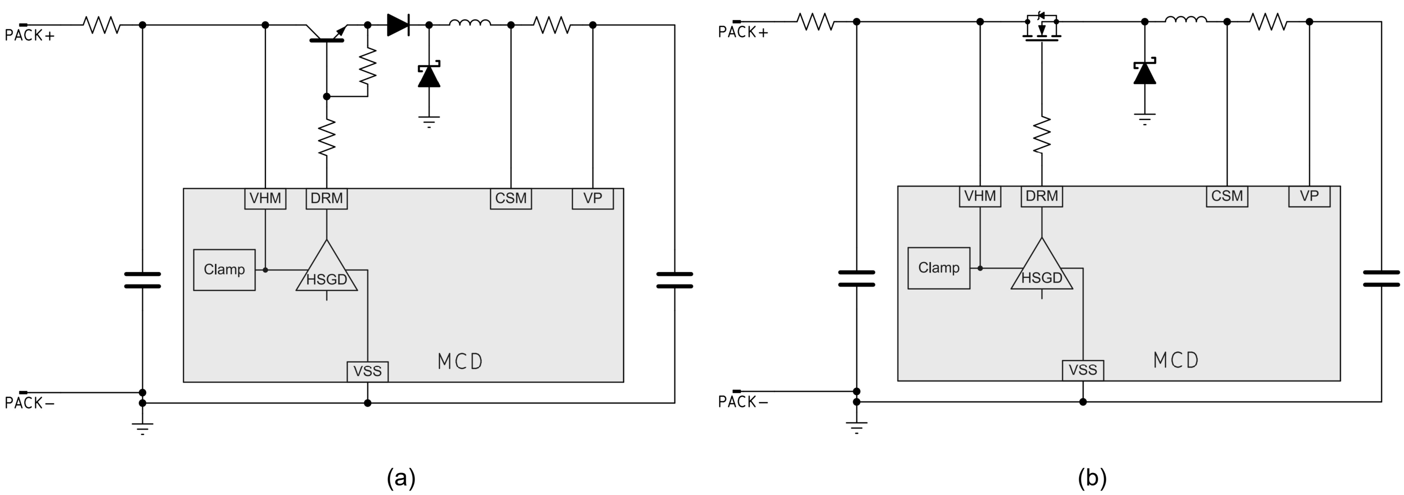

Fig. 5-1. Buck converter (a) using external NPN transistor, and (b) using external MOSFET

Fig. 5-1(a) shows a buck converter using an NPN transistor as the switch (plus emitter protection diode). The low drive voltage required by the NPN allows VHM to be lower than for the external MOSFET implementation in Fig. 5-1(b).

MCDs with AC-DC flyback input option include an "ultra-high-voltage buck mode" with an NPN transistor driving a P-channel MOSFET in Darlington configuration. See corresponding datasheets for details.

For other power supply configurations, please refer to Table 2-1 and corresponding datasheets, user guides, and EVKs.

6. Processing

PAC52xxx motor controllers contain a 50 MHz Arm® Cortex®-M0 32-bit microcontroller core with 32 KB of embedded FLASH and 8 KB of SRAM. PAC55xxx motor controllers contain a 150 MHz Arm® Cortex®-M4F 32-bit microcontroller core with floating point unit (FPU), 128 KB of FLASH, and 32 KB of SRAM. They all contain peripherals, including pulse width modulation (PWM) and other timers, analog to digital converters (ADC) with associated state machine, various serial communications, and security.

Each MCD has an industry leading low-power mode called sleep or hibernate mode. This important feature keeps a battery pack ready for use with full charge even after months of storage. The MCD exits sleep mode after a wakeup timer count expires or after a push button event (if enabled).

7. Communication

There are multiple options for PAC intelligent motor controllers to communicate with other ICs or externally. Table 7-1 lists communication peripherals included in each Qorvo PAC MCD. Note that SWD is used for both debugging and programming. JTAG can also be used for programming if included.

Table 7-1. Communication and debug/program interfaces by device type

Series	Communication and Debug Peripherals	Notes
PAC52xxx	• SPI • I2C • UART • SWD	• UART means serial port. • SWD is Serial Wire Debug, also called Single Wire Debug although it uses data and clock signals.

PAC55xxx	• 3 x USART (Either SPI or UART)
	  ○ SPI Master/Slave up to 25 MHz
	  ○ UART up to 1 Mbps
	• I2C/SMBus Master/Slave
	• CAN 2.0B Controller
	• SWD
	• JTAG
	• Embedded Trace Macrocell (ETM)
		• PAC5532x has 2 USARTs instead of 3.
		• SMBus is a variant of I2C.
		• JTAG (Joint Test Action Group) is also known as boundary scan and is covered by IEEE 1149.x standards.

8. Application Specific Power Drivers

Qorvo PAC5xxx series and the integrated three-phase driver ACT72350 all have at least six internal gate drivers to support a triple half-bridge arrangement. The following part numbers have two additional open-drain drivers for relays, LEDs, buffers, and other loads: PAC5210, PAC5250, PAC5253, and PAC5255 (see Table 2-1). PAC5253 and PAC5255 have 4 and 6 low-side gate drivers respectively, and each have 3 high-side gate drivers.

Revision History

Revision	Author	Date	Description
A	Jonathan Dodge, P.E.	12 Sept. 2025	Initial draft

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: +1 844-890-8163

Email: customer.support@qorvo.com

Important Notices