Outdoor Power Equipment Design Guide

Abstract

This document outlines Qorvo's Power Application Controller® (PAC) battery management and intelligent motor controller & drive solutions for higher voltage battery powered outdoor equipment, including lawnmower, string trimmer, chainsaw, leaf blower, hedge trimmer, etc. It reviews the design requirements of outdoor power equipment and introduces specific solutions based on Qorvo's battery management and intelligent motor controller products. Detailed design examples for battery management and motor control provide guidance and step-by-step instructions. Further implementation details are contained in corresponding product-specific datasheets, application notes, user guides, and evaluation kits.

1. Introduction

The performance of lithium-based batteries enables many new applications, especially outdoor power equipment, high power tools, e-bikes, and scooters. Thanks to increasing energy density (light weight) coupled with the capability to deliver high power, battery powered lawn and garden tools are steadily replacing noisy gasoline powered counterparts, eliminating the need for homeowners to fill and store volatile gasoline in containers. To satisfy the demand for ever higher power and longer run times, battery pack voltage and capacity is steadily increasing. This rapidly expanding industry is however struggling with battery cell variability and durability. High energy density and small form factors make safety the overriding design priority. This application note introduces Qorvo PAC battery management systems and intelligent motor controllers that greatly extend battery service life and facilitate outdoor power tool certification. Two detailed design examples cover many aspects of system design including circuit protection, gate drive, and power management.

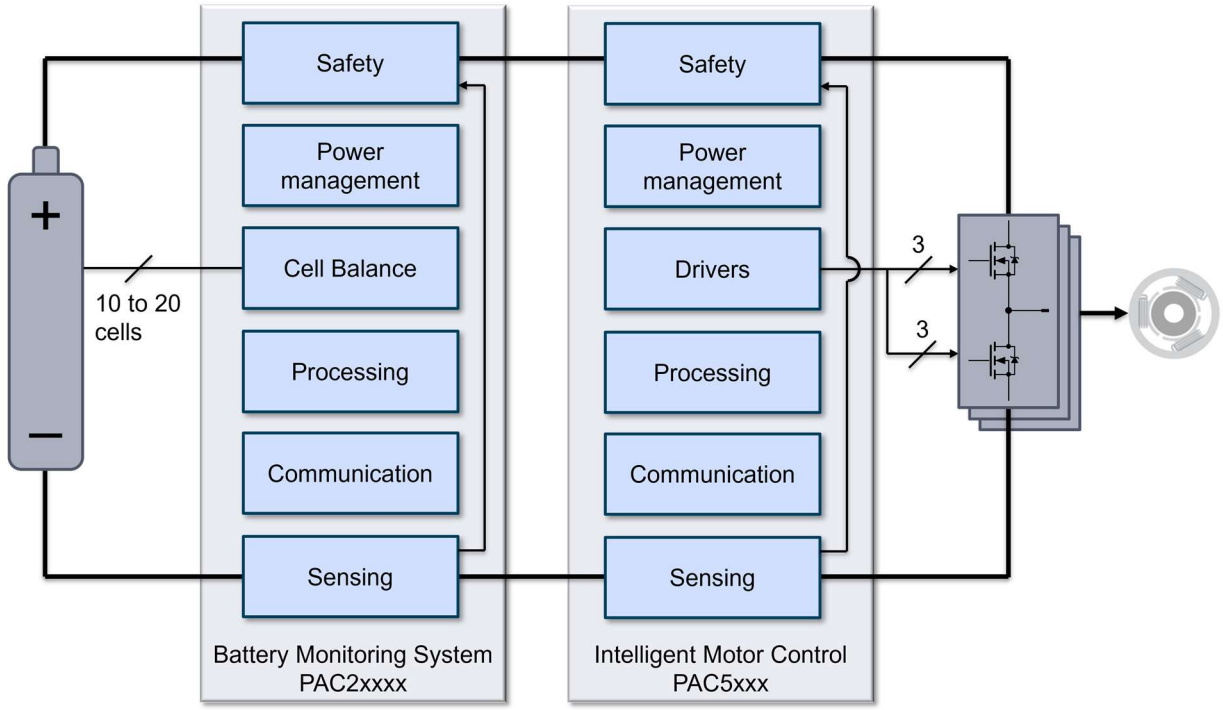


Fig. 1-1. Battery powered equipment system

Fig. 1-1 shows a battery powered equipment system block diagram. The battery is comprised of cells connected in series. Qorvo PAC battery management systems (BMS) are configurable and support a wide cell voltage range and can work with any battery chemistry.

PAC motor control and drive (MCD) solutions directly drive the gates of power transistors in half-bridge, full-bridge, or 3-phase bridge configurations. Battery pack and BMS functions are described first along with a design example, then MCD functions and design example.

2. Battery Pack Construction

The battery pack defines the performance of outdoor power equipment. Several battery cells are series-connected to achieve the desired battery pack voltage. Meeting the demand for high power requires high series cell count, designated with suffix S. Common battery pack configurations range from 10S to 20S corresponding to nominal voltages of 32 to 80 V depending on chemistry. Typical battery chemistry for power tools is lithium manganese oxide (LMO) or lithium nickel manganese cobalt (NMC) because their higher cell voltage allows fewer cells and hence lighter weight.

With higher cell count comes increasing risk of cell voltage mismatch, which corresponds to cell charge mismatch. Cells with lower-than-average voltage not only degrade battery pack performance, but cells with higher voltage could overcharge, which is extremely hazardous for lithium-based batteries. Preventing charge imbalance requires intelligence within the battery pack.

One approach is for the charger to check for cell voltage imbalance, and if out of range, to simply refuse to charge the battery pack. Battery cycles are sometimes extremely limited with this approach, causing frustration among outdoor equipment customers as they reluctantly switch back to gasoline-powered tools rather than risk more money on unreliable battery packs.

Active cell balancing on the other hand greatly extends battery service life. Methods exist to shuttle energy from higher to lower voltage cells through a matrix of power interconnections and one or more DC-DC converters. A much simpler solution is to alternately partially discharge energy in higher voltage cells, with heat dissipated in power transistors and resistors. This is the approach taken in Qorvo's Power Application Controller® (PAC) series of battery management systems.

3. PAC Overview

Qorvo PAC battery management and motor controller systems are highly integrated. The PAC system-on-chip platform integrates either a 50 MHz Arm® Cortex®-M0 or 150 MHz Arm Cortex-M4F microcontroller core, power management, gate drive, and signal conditioning in a single, small package. This saves cost and space but also reduces design risk and time. Each function is fully tuned and qualified. The bill of material is greatly simplified, which improves reliability and reduces manufacturing risk. Qorvo can provide UL / IEC IEC60730 Class B pre-certified firmware to facilitate system-level certification. Application notes [1] and [2] explain the various part numbers and functions of PAC BMS and intelligent motor control & drive solutions.

4. Design Example

4.1. Overview

This example is for motorized equipment powered with a 52 V nominal battery pack made with 14 series connected Nickel-Manganese-Cobalt (NMC) battery cells. The equipment could be anything, including a lawnmower, string trimmer, chainsaw, leaf blower, e-bike, e-scooter, etc. Let us say it is a lawnmower with a peak power requirement of 1500 W. The battery pack requires a PAC BMS with cell balancing due to the number of series cells.

Side note: 16S LiFePO4 (LFP) is a typical energy storage system battery setup that would have about the same voltage as 14S NMC. Higher LFP cell count makes it slightly bulkier and heavier than NMC, so LFP is less attractive in handheld tools. However, LFP has the longest cycle life, lower cost, and avoids mining issues with cobalt and nickel.

It is necessary to know the battery characteristics to set appropriate limits. Batteries are rated by Amp hours (Amps integrated over time with unit symbol Ah) at a specified discharge rate or duration. The charge or discharge rate is normalized to the Amp hours with the letter C next to the number and is generally less than the Amp hour number. For example, charging a 40 Ah battery at 10 A would be a 0.25C charge rate.

Assuming the battery temperature is kept above freezing, which is necessary for recharging many lithium-based batteries, battery voltage changes slightly with temperature. Battery temperature effects on state of charge (SoC) are therefore ignored in this design example.

The battery voltage changes significantly based on charge or discharge current. For this reason, accurate Coulomb counting (integrating battery current over time to keep track of Amp hours) is required.

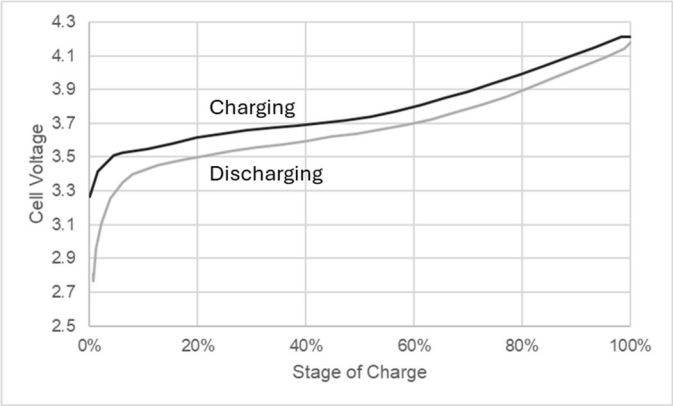


Fig. 4-1. NMC battery cell voltage versus state of charge at 0.25C rate, 25 °C

The chart in Fig. 4-1 shows two curves, one for charging and the other for discharging an NMC battery cell at 0.25C rate and 25 °C. The nominal cell voltage is 3.7 V discharging at about 60% SoC based on the curves in Fig. 4-1, corresponding to 52 V nominal battery pack voltage. Note the gradual change in voltage between about 15% to 50% SoC, and the steep reduction in voltage below about 10% SoC. We set the charge voltage at 4.2 V maximum and discharge voltage at 3.2 V minimum per cell, or a total of 58.8 and 44.8 V respectively. The automatic over- undervoltage shutdown thresholds should have some margin beyond these. Firmware should disconnect the charger or the load before these thresholds are reached; these activate automatically in case firmware fails to.

Maximum continuous output power is 1500 W with battery pack voltage above 48 V. Assuming about 90% overall efficiency, the maximum continuous battery current is 35 A. When the battery pack voltage is below 48 V, its state of charge is low, and power derates by limiting the current to 35 A.

4.2. PAC Battery Management Solution

Each Qorvo PAC BMS does the following:

- Measure all cell voltages and current
- Precisely measure battery and internal temperatures
- Automatically interrupt battery current in emergency conditions
- Function as a battery disconnect when not in use
- Actively balance cells with transistors and resistors

The BMS is part of the battery pack. PAC25140 is an excellent choice with plenty of FLASH and SRAM for the MCU plus it includes a floating-point unit that greatly simplifies programming. We work through the design by function block, beginning with power management.

4.2.1. Power Management

The built-in buck converter works well for the PAC25140 power supply. The default buck switching frequency is 100 kHz. See the PAC2514x User Guide for other buck switching frequency options. Power management and battery disconnect designs are shown in Fig. 4-2.

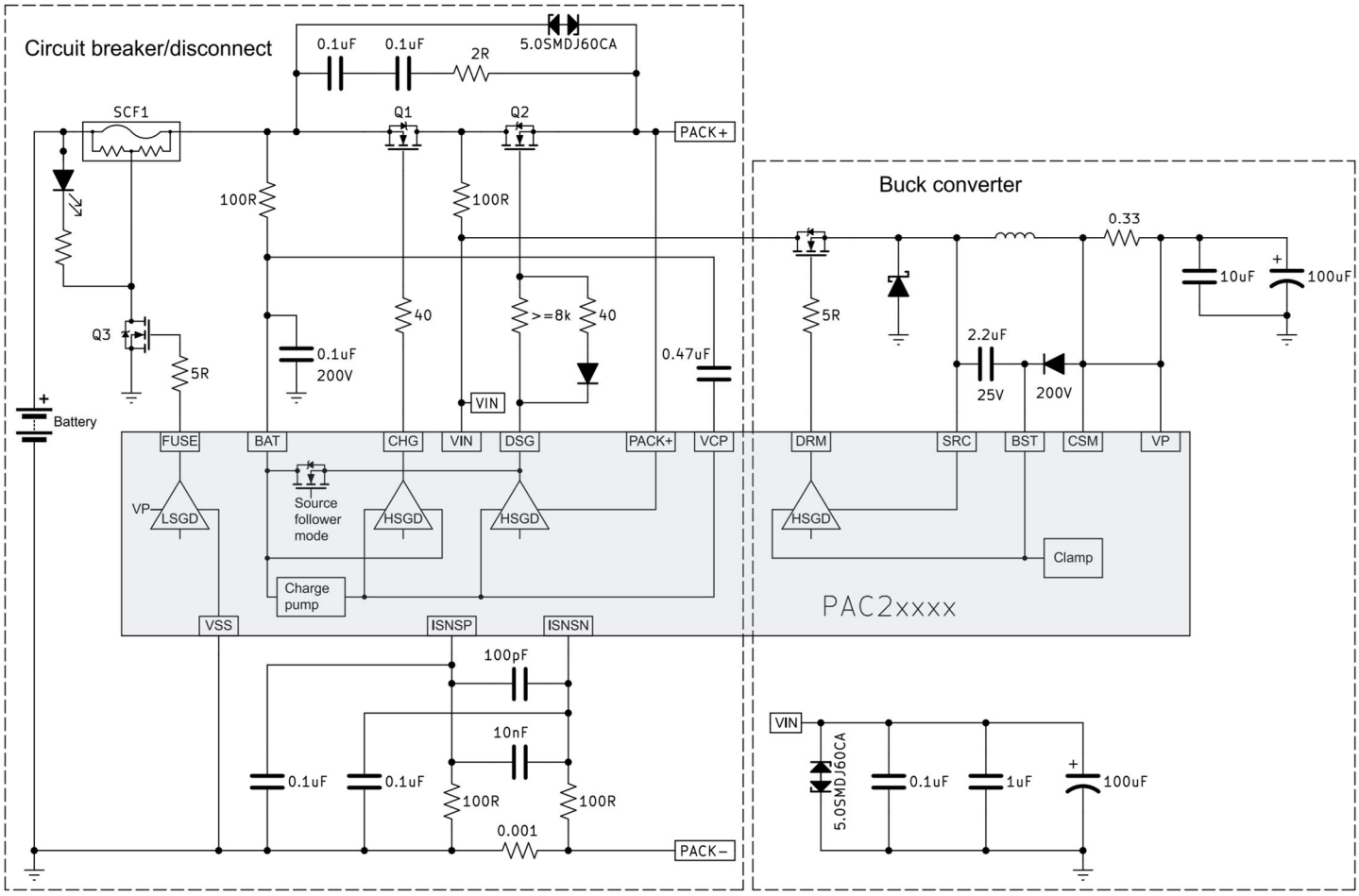


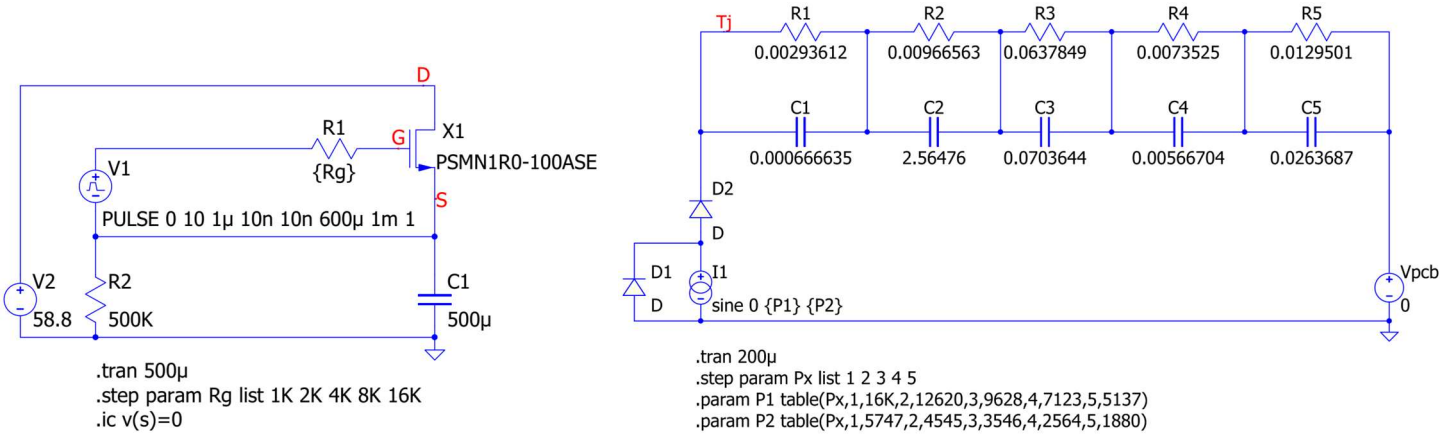
Fig. 4-2. PAC25140 battery disconnect and power management simplified schematic

4.2.2. Battery Circuit Breaker / Disconnect

This design example deviates from the EVK in the selection and configuration of the battery disconnect / breaker MOSFETs, and there is an important addition to the snubber. It is desirable to switch on slowly to limit inrush current, deliberately spending time in active mode (commonly called linear mode). Active mode is where MOSFET drain current depends more on V_{GS} than V_{DS}. High V_{DS} causes high power dissipation in active mode, which is desirable because it reduces the inrush into the tool capacitor bank. Parallel MOSFETs in active mode can have significant current mismatch due to differences in threshold voltage $V_{GS(th)}$. The effectiveness of paralleling to achieve high power dissipation capability is unpredictable without some way to improve current sharing, such as series resistors, which are too lossy in a breaker / disconnect, or individual gate feedback control, which is complex. Ideally, we avoid paralleling the MOSFETs. This is possible with a low $R_{DS(on)}$ MOSFET with high power dissipation capability and sufficient safe operating area (SOA) in active mode. Such a MOSFET is part number PSMN1R0-100ASE from Nexperia, which was designed for this type of application.

Worst case conduction loss is $\left(\frac{1500\ W}{48\ V}\right)^2 \cdot 2\ m\Omega = 1.95\ W$. This calculation uses roughly 2x the maximum 25 °C $R_{DS(on)}$ to account for the temperature effect on $R_{DS(on)}$, which is worst case. A single part can easily dissipate 2 W on a typical circuit board, so there is no need to parallel based on conduction loss.

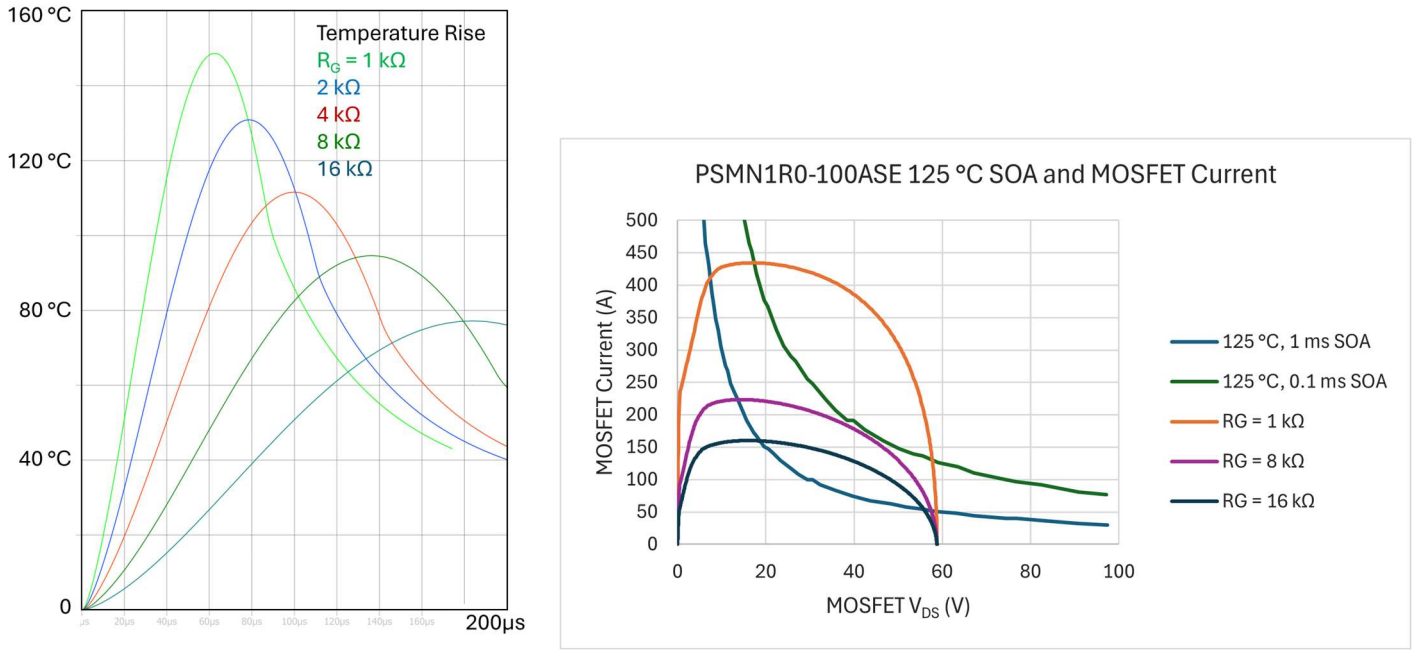
Any MOSFET is most vulnerable in active mode (partially on) at high voltage, high power dissipation due to a self-reinforcing hot spot (current filamentation) effect. This effect is reduced by design in the PSMN1R0-100ASE, with somewhat lower gain and slightly higher $R_{DS(on)}$ traded for significantly wider SOA. The SOA chart in the MOSFET datasheet provides guidance for the mounting base at 25 and 125 °C. Also, a very useful tool is transient thermal simulation. Nexperia provides SPICE models and Foster and Cauer thermal impedance models. Fig. 4-3 (a) shows a simple simulation circuit with various gate resistances, and (b) shows a Foster transient thermal impedance model with power dissipation in the MOSFET modeled as part of a sine wave, which is accurate enough.



(a) (b)

Fig. 4-3. (a) Foster thermal model of PSMN1R-100ASE MOSFET, (b) simulation results for charging a 500 µF capacitor bank

Note that Foster and Cauer thermal models do not represent physical layers in the MOSFET. They are simply the result of curve fitting to thermal impedance test data.

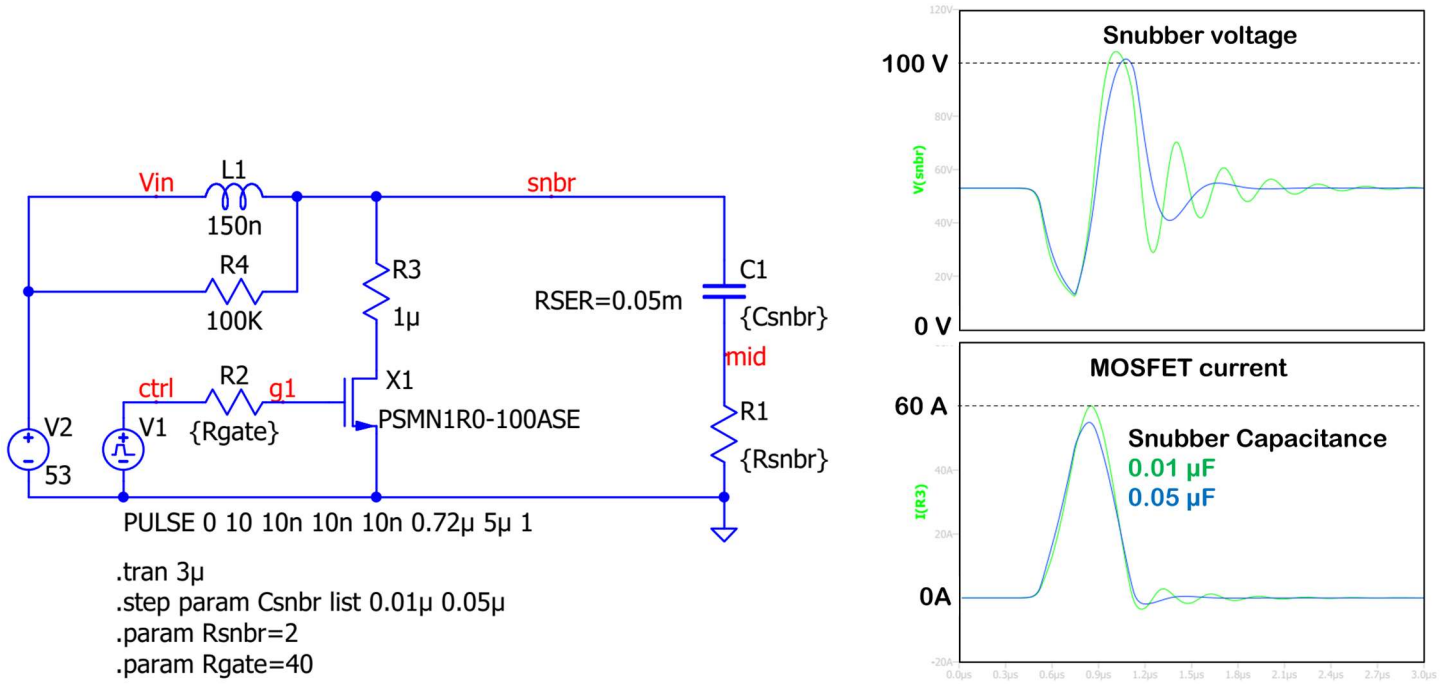


(a) (b)

Fig. 4-4. (a) MOSFET temperature rise with various R_G values , (b) PSMN1R0-100ASE SOA with MOSFET current superimposed

Fig. 4-4(a) shows simulation results from the circuit in Fig. 4-3(a). The curves represent MOSFET junction temperature increase versus time with various gate resistance values. Fig. 4-4(b) shows simulated MOSFET current with various R_G values superimposed upon PSMN1R-100ASE 125 °C SOA curves with pulse durations of 100 µs and 1 ms. The gate resistance needed to sufficiently slow MOSFET switch-on is huge, which is acceptable only for switch-on. Such high switch-off gate resistance would cause excessive delay and slow switch-off during an emergency. The gate steering diode in Fig. 4-2 allows a lower switch-off gate resistance. The simulated peak temperature rise is 95 °C and 77 °C with gate resistance of 8 kΩ and 16 kΩ respectively. The current curve in Fig. 4-4(b) corresponding to R_G = 8 kΩ is just under the 100 µs SOA curve. Based on these simulations, a single MOSFET (not paralleled) with gate resistance of at least 8 kΩ could safely limit the tool's capacitor charge inrush current. It merits further investigation and testing in a real application.

A snubber across the breaker MOSFETs is strongly recommended. It damps ringing during normal switching, and it helps clamp peak voltage during emergency switching. The snubber design begins with worst case analysis. The breaker must switch off safely with a shorted load (short in the tool). For the breaker MOSFETs, this is effectively unclamped inductive switching with inductive energy stored in the battery pack itself and interconnections between the battery pack the load. This energy must be dissipated as the breaker switches off. The inductance is reasonably low due to short interconnections. Let us assume it is 150 nH. If we set the automatic overcurrent trip above 53 A (1.5 · 35 A), the energy that must be dissipated is $0.5 \cdot 150\,nH \cdot 53\,A^2 = 0.21\,mJ$. We will add plenty of design margin to this.



(a) (b)

Fig. 4-5. Snubber simulation wtih Rsn = 2 Ω and Csn sweep (a) simulation circuit, (b) results

A simple way to think of an RC snubber is as follows. The goal is to achieve acceptable voltage overshoot and ringing while minimizing both capacitance and resistance. The snubber capacitance adds to the MOSFET output capacitance and reduces the switching voltage slew rate. The snubber resistance provides damping to reduce ringing. This is an oversimplification, but it helps to start the design. Excessively increasing capacitance has diminishing benefits. Too much resistance restricts current through the capacitor(s). It is helpful to start with a small snubber resistance, then adjust the capacitance, and finally re-adjust the resistance.

A QSPICE simulation helps to better understand the snubber circuit, even though it cannot fully represent the real circuit. Fig. 4-5(a) shows an RC snubber across a MOSFET. The result of switching the MOSFET on and then off again is shown in (b). A snubber capacitance of 0.05 µF results in acceptable voltage overshoot. Not shown is the effect of snubber resistance. There is excessive ringing without a snubber resistor, and best simulation result is with Rsn = 2 Ω, so this is a good starting point for testing.

Full voltage can appear across the snubber resistor and capacitor, so voltage rating and clearances for each must be considered. Therefore, they must be in at least 0805 package size, or larger such as 1206. Two example part numbers (of many) for the 2 Ω resistor are CRCW12062R00FKEAHP or RCS08052R00FKEA, both made by Vishay. These are pulse rated, which is a requirement for snubber resistors. A common option for the snubber capacitors is to use two in series to reduce the voltage across each and the clearance requirements. An example part number is 885342208002, made by Würth Elektronik. Two of these in series yield the desired 0.05 µF snubber capacitance.

There is a small tradeoff circle between MOSFET BV, PAC2xxxx maximum voltage, and peak voltage during emergency switch-off. A transient voltage suppressor (TVS) diode has about 2:1 ratio between maximum clamp and operating voltages according to commonly used 8 / 20 µs current surge curve. The difference is somewhat greater for Metal Oxide Varistors (MOV). A bidirectional TVS that could work (among others) is 5.0SMDJ60CA. This would of course connect across the two breaker MOSFETs, in parallel with the RC

snubber. It would at least prevent a peak voltage from exceeding the PAC2xxxx maximum voltage of 145 V, even though the MOSFET could avalanche, depending on the current surge waveform and actual BV of the MOSFET. The same type TVS optionally connects between VIN and battery negative (ground), as shown in Fig. 4-2, mounted close to the BMS. Choosing a MOSFET with higher BV means higher $R_{DS(on)}$, and the PAC2xxx cannot increase its maximum voltage anyway. A viable option is to simply let the MOSFET act as the voltage suppressor, if its maximum BV is always less than the PAC2xxxx maximum of 145 V. The selected MOSFET is fully characterized for avalanche and can handle thousands of times more than the previously estimated stored energy of 0.21 mJ.

A self control fuse (SCF), such as the one labelled SCF1 in Fig. 4-2 provides two-in-one protection. First, it is a fuse, and it will blow if an abnormally high current persists too long. Second, when the fuse MOSFET, Q3 in Fig. 4-2, switches on, current flows through a heater in the SCF, causing the SCF fuse to quickly blow. Switching the fuse MOSFET requires MCU code, such as a battery overvoltage fault interrupt service routine. The Eaton SCF9550-45-14 is rated at 45 A. This SCF is the largest in its series, and its current rating has 29% margin from the maximum continuous battery current of 35 A. The SCF is not resettable, so if it blows, the battery pack is not usable until the SCF is replaced. This author considers 29% margin to be insufficient, preferring at least 50% and up to 100% fuse margin, especially considering necessary margin for overcurrent detection and shutdown by firmware, and even higher margin for comparator tripped shutdown, without risking false trips. A fast-acting fuse with more margin could be used instead of the SCF. If the system design omits the SCF, then the PAC's FUSE output can perform another function such as driving an LED or relay. Just for completeness, the SCF9550-45-14 has a heater resistance of 38.5 to 75.0 Ω, corresponding to a maximum heater current of $\frac{58.8\ V}{38.5\ \Omega} = 1.5\ A$. A small MOSFET can handle this.

4.2.3. Cell Balancing

Balancing cells *greatly* extends battery service life, yields longer runtime, and increases safety.

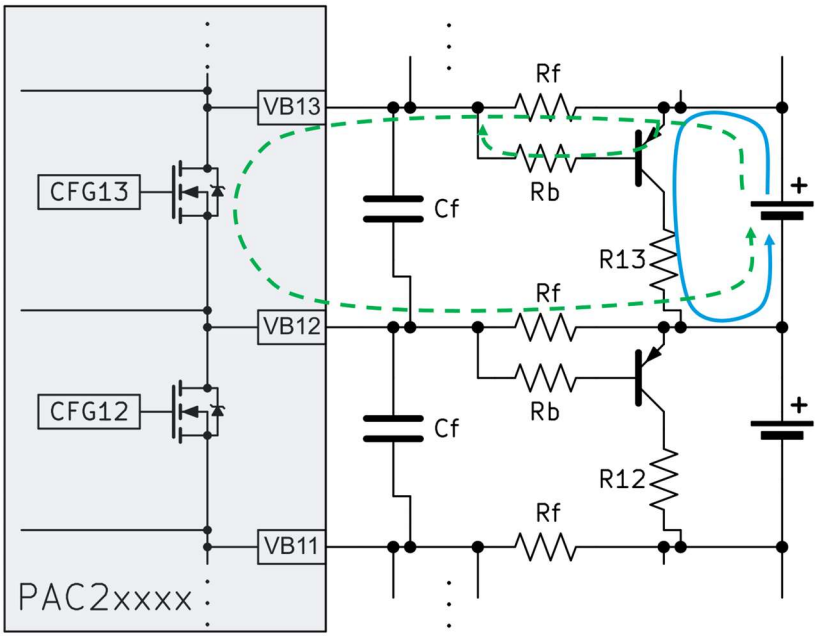
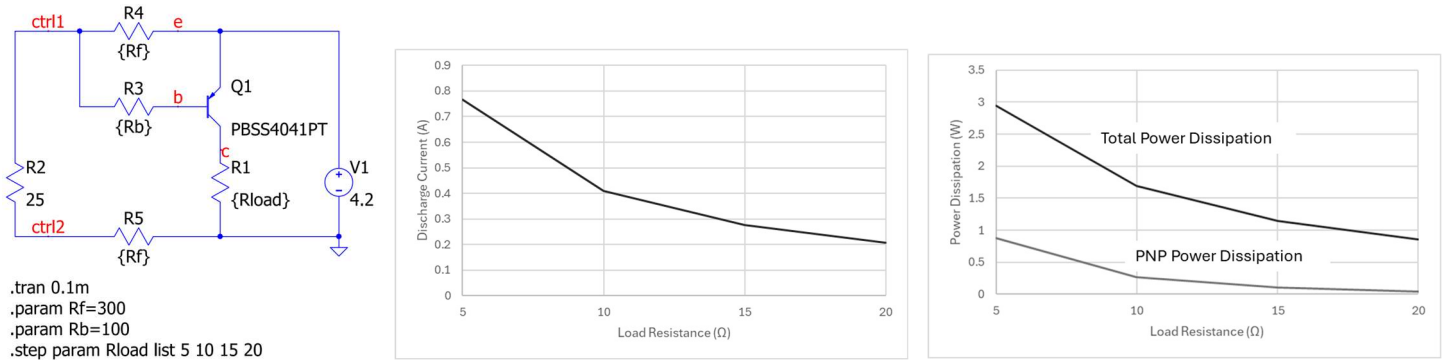


Fig. 4-6. PAC2xxxx BMS cell balancing with external transistors

Each PAC2xxxx BMS can balance cell voltages with internal 25 Ω FETs that support up to 50 mA, limited by internal heating. However, outdoor tools usually require higher balance current, so the internal FETs control external transistors and load resistors capable of hundreds of milliamps. One implementation is shown in Fig. 4-6 where an internal FET biases a PNP transistor on with a voltage drop across resistors Rf. Much higher current flows through the PNP and load resistor to partially discharge a higher voltage cell, which could be anywhere in the battery pack. This balancing process is programmable, so it can happen anytime, but it is typically done while charging to maximize run time.

When an internal balancing FET is on, current flows through the filter resistors Rf, PNP base, internal 25 Ω FET, and the battery cell being discharged, as indicated by the dashed arrow in Fig. 4-6. This outer loop current is mostly determined by Rf. Increasing Rf decreases outer loop current, which is desirable, but it decreases the PNP transistor's base current, and it creates a longer time

constant with filter capacitance Cf, requiring longer settling time before making cell voltage measurements. Diminishing returns limits Rf to 500 Ω maximum.



(a) (b) (c)

Fig. 4-7. (a) Cell discharge simulation circuit, (b) current in load resistor, (c) dissipation in PNP and total (PNP plus resistor)

A QSPICE simulation helps to predict balancing circuit conditions. Fig. 4-7(a) shows a simulation schematic of a cell discharge circuit from Fig. 4-6, where R2 represents an internal 25 Ω FET, and V1 is a fully charged battery cell. The filter resistors Rf (R4 and R5) and the PNP transistor's base resistor R3 each have a fixed 200 Ω value. The load resistance R1 is stepped with four values: 5, 10, 15, and 20 Ω. The PNP transistor X1 is part number PBSS4041PT from Nexperia, a 60 V, 2.7 A PNP in SOT-23 package. Fig. 4-7(b) shows load current at various resistance values, and (c) shows power dissipation in the PNP transistor as well as total power dissipation (PNP plus load resistor). A 200 Ω filter resistance is sufficient to bias the PNP transistor on, but with R1 = 5 Ω, the PNP V_{CE} increases significantly because of higher load current. To operate with R1 = 5 Ω, the base resistance would probably need to decrease from 200 Ω to about 100 Ω. Note that at higher discharge current, characteristics of the PNP transistor govern the circuit operation.

With R1 = 10 Ω, and Rf and Rb = 200 Ω, outer loop current is almost 12 mA, resulting in 3.5 mW in the internal FET. According to the simulation, dissipation in the PBSS4041PT transistor is 37 mW, resulting in a junction-to-ambient temperature rise of about 7 °C with standard layout on a 4-layer circuit board. Current through the battery cell is about 0.41 A, corresponding to 1.7 W from the cell. Power dissipation in the load resistor is also 1.7 W. For continuous use, a dissipation margin factor ≥ 5 is recommended for power resistors, which is arguably conservative. The margin requirement is substantially reduced by alternately discharging cells for a short time, greatly reducing the average dissipation in each load resistor. Application note [3] shows examples.

Balancing cell voltages requires highly precise voltage measurements, and for this reason, each PAC2xxx BMS includes a 16-bit analog-to-digital converter (ADC) dedicated to cell voltage measurement, and safety checks of DAC outputs for short circuit and battery overvoltage protection.

4.2.4. Battery Current Sense

Battery current measurement requires high precision to enable Coulomb counting for battery gauge and service life calculations. A second 16-bit ADC serves this purpose, plus safety checks of DAC outputs for overcurrent protection while charging and discharging. A dedicated precision, programmable-gain differential amplifier senses voltage across an external current sense resistor. The output of this amplifier is multiplexed to the 16-bit current sense ADC and to overcurrent charge and discharge comparators. The differential current sense amplifier gain DA_{GAIN} is programmable to be 1, 2, 4, 8, 16, 32, 64, or 128. The differential input voltage V_{ISENSE} multiplied by DA_{GAIN} is the amplifier's output, which must remain within a range of ±0.3 V to ensure accurate ADC conversion.

The value of the current sense resistor R_{sense} is determined by balancing the tradeoff between accuracy and power dissipation. The amplifier output voltage range limit of ±0.3 V limits R_{sense} to 8.6 mΩ maximum, but power dissipation at maximum continuous current of 35 A would be quite excessive, over 10 W. The lower limit for R_{sense} is 67 µΩ, but noise would overwhelm the signals. Full scale V_{ISENSE} should significantly exceed the amplifier input offset voltage, which is ±8 mV. A good compromise at this power level is a current sense resistor in a 2512 or larger surface mount package. Part number PSR100KTQFH1L00 by ROHM Semiconductor is a 1 mΩ, 8 W, 1% current sense resistor in 2512 package. This would work with DA_{GAIN} = 8, full scale voltage of ±35 mV, and power loss at 35 A would be 1.2 W. Several 6 W, resistors could also work, such as Isabellenhuette BVT-M-R001-1.0. With R_{sense} = 0.5 mΩ, there is a wide selection of 2512 package resistors, some up to 10 W rated dissipation. Gain setting DA_{GAIN} would be 16. A calibration step should be performed

after final assembly to achieve the best accuracy. The bulk of the remaining design work is configuring the PAC25140. Information for that is found in the PAC2514x User Guide.

4.3. Motor Controller Solution

The recommended maximum battery voltage is two-thirds of absolute maximum voltage rating, unless using a transient voltage suppression method. For example, the PAC5532B maximum voltage is 160 V, so it could operate with a maximum battery voltage of 0.67 · 160 V = 107 V. This is well above the maximum battery voltage in this design example, so the PAC5532B is a good choice, taking advantage of the M4F MCU core with floating point. Each PAC5xxx intelligent motor controller has an EVK with documentation that covers implementation details. Some of the main points are presented here.

4.3.1. Power Management

The PAC5532B input voltage range is 25 to 160 V DC, so its built-in buck converter works well for the power supply. The configurable buck switching frequency range is 50 to 400 kHz. The motor controller buck converter design is same as the BMS buck shown in Fig. 4-2. The datasheet specifies 100 µH for the inductor, same as the BMS. An optional TVS connects between VM, buck converter input pin (VIN in Fig. 4-2), and PACK-. The same TVS can be used as for the BMS, such as 5.0SMDJ60CA.

4.3.2. Power MOSFETs

The lawnmower of our design example must be capable of operating at 1500 W continuously down to 48 V battery voltage. The phase current remains to be determined. The motor drive is effectively a buck converter, stepping down the DC link voltage and thus delivering higher current. The phase current could be arbitrarily high unless limited. Let us say the maximum allowed phase current is 2.5 times the full power current with the motor at full speed and modulation index of 0.9. This 2.5x overload factor is to provide starting or peak torque for a limited duration. The modulation index is defined as $m = \frac{v_{LN,pk}}{V_{DC}/_2} = \frac{2 \cdot \sqrt{2} \cdot v_{LN,rms}}{V_{DC}}$. Solving for $v_{LN,rms}$: $v_{LN,rms} = \frac{m \cdot V_{DC}}{2 \cdot \sqrt{2}}$. With m = 0.9, $v_{LN,rms} = \frac{0.9 \cdot 48}{2 \cdot \sqrt{2}} = 15.3\ V\ rms$, and the phase current is $i_{ph,rms} = \frac{P_{ph}}{v_{LN,rms}} = \frac{1500\ W/_3}{15.3\ Vrms} = 32.7\ A\ rms$. Maximum allowed motor current is 32.7 · 2.5 = 82 A rms.

A power semiconductor chip saturates thermally after roughly 10 µs, and a discrete package after roughly 10 ms. After that, the capacity of the heatsink becomes relevant. The motor needs much longer than 10 ms to start spinning, so electronically speaking, we must design the MOSFET drive as if the overload condition were permanent.

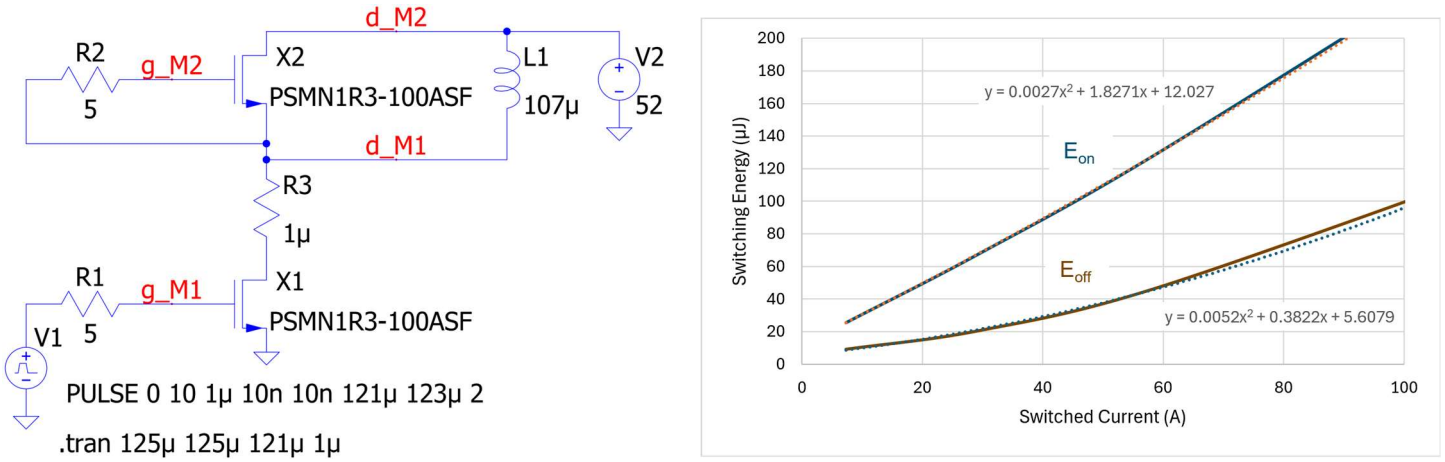
Having determined the maximum current, the next step is to choose the voltage rating. Best practice for reliability dictates a ratio of about 0.67 applied versus rated voltage. A 100 V rating is sufficient. Top-side cooling is an attractive option, but this simple design uses surface mount discrete MOSFETs. The next question is whether paralleling is required.

Three promising MOSFETs to consider (among others) are PSMN2R0-100SSF, PSMN1R3-100ASF, and PSMN1R0-100ASF from Nexperia. These are all standard threshold MOSFETs that would work well with 0 V for switch-off, as is the case with an integrated MCD. To help estimate the power loss in each MOSFET, an inductive switching QSPICE simulation shown in Fig. 4-8(a) uses the SPICE models for PSMN1R3-100ASF and PSMN1R0-100ASF. The SPICE model for PSMN2R0-100SSF is encrypted, so the QSPICE model generator utility created a model for it, see Appendix. The result of the double-pulse simulations is switching energy versus current curves as shown in (b). A power loss calculator [4] uses curve fit coefficients from the switching energy data. Such a calculator allows rapid comparison of different parts and operating conditions.

Technical Tips: Accuracy of a power loss calculator as described in [4] is quite good but not perfect. It is very useful to identify trends and choose configurations that merit further investigation and ignore infeasible ones. If power dissipation in an air-cooled switch-mode surface mount power transistor is more than a few Watts, and if there is sufficient space, it is best instead to parallel power transistors and spread them out as much as possible on the circuit board. This is true even if the paralleled MOSFETs have higher $R_{DS(on)}$.

Calculations were made with the following conditions:

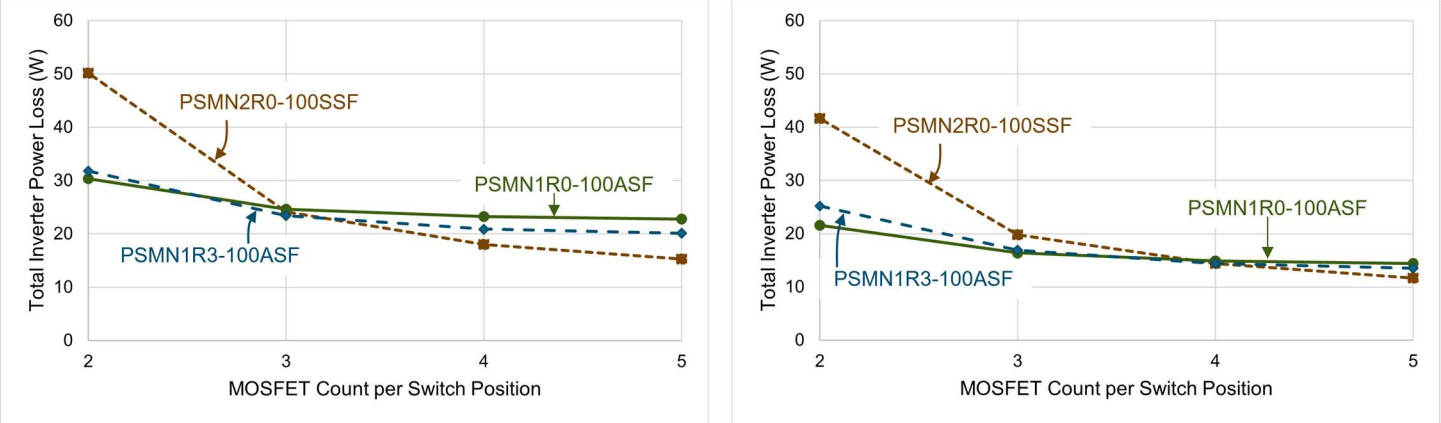
- Power = 1500 W
- V_{bus} = 48 V
- I_{phase} = 82 A RMS
- V_{LN} = 6.1 V RMS with modulation index = 0.36
- Switching frequency = 20 kHz



(a) (b)

Fig. 4-8. Switching simulation (a) QSPICE schematic, (b) switching energy results

Results with space vector modulation (SVM) are shown in Fig. 4-9(a), and with 60° discontinuous modulation (DPWM1) in (b). See [5], [6], and [7] for modulation method details.



(a) (b)

Fig. 4-9. Total MOSFET losses in motor drive inverter (a) using SVM, (b) using DPWM1

Calculations predict that a single MOSFET per switch position would overheat, so paralleling is required. There is a big difference between 2 versus 3 in parallel for PSMN2R0-100SSF. With 2 in parallel, power loss per MOSFET is 4.2 W and 2.7 W for PSMN2R0-100SSF and PSMN1R3-100ASF respectively. This is under the worst-case scenario, so 2 in parallel is acceptable. The PSMN1R3-100ASF is a newer part with significantly better efficiency. Its copper clip construction results in better current sharing, and cost at time of writing is about the same as for the higher $R_{DS(on)}$ part. Therefore, two parallel PSMN1R3-100ASF is the preferred configuration for further investigation.

Technical tip: When paralleling MOSFETs, each must have its own gate resistor, or resistors if using separate switch-on -off resistors. Avoid using an “upstream” gate resistor and then branching out to each MOSFET gate, even if each MOSFET has a gate resistor. It is best to place all needed gate resistance at the gate of each MOSFET to maximize damping and prevent parasitic oscillations between parallel MOSFETs.

4.3.3. Gate Drive

It is important to understand gate charge and its thermal effect on the driver. Each PAC gate driver is a “totem pole” with effectively two MOSFETs connected in series, as indicated in Fig. 4-10. Current flows through the top or bottom driver MOSFET when the driven

MOSFET switches on or off respectively. The charge delivered to and extracted from the driven MOSFET gate is equal, meaning the area inside the gate current switch-on and off current curves is equal.

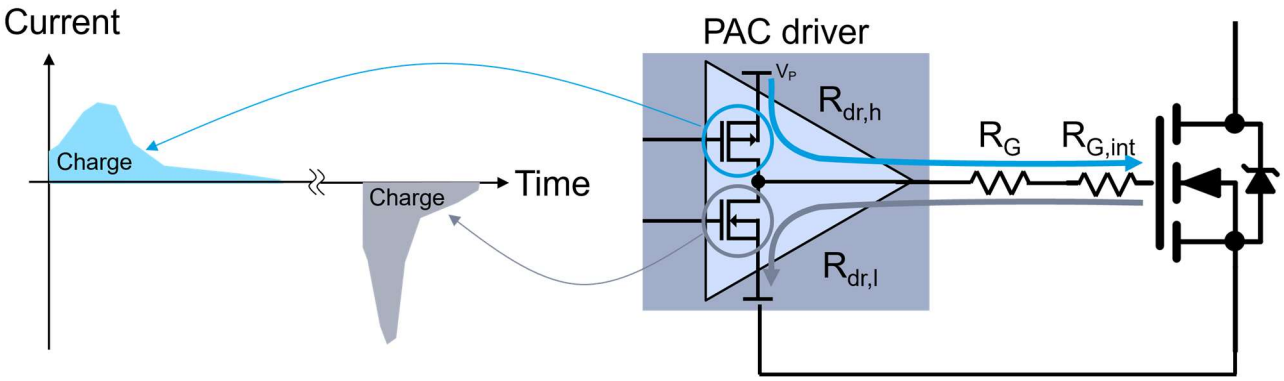


Fig. 4-10. Gate charge supplied to and extracted from MOSFET gate by PAC driver

Before building the motor drive, we need to know if we need to add a current buffer between the PAC drivers and each motor drive MOSFET. For this we use gate charge information in the MOSFET datasheet.

Power to the gate driver stage used for switching the driven MOSFET is $P_{driver,sw} = Q_{G(tot)} \cdot f_{sw} \cdot \Delta V_{GS}$, where $Q_{G(tot)}$ is the total gate charge from the external MOSFET datasheet, f_{sw} is the switching frequency, and ΔV_{GS} is gate voltage swing of the external MOSFET. Note that gate voltage swing for the datasheet gate charge must match that of the external MOSFET. All this power is lost during switching as heat in resistances in the gate current path, namely the driver MOSFET on resistances $R_{dr,h}$ and $R_{dr,l}$, external gate resistance R_G, and gate resistance inside the driven MOSFET $R_{G,int}$. Half the power is lost during switch-on, the other half during switch-off. Power loss in internal gate drive MOSFETs is therefore, by voltage division across the resistances:

$$P_{dr,h} = \frac{1}{2} \cdot Q_{G(tot)} \cdot f_{sw} \cdot \Delta V_{GS} \cdot \frac{R_{dr,h}}{R_{dr,h+R_{G,on}+R_{G,int}}}$$

$$P_{dr,l} = \frac{1}{2} \cdot Q_{G(tot)} \cdot f_{sw} \cdot \Delta V_{GS} \cdot \frac{R_{dr,l}}{R_{dr,l+R_{G,off}+R_{G,int}}}$$

The PAC5532B has 2.0 source and sink capability and drives to about 10 V. The internal driver resistances are equal and approximately 4.4 Ω. We selected two parallel 100 V, 1.02 mΩ (typical) MOSFETs for each switch position. Internal gate resistance is R_G = 1.08 Ω typical. Typical gate charge per selected MOSFET is 255 nC, driving between 0 and 10 V. For now, let R_G = 5 Ω. Gate driver power loss per driven MOSFET is:

$$P_{dr,h} = P_{dr,l} = \frac{1}{2} \cdot 255\ nC \cdot 20\ kHz \cdot 10\ V \cdot \frac{4.4\ \Omega}{4.4\ \Omega + 5\Omega + 1.08\Omega} = 10.7\ mW$$

These values must be doubled because of two driver MOSFETs inside PAC5532B and doubled again because of parallel driven MOSFETs. Total driver power loss per switch position is 43 mW, and the sum for all six drivers is 257 mW. This is a light thermal load considering the PAC5532B has an exposed bottom metal pad and junction-to-ambient thermal resistance of 23.4 °C/W. Estimated temperature rise due to gate driver loss is about 6 °C.

4.3.4. Motor Current Sense

Peak motor current is $\sqrt{2} \cdot 82$ = 116 A during overload (startup). This paper design uses low-side, 1 mΩ, 10 W current sense resistors with a low-inductance design, such as part number SEWF5930D1L00P9 from C&B Electronics. With a 2.5 V full-scale output, the differential amplifier gain in the PAC5532 could be set at 16 while still allowing measurement of 156 A peak current. Power dissipation during normal full-load current of 32.7 A rms is only 1 W.

4.3.5. Partial Motor Drive Schematic

Fig. 4-11 shows a simplified schematic implementation of gate drive and current sense for two parallel MOSFETs per switch position in phase U of the motor drive. High-side gate drive power is from a bootstrap for each phase, but node VP_BST is common for all phases. Low-side driver power is from VP. Following best practices for paralleling, each half-bridge MOSFET has its own gate resistor.

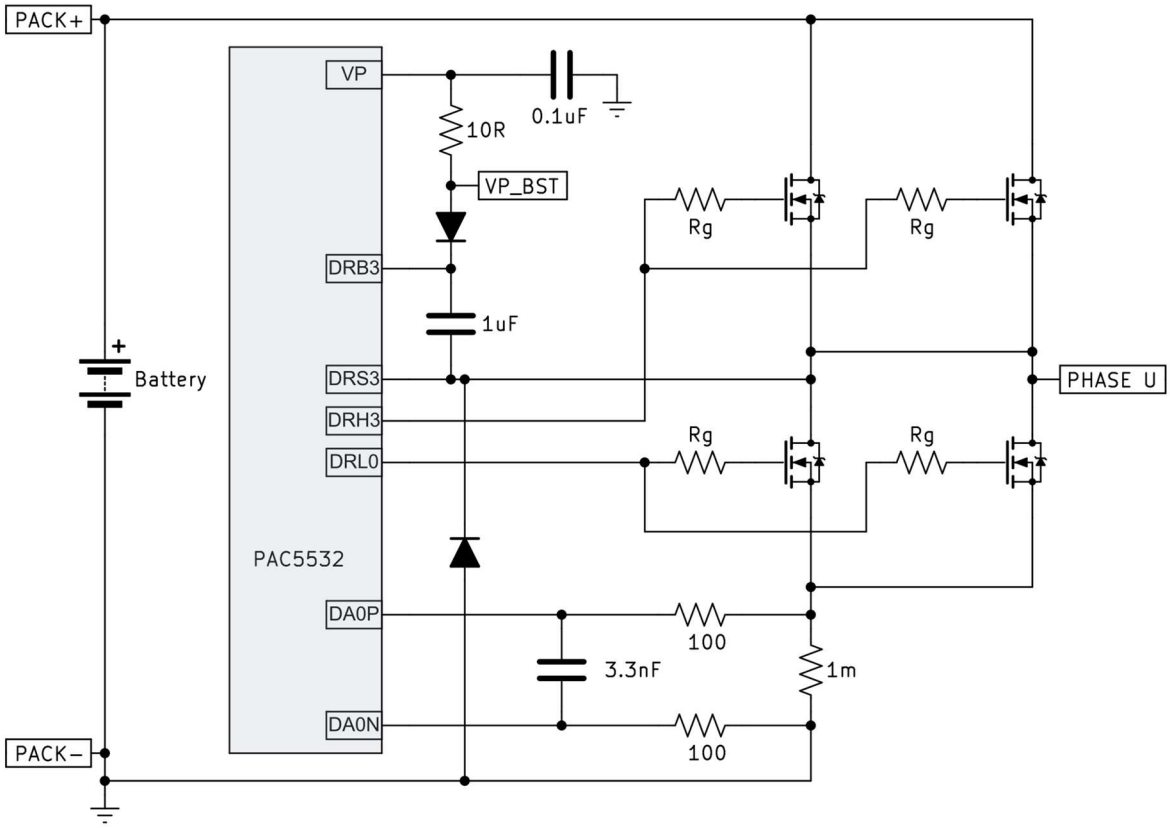


Fig. 4-11. PAC5532B gate drive implementation, phase U

5. Summary

This application note provides a comprehensive design guide for developing high-voltage, battery-powered outdoor power equipment using Qorvo's Power Application Controller® (PAC) battery management systems (BMS) and intelligent motor controllers. It reviews key requirements for tools such as lawnmowers, trimmers, and e-bikes, emphasizing safety, reliability, and efficiency as battery voltages and power demands increase. The document outlines PAC-based solutions for battery pack construction, active cell balancing, precision current measurement, power management, and protective circuitry, along with detailed design examples including a 52 V, 1500 W system to illustrate implementation of BMS and motor control functions. It also covers MOSFET selection, gate-drive considerations, inverter power-loss analysis, and practical thermal and protection strategies, providing engineers with step-by-step guidance to accelerate development and certification of robust, high-performance outdoor power equipment.

6. Appendix

Below is a Nexperia PSMN2R0-100SSF SPICE model created with QSPICE Model Generator for a MOSFET.

```
.model PSMN2R0-100SSF VDMOS Rs=611µ Rd=611µ Rg=1.4 Vto=3.82
+ Kp=98.4 lambda=55.4m RonX=4.04 eta=75m Vtotc=-2m Is=6.67µ
+ N=2.18294 Rb=164µ Eg=1.11 XTI=6.03973 trb1=-6.67m Cgs=10.5n
+ Cgdmin=178p Cgdmax=4.56n Cjo=4.44n tt=2.2n Tnom=25
+ mfg="Nexperia" Vds=100 Ids=267 Ron=1.63m Qg=161
```

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Revision History

Revision	Author	Date	Description
A	Jonathan Dodge, P.E.	17 September 2025	Initial draft
B	Jonathan Dodge, P.E.	20 October 2025	Changed battery monitoring to PAC battery management
C	Jonathan Dodge, P.E.	8 December 2025	Updated Fig. 4-2
D	Jonathan Dodge, P.E.	18 February 2026	Updated schematics, used loss calculator for MOSFETs

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