

PLP Capacitor Selection and Configuration

Abstract

This application note outlines Power Loss Protection (PLP) and explains storage capacitor selection and configuration for enterprise solid-state drives (SSDs) and server applications.

1. Introduction

Power loss protection (PLP) in a solid-state drive (SSD) prolongs operating time in the event of sudden power loss. During this extra time, the SSD transfers data from volatile memory (DRAM or SRAM cache buffers) to non-volatile FLASH memory and updates mapping tables, enabling a graceful SSD shutdown. Although some Qorvo PLPs include flexible power management features, this application note focuses exclusively on power loss protection functions and storage capacitor selection and configuration.

2. PLP System Overview

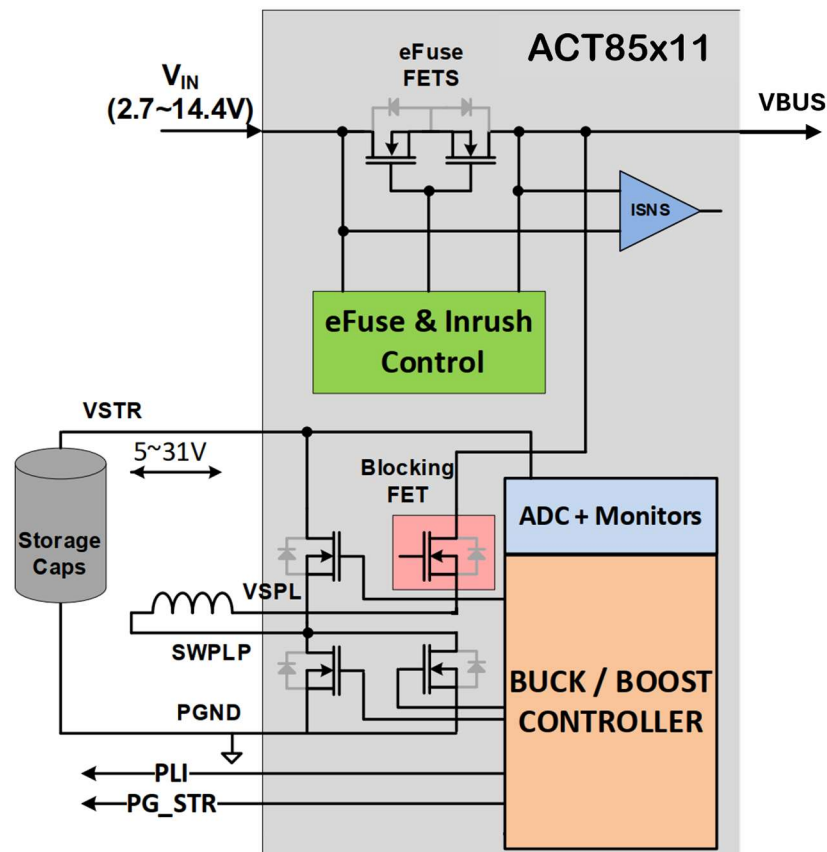


Fig. 2-1. Partial block diagram of a Qorvo PLP & Power Management IC



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Qorvo PLPs contain an e-fuse and a boost converter that shares an inductor with a buck converter. External storage capacitors provide the SSD with enough energy to shut down without data loss. The partial block diagram of Fig. 2-1 shows the connection between PLP-related components. In normal operation when power is good, the e-fuse connects the input V_{IN} to the output V_{BUS} with minimal power loss. If an input voltage fault occurs, the e-fuse switches off and operation transitions to supplement mode. In supplement mode, the PLP buck converter draws power from the storage capacitors and delivers current to the voltage-regulated output V_{BUS} . During startup or restart, the boost converter stores energy in the storage capacitors and subsequently maintains the storage voltage. High storage voltage reduces the storage capacitor bank volume by reducing the parallel capacitor count. Interface signals indicate to the SSD controller the status of input and storage voltages. Periodic telemetry checks during a slight discharge indicate capacitor fitness for use.

3. Energy Stored in Capacitors

Capacitance of an ideal capacitor is defined as the ratio of charge Q on conductors in the capacitor to the voltage V across the capacitor: $C = \frac{Q}{V}$

The work required to move an incrementally small charge from the negative to the positive plate of a capacitor is:

$$dW = \int_0^Q V(q) dq = \int_0^Q \frac{q}{C} dq = \frac{1}{2} \frac{Q^2}{C} = \frac{1}{2} CV^2$$

This is the energy stored in a capacitor. (Note that the energy required to charge a capacitor from a fixed voltage source through a resistor is QV or CV^2 , with $\frac{1}{2}CV^2$ dissipated in the resistor.) Capacitor-stored energy increases as the square of the capacitor's voltage. This provides motivation to boost the voltage of storage capacitors above the operating voltage. Higher voltage means less capacitor volume, which is an important benefit. Tantalum-polymer capacitors are popular in SSDs, but above 35 V rating, selection of these capacitors dwindles, and their cost skyrockets. Furthermore, safety margin between capacitor and PLP IC voltage ratings accommodates normal switching transients and extends service life. These constraints place a practical limit on the storage capacitor voltage, mostly due to the required capacitor voltage derating.

4. Storage Capacitor Selection

Diminishing returns in power conversion efficiency and system cost limit storage capacitor voltage to about 30 V. The PLP buck converter stepdown ratio approaches 10:1, which is only efficient with synchronous rectification. A transformer-based DC-DC converter would add excessive cost and complexity. Furthermore, the selection of economical, high charge per volume capacitors narrows with increasing voltage ratings.

Qorvo PLP & PMICs are compatible with many types of storage capacitors, including tantalum-polymer, aluminum-polymer, etc. Table 4-1 lists a variety of capacitor types and some important parameters. Criteria for each part type listed are:

- At least 10 μF apiece
- Voltage rating of at least 35 V
- Surface mount package

Tantalum-polymer capacitors surpass tantalum capacitors in energy density and stability. They are readily available in surface-mount packages and an excellent choice in SSDs. Aluminum-polymer surpass aluminum-electric in ESR and longevity, but taller packages preclude them from space-critical SSDs. When space allows, aluminum-polymer capacitors have good overall performance at very low cost. Film capacitors excel at higher operating voltages, but they are simply too bulky for such a relatively low voltage application as SSDs. Multi-layer ceramic capacitors are low cost and have super-low equivalent series resistance (ESR). However, they are considerably bulkier than tantalum-polymer, especially considering how DC bias reduces their capacitance and requires large voltage margin. Furthermore, ESR is important but not a top priority for SSD storage capacitors. The voltage rating of supercapacitors is too low, and series-connecting them is impractical in an SSD. Their packaging is also too bulky, despite huge charge density.

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Table 4-1. Comparison of various capacitor types

Type \ Parameter	Farads/Volume	Cost/Farads	Voltage	Stability	Longevity	ESR
Tantalum	Moderate	Moderate	125	Moderate	High	Low
Tantalum-polymer	High	Moderate	100	High	High	Low
Aluminum-electrolytic	Moderate	Low	450	Moderate	Moderate	Moderate
Aluminum-polymer	Moderate	Low	250	High	High	Low
Polyester film	Low	High	500	High	High	Low
Multi-layer ceramic	Low	Low	500	Low	High	Very low

Stability in Table 4-1 relates to change in capacitance and/or ESR versus temperature or bias voltage. Each high-stability capacitor type requires little voltage margin. Tantalum should operate at less than 80% of rated voltage. Aluminum-electrolytic, aluminum-polymer, and tantalum-polymer can operate at 80% of rated voltage, depending on temperature. A multi-layer ceramic capacitor (MLCC) operates at as little as 50% of rated voltage, depending on its construction.

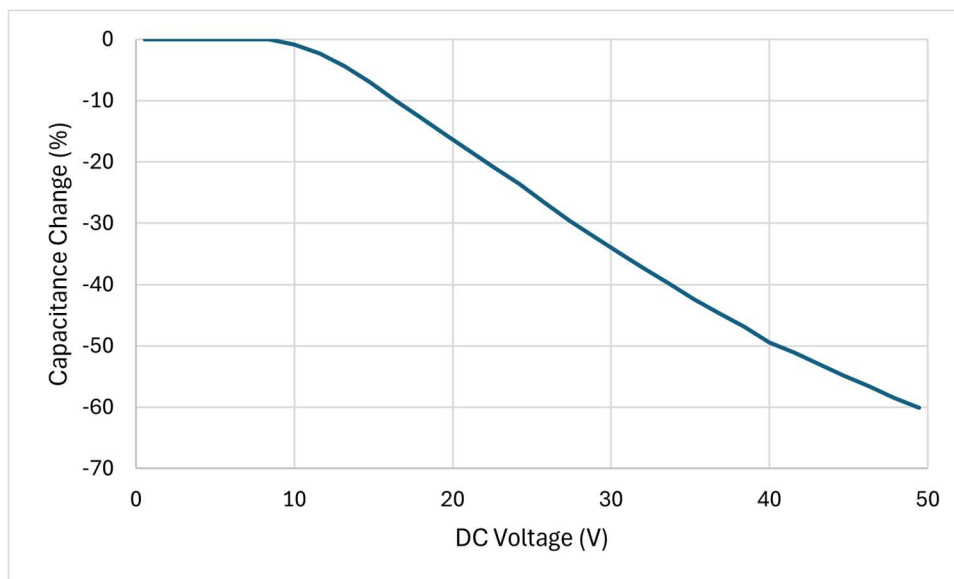


Fig. 4-1. Percent change in capacitance versus DC voltage for a 50 V rated, X7R MLCC

Fig. 4-1 shows the decrease in capacitance versus DC voltage for a 50 V rated X7R MLCC, which is in Class II. Class I capacitors on the other hand, such as C0G (NP0), are very stable and have almost no capacitance shift with DC or AC voltage (or temperature). The advantage of Class II versus Class I is volumetric efficiency. For example, a 0.1 μF , C0G MLCC with 50 V rating is available in a 1206 or larger package, whereas the 0.1 μF , X7R MLCC with 100 V rating fits in a much smaller 0603 package. Higher voltage margin accommodates the X7R reduction in capacitance due to DC voltage bias.

Tantalum-polymer and aluminum-polymer have excellent volumetric efficiency for both charge and energy, which explains their popularity for energy storage in enterprise SSDs. What happens when a boost or buck converter causes ripple current in these capacitors? Fig. 4-2 shows percent change in capacitance versus frequency for an MLCC with X7R dielectric, a 35 V tantalum-polymer, and a 35 V aluminum-polymer capacitor. These are all surface-mount capacitors. Except for an initial drop at very low frequency, the MLCC capacitance is stable versus frequency. Tantalum-polymer capacitance is stable up to a few hundred kilohertz, but near 1 MHz where a PLP IC typically operates, capacitance reduces to less than 40% of the nominal value. Aluminum-polymer capacitance in Fig. 4-2 derives from an impedance versus frequency chart for a 35 V, 270 μF , so it includes the effect of equivalent series resistance and inductance. The aluminum-polymer capacitance drops sharply beginning at low frequency despite low ESR (20 m Ω at 20 $^{\circ}\text{C}$, 100 kHz).

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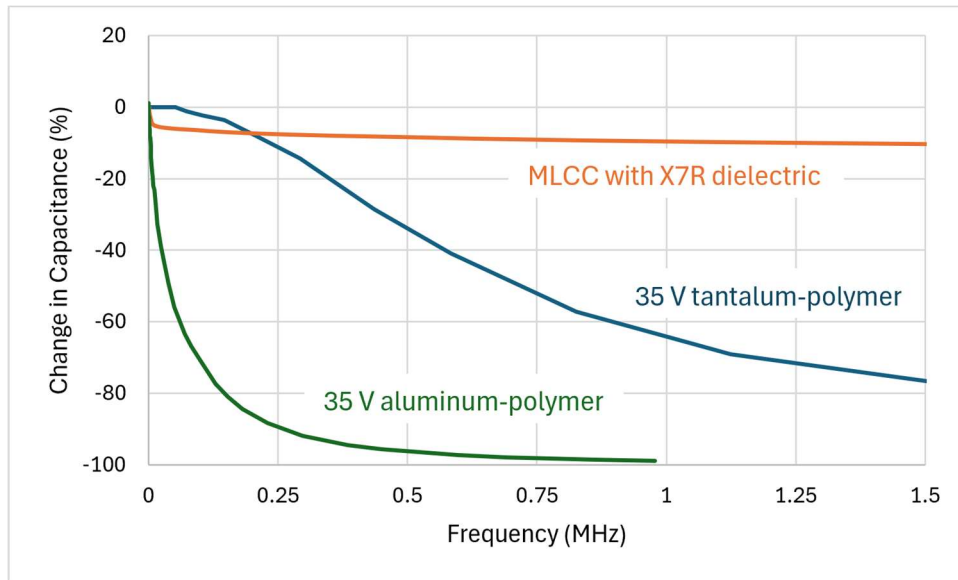


Fig. 4-2. Capacitance versus frequency for an X7R MLCC, a 35 V, 15 μF Ta-polymer, and 35 V, 270 μF Al-polymer capacitor

Combining MLCCs in parallel with either type polymer capacitor combines the benefits each capacitor type while the MLCC absorbs the switching ripple current. This is thanks to the ultra-low ESR of MLCCs, a fraction of a milliohm at typical PLP IC switching frequency. The MLCC capacitance value is unimportant because the polymer capacitors store the required energy. Circuit layout is critical. MLCCs must be next to the PLP IC, following layout guidelines for radio-frequency signals including a return plane under, or at least adjacent to MLCC connections to the PLP IC.

5. Storage Capacitance Calculation

Configuration is about choosing how many capacitors to connect in parallel to store sufficient PLP energy. Series connecting capacitors would add unnecessary complexity. Capacitor configuration depends on the following variables.

- Hold time t_{hold}
- Output power P_{out} is SSD power consumption
- Initial storage voltage V_{STR}
- SSD supply voltage V_{BUS}
- Storage capacitance C_{STR}
- Stored capacitance energy W_{STR}
- PLP buck converter efficiency η , which is typically 0.9, maximum 0.95

Energy consumption during supplement mode equals the change in stored capacitance energy.

$$\Delta W_{STR} = \frac{1}{2} C_{STR} (V_{STR}^2 - V_{BUS}^2) = \frac{P_{out}}{\eta} t_{hold}$$

The required storage capacitance is:

$$C_{STR} = \frac{2P_{out}t_{hol}}{\eta(V_{STR}^2 - V_{BUS}^2)}$$

After choosing a capacitor type, storage voltage, and adding sufficient voltage margin, the number of parallel capacitors is simply C_{STR} divided by per piece capacitance, rounded up.



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6. Design Example

Suppose we need to power an SSD for at least 40 ms after power loss. The SSD consumes 5 W while writing to FLASH, and it runs on 5 V. The height of the SSD is 7 mm, which precludes usage of any can-packaged capacitors, and consequently aluminum-electrolytic and aluminum-polymer are not options. Based on Table 4-1, tantalum-polymer is the best choice. If V_{STR} is 30 V, then the capacitor voltage rating must be at least $1.25 \cdot 30 = 37.5$ V. The nearest voltage rating is 40 V. However, at 40 V or higher, tantalum-polymer capacitor selection is limited and costly. Reducing V_{STR} to 28 V or less allows a 35 V rating, which greatly increases the selection pool. A good balance between cost and volume is 35 V rated, 100 to 150 μ F per piece, such as those listed in Table 6-1, among others.

Table 6-1. Partial list of 35 V rated tantalum-polymer capacitor examples for PLP in SSDs, alphabetical order

Manufacturer	Part Number (# = wildcard)	Capacitance (μ F)	Note
Kemet	T521O157M035ATE100	150	
Kemet	T523H107M035APE070	100	Facedown terminal
Kyocera-AVX	TCJU157M035#0100E	150	
Kyocera-AVX	TCN4107M035R0100	100	Facedown terminal
Vishay	T52M1107M035C0###	100	Facedown terminals
Vishay	T52M9107M035C0###	100	

The tantalum-polymer ratio of operating versus rated voltage is 80% maximum. This voltage margin exceeds the PLP & PMIC IC voltage margin requirement. For example, Qorvo ACT85611 and ACT85411 are characterized with a storage voltage of 31 V, and absolute maximum storage voltage is 33 V. This is because several parallel capacitors reduce the likelihood of an overvoltage transient, and parallel MLCCs to absorb switching ripple current. We focus on the 150 μ F tantalum-polymer capacitors for energy storage in this design example.

Before calculating the required capacitance, it would be wise to extend the hold time somewhat beyond the 40 ms requirement because we have assumed that the storage voltage drops to V_{BUS} just as the SSD finishes saving and cataloging its data, leaving no extra energy. We add 15% to the 40 ms hold time, so $t_{hol} = 46$ ms. Capacitor tolerance should be considered, which is $\pm 20\%$ for the two 150 μ F capacitors in Table 6-1. Although worst-case tolerance stacking may not be realistic, it would accommodate aging and capacitance measurement (health check) accuracy. Subtracting 20% from 150 μ F yields 120 μ F for use in the storage capacitance calculation. Storage voltage is programmable, and we set it to 28 V, which is 80% of the 35 V capacitor rating. Now we can calculate the total storage capacitance and then the number of parallel pieces.

$$C_{STR} = \frac{2 \cdot P_{out} \cdot t_{hold}}{\eta \cdot (V_{STR}^2 - V_{SPL}^2)} = \frac{2 \cdot 5 \text{ W} \cdot 0.046 \text{ s}}{0.9 \cdot (28 \text{ V}^2 - 5 \text{ V}^2)} = 673 \mu\text{F}$$

Dividing this by 120 μ F (150 μ F – 20%) and rounding up yields 6 parallel capacitors for a total of 720 μ F with tolerance stacking. Omitting the 20% capacitor stacked tolerance results in 5 parallel capacitors, only one piece-count difference. Using 100 μ F capacitors with the same 20% tolerance stacking results in 9 parallel capacitors.

Simulating supplement mode offers some important insights. Fig. 6-1 shows total current from the storage capacitors as well as voltage across them, assuming $C_{STR} = 720$ μ F. At 40 ms, the voltage falls from 28 to 13 V, and total current is 0.42 A. Beyond this point, the current increases sharply as the voltage decreases roughly quadratically. At 46 ms, the design target for t_{hol} , the voltage is 9.1 V and the current is 0.61 A. This chart highlights the prudence of adding safety margin to the hold time requirement.

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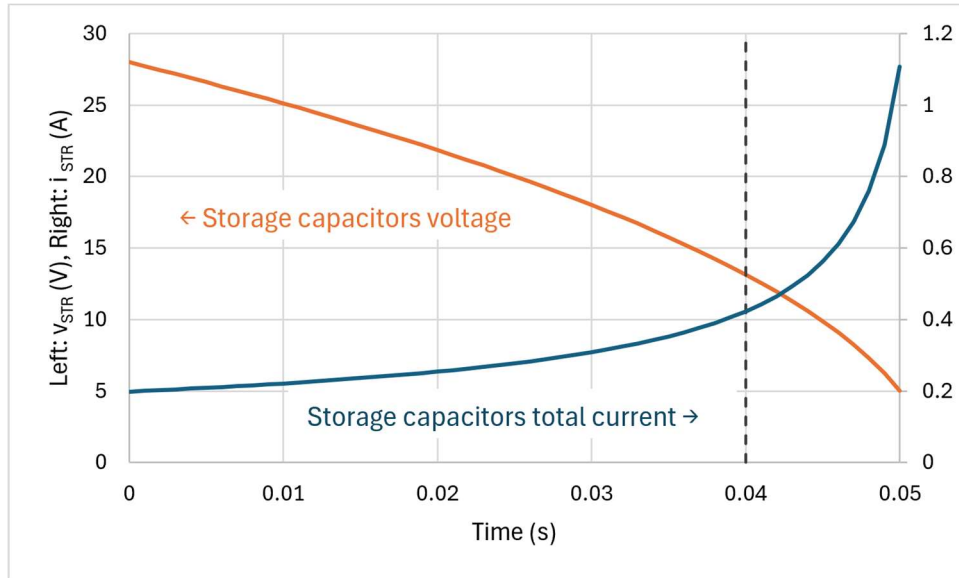


Fig. 6-1. Storage capacitors voltage and current at 5 W constant power to SSD, 90% conversion efficiency

Storage capacitor ripple current is root mean squared (RMS) current into the buck converter. This is $I_{pk} \cdot \sqrt{D}$, where D is the buck duty factor, which is approximately equal to the ratio of V_{BUS} to V_{STR} . At 40 ms, according to Fig. 6-1, $D \approx 0.38$, and peak current would equal total current divided by D , or $I_{pk} = 0.42 \text{ A} / 0.38 = 1.1 \text{ A}$, which is of course the current to the SSD (1 A) divided by buck converter efficiency. Ripple current is therefore $1.1 \text{ A} \cdot \sqrt{0.38} = 0.68 \text{ A RMS}$. This small current squared and multiplied by the ESR of an MLCC results in at most a few hundred microwatts of power to be dissipated. Just for example, a few parallel 100 V, X7R MLCCs such as 0.1 μF to 1 μF in 0805, or 1206 package should suffice. Wide voltage margin extends the service life of these MLCC capacitors.

For further design information, Qorvo datasheets contain detailed operating and application information, and evaluation kits are available.



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Revision History

Revision	Author	Date	Description
A	Jonathan Dodge, P.E.	4 Nov. 2025	Initial draft

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